DT0151
Design tip

Application of two SRK2001(A), each as single channel driver, to halve the dynamic power dissipation

A design tip is a description of an application oriented, technical implementation that leads to a specific benefit.
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Main components	
SRK2001	Adaptive synchronous rectification controller for LLC resonant converter
SRK2001A	

Purpose and benefits

The purpose of this design tip is to show the way a pair of SRK2001(A)s can be connected, each as single channel driver, to implement synchronous rectification control for the LLC resonant converter.

The proposed circuit allows to cut the power dissipation of the single device that is mainly dynamic power to drive the SR MOSFETs: in this way, a thermally critical situation could be solved.

Furthermore, it could give a useful degree of freedom in the placing and routing of the secondary side of flat TV power supplies. In fact, the study of the proposed solution has been pushed by one of the major players in that field.

Description

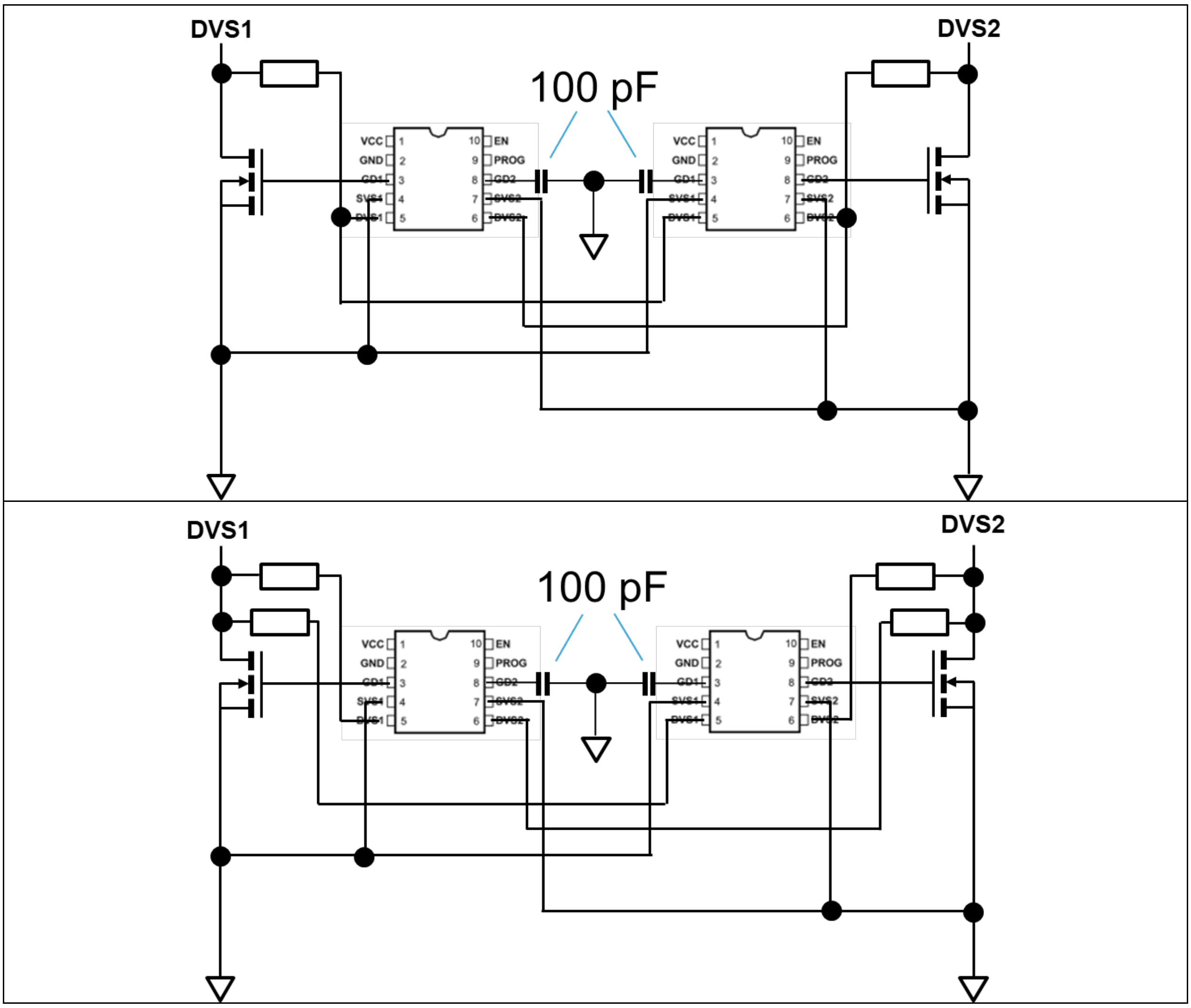
The SRK2001(A) is a dual channel controller for synchronous rectification of LLC converters. Its operation is based on the drain-source voltage at the SR MOSFETs sensed at dedicated pins and on the internal algorithms that find the turn-on and turn-off times to maximize the conduction time with respect to the rectified current.

The junction-ambient thermal resistance, R_{TH_JA}, of SRK2001(A) is 130 °C/W. If the static power consumption, $P_{STAT} = V_{CC} \cdot I_{CC}$, is neglected with respect to the dynamic power consumption, P_{DYNA}, then the following relationship holds true for the temperature increase due to the power dissipation: $\Delta T = R_{TH\_JA} \cdot P_{DYNA}$, where $P_{DYNA} = 2 \cdot N_{PAR} \cdot V_{CC} \cdot Q_{gSR} \cdot f_{sw}$ (N_{PAR} is the number of SR MOSFETs in parallel driven by SRK2001A and Q_{gSR} is the gate charge of the SR MOSFET computed according to AN2644, Appendix A, for instance).

In the expression of the dynamic power, the factor 2 is for the two sections of the SRK2001(A): the proposed solution allows to reduce this factor from 2 to about 1, since the unused driver is charged by a small dummy capacitor. So, the temperature increase of each SRK2001(A) instance is practically halved.

The schematic of the proposed solution is given hereinafter, in Figure 1, in two equivalent versions. In practice, alternate sections of the two instances of the controller are used. The section that is not used is charged with a dummy capacitor and connected to the corresponding DVS signal. In this way, the two instances can work properly, despite the fact that one section only of each is driving an SR MOSFET.

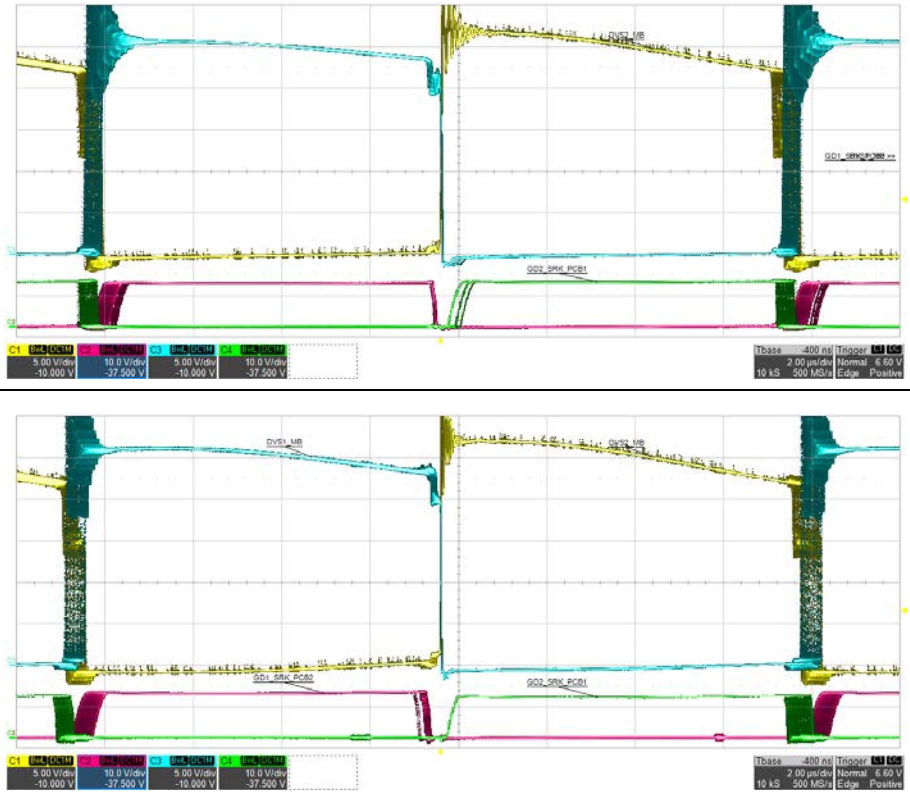
Figure 1. Circuit diagram: with common series resistor on DVS pins (top), with separated series resistors on DVS pins (bottom).



The first validation step of the proposed solution has been done on a static test board where the signals to the DVS pins are from an arbitrary waveform generator. In this way, correct behavior of the proposed solution in a safe environment has been demonstrated.

Then, the proposed solution and the traditional solution have been compared on the very same application board: the 400 W / 12 V adapter with L4984 and L6699 at the PFC and the LLC stages, respectively. Some results of this second validation step are reported hereinafter for reference.

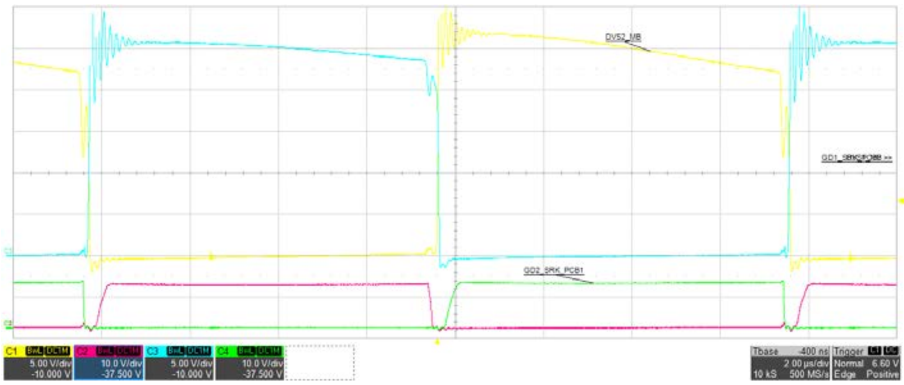
Figure 2. 230 Vac / 33 A (Full Load), Original SR board (top) and Proposed SR board (bottom).



CH1, CH3: input signals at DVS pins / CH2, CH4, output signals at GD pins
Oscilloscope in infinite persistence, trigger on rising edge on CH1

The two solutions do behave almost in the same way: the proposed solution shows larger jitter at turn-off, but no jitter at turn-on. The measured efficiency is practically the same. In the following figure, a typical switching cycle on the proposed solution is shown, with the oscilloscope in normal acquisition mode (no persistence).

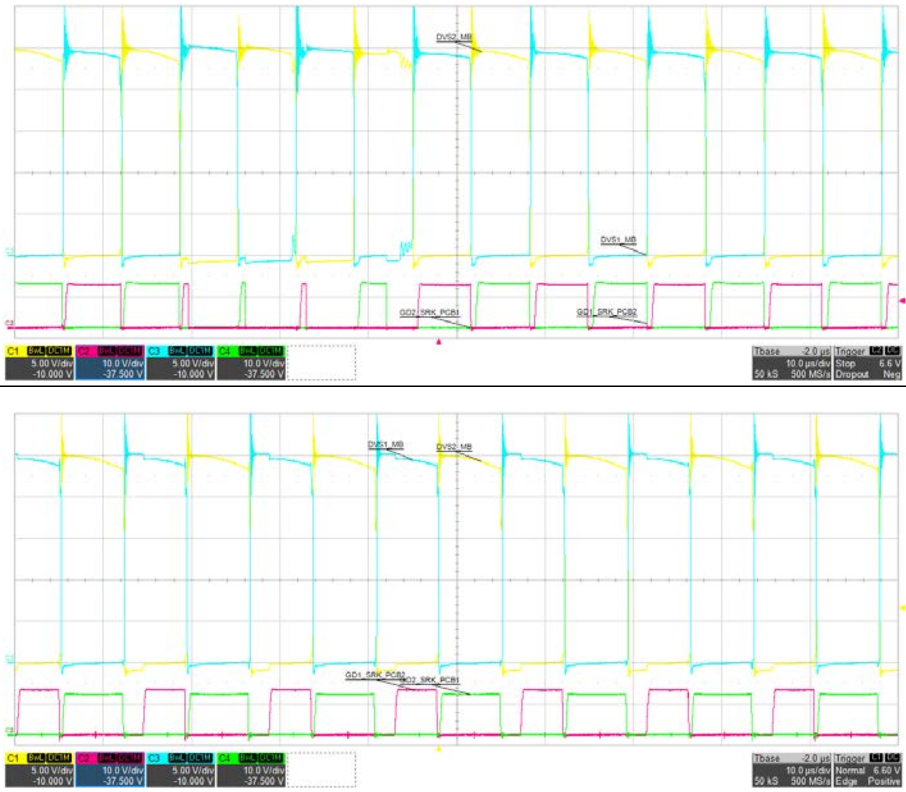
Figure 3. 230 Vac / 33 A (Full Load), Proposed SR board (bottom), Full switching cycle.



CH1, CH3: input signals at DVS pins / CH2, CH4, output signals at GD pins

About the half load, in detail between about 10 A and 17 A, on one side, the proposed solution seems to suffer from delayed turn-on, on section 1: GD1 pulses are generated with a delay of about 1.5 us with respect to a DVS1 pulse of about 6 us. Conversely, it does not generate the narrow GD pulses that can be observed on the traditional solution (random earlier turn-off). The difference has not been investigated but could be related to the actual implementation of the proposed solution that has not been optimized and/or to the actual rectified current that is flowing in the SR MOSFETs. The described behavior is shown in the following figure.

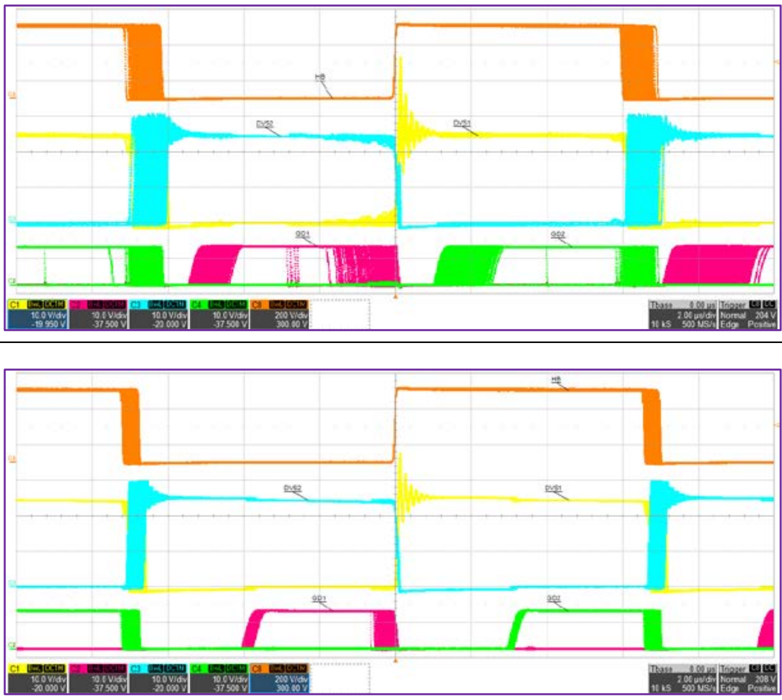
Figure 4. 230 Vac / 15 A, Original SR board (top) and Proposed SR board (bottom).



CH1, CH3: input signals at DVS pins / CH2, CH4, output signals at GD pins
Random narrow pulses on GD1 and GD2, in the traditional solution.
Systematic delayed turn-on, on GD1, in the proposed solution.

At around 5 A, in the proposed solution, both sections seem to suffer from delayed turn-on, but with respect to the traditional solution, the behavior is steady-state: narrower jitter at turn-on and turn-off and no narrow pulses observed. However, overall, the average width of the GD pulses generated by the traditional solution is larger than the proposed solution, so the efficiency of the former is slightly better than the latter. The following figure clarifies the given description.

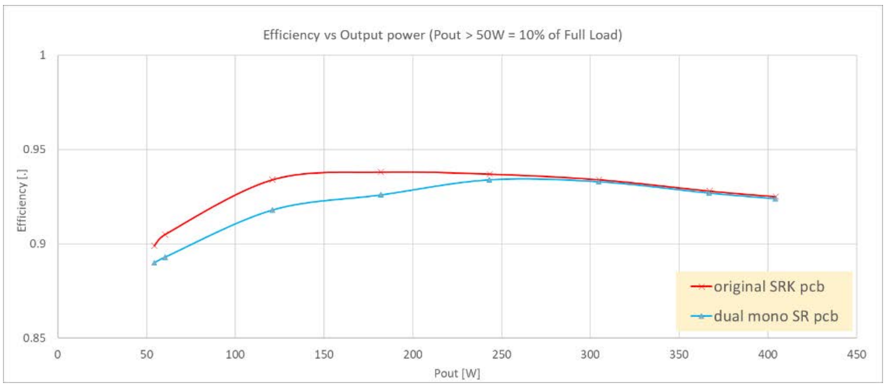
Figure 5. 230 Vac / 4.5 A, Original SR board (top) and Proposed SR board (bottom).



CH1, CH3: input signals at DVS pins / CH2, CH4, output signals at GD pins
CH8: half-bridge node at primary side.

The validation of the proposed solution also included the analysis of its behavior at some dynamic conditions like load transients and output short-circuits: in the considered cases, the behavior is aligned with one of the traditional solutions. Eventually, a comparison at efficiency level has been carried out on both solutions, using the very same motherboard. As expected from previously reported results, the proposed solution has a slightly worse efficiency than the traditional solution from about 50% load to 10% load. The efficiency diagram is shown in the following figure.

Figure 6. efficiency of the traditional and proposed solutions, at 230 Vac.



Support material

Related design support material
STEVAL-ISA165V1: a pair of STEVAL-ISA165V1 samples have been used to demonstrate the solution and can be used to build a custom prototype
Documentation
Datasheet SRK2001(A), Adaptive synchronous rectification controller for LLC resonant converter

Revision history

Date	Version	Changes
01-Mar-2022	1	Initial release.