SPC58xNx
Errata sheet

SPC584Nx, SPC58ENx, SPC58NNx devices errata
JTAG_ID = 0x1011_2041

Introduction

This errata sheet describes functional and electrical problems of the SPC584Nx, SPC58ENx, SPC58NNx devices.

The reference documentation is reported in *Chapter 2: Reference document*.

Device identification for cut 1.1:

- JTAG_ID = 0x1011_2041
- MIDR1 register:
  - MAJOR_MASK[3:0]: 4’b0000
  - MINOR_MASK[3:0]: 4’b0001

Errata and BAF related errata are contained in Microsoft Excel® workbook files attached to this document.

Locate the paper clip symbol on the left side of the PDF window, and click it. Double-click on the Excel file to open it.

1 BAF Image version

The BAF version is a 32-bit field in the image header starting at address 0x0040_4000. The 32 bit-bit field is explained in the following table.

Table 1. BAF Image version registers

Field	Description
0:7	Major Number: This field contains the major version number for the BAF image
8:15	Minor Number: This field contains the minor version number for the BAF image
16:31	Reserved

2 Reference document

Table 2. Reference documents

Doc name	ID	Title	Revision
RM0421	DM00239196	SPC58xNx 32-bit Power Architecture® microcontroller for automotive ASILD applications	3
DS11734	DM00307505	32-bit Power Architecture® microcontroller for automotive ASIL-D applications	5

Revision history

Table 3. Document revision history

Date	Revision	Changes
30-Jun-2017	1	Initial release
13-Dec-2017	2	1) GTM erratum removed (not applicable to SPC58xNx) – DAN-0041994 GTM: Loss of data for PMT transfer to DPLL via ARU Removed errata – DAN-0043282 FUSE: VDD_HV supply of FUSE is not connected ID change for an erratum: legacy ID had been picked up in previous generation the current one would be the correct one – DAN-0042364 AMU: Incorrect operation with spurious MEMU/FCCU errors when AMU is working with APC enabled. => – DAN-0042750 AMU: Incorrect operation with spurious MEMU or FCCU errors when AMU is working with APC enabled. 8 new normal errata (5 GTM) – DAN-0043442 GTM: TIM Serial shift mode (TSSM) no capture on bit number event if external capture is enabled – DAN-0043443 GTM: TOM/ATOM CCU0 interrupt at the wrong time in case of RST_CCU0=1 – DAN-0044106 GTM: Accessing MCS RAM while disabling last MCS channel fails – DAN-0044107 GTM: Access to the ADC interface address range by MCS while a CPU access to an address in the same cluster is pending will stall the MCS bus master interface – DAN-0044108 GTM: If the buffer of a MCS bus master interface is full and new accesses are scheduled by other MCS channels, the MCS bus master interface will block forever – DAN-0044109 Q100-JEDEC78D: Device non-compliant with Pin Latch-up I-tests on some pads – DAN-0044555 LINFlexD: in UART mode, receiver can miss counting incoming frames if framing errors are present – DAN-0045056 Decimation filter: No transfer error generated for accesses within the unused range of the decimation filter peripheral memory map NOTE: DAN-0044109 is the PS2992 erratum (Pad latchup), figuring with a distinct DAN ID
02-Feb-2018	3	Removed errata (not applicable to Bernina): – PS864 MEMU ECC bits not included in MEMU error log (ERR005611) BAF 01.01 Errata

Table 3. Document revision history (continued)

Date	Revision	Changes
06-Jul-2020	4	Removed errata: – ERR006836 DCF: DCF record for initial IVPR cannot be used New Errata: – DAN-0041121 SARADC: Some MCR register bits should not be asserted high together. – DAN-0041154 [DOC] SARADC: need to check MSR register before raising new command – DAN-0041182 SAR ADC: Normal conversion chain does not resume correctly if interrupted. – DAN-0043474 SARADC: The delay programmed in ECDSDR.DSD occurs before setting the external multiplexer pins – DAN-0044114 JTAGM: JTAGM_SR[15] may not report the debugger connection – DAN-0046042 GTMINT: GTM (Generic TImer Module) DTM Module Auxiliary Inputs may not function correctly – ERR008310 XBIC: Crossbar Integrity Checker may miss recording information from an initial fault event in the case of back-to-back faults – ERR008547 e200z425: Additional cycles required for Load/Store accesses to guarded/precise space Reworded errata: – DAN-0043138 STCU2: False FCCU alarms and MEMU entries after On line self-test execution of LBIST partition 0, 3, 4 or 5. – DAN-0043599 MEMU: Fake entries after offline LBIST execution on Partition0 – DAN-0043762 SDADC: Degraded common mode rejection ratio (Vcmrr) and absolute value of the ADC gain error (|dGAIN|) values. – ERR007701 STCU2: Short Functional Reset reaction and Long Functional Reset reaction of the FCCU does not take effect upon PLL1 Loss-Of-Lock while MBIST ONLINE is running – ERR007869 FCCU: FOSU monitoring of a fault is blocked for second or later occurrence of the same fault – ERR008145 MEMU: address registers in the uncorrectable error reporting tables can be written when the corresponding valid bit is not asserted BAF 01.01 Rev 2. Added errata: – DAN-0044825 MC_CGM: CGM_ACx_SC registers not reset after a destructive reset event – DAN-0046237 BAF: TDM diary size in use is 2K instead of 4K

Table 3. Document revision history (continued)

Date	Revision	Changes
05-Oct-2018	5.0	**New Errata:** – DAN-0043444 GTM: TIM captured value in TIM[i]_CH[x]_GPR1 incorrect – DAN-0043446 GTM: AEI configuration interface using standard protocol in synchronous mode with write-buffer enabled may behave incorrectly (a write transaction can be executed twice) – DAN-0043447 GTM: AEI configuration interface using pipelined protocol writing to GTM_BRIDGE_MODE not fully functional – DAN-0043628 MC_CGM: CGM_ACx_SC registers not reset after a destructive reset event – DAN-0046687 GTM: Back-to-back TIM data transfers at full ARU clock rate cannot be transferred correctly with ARU dynamic routing mode – DAN-0046689 GTM: Aborting an AEI access to the GTM when bridge buffer is full results in an unexpected behavior – DAN-0046692 GTM: unexpected (A)TOM_CCU1TCx_IRQ interrupts in (A)TOM configured in up/down counter mode – DAN-0046703 GTM: GTM_HALT_ACTIVE signal incorrect – DAN-0047497 STCU2: Device can get stuck after execution of online MBIST – DAN-0047602 [DOC] SDADC: Full scale values as mentioned in Reference Manual chapter "Gain Calibration support"? may vary with different OSR configurations. – DAN-0047687 e200z425: Specific instructions executed immediately after reset can cause RCCU alarms of the core to be asserted. – DAN-0047977 MCAN: Unexpected High Priority Message (HPM) interrupt. – DAN-0047979 MCAN: Message transmitted with wrong arbitration and control fields. – DAN-0047983 Interrupt flag IR.ARA not set when accessing reserved addresses 0x144 to 0x1FF. – DAN-0047984 MTTCAN: Unexpected High Priority Message (HPM) interrupt. – DAN-0047985 MTTCAN: Message transmitted with wrong arbitration and control fields. – DAN-0048196 [DOC] PMC_DIG: wrong description of timing values for testing of voltage monitor BIST – DAN-0048198 SDADC: Degraded VDD_HV_ADV power supply current (each ADC IADV_D) and BIAS consumption (IBIAS) – DAN-0048204 SIUL2: Incorrect flash size value reported by MIDR2 register – DAN-0048205 STCU2: Spurious faults on FCCU channel 10 and/or 12 may occur after Online self-test **Reworded errata:** – PS2949 – PS2582 – PS2817 – PS3021 – ERR007869

Table 3. Document revision history (continued)

Date	Revision	Changes
7-Jun-2019	6.0	**Modified Errata:** – PS2231 – PS3021 **New ERRATA**: – DAN-0048189 – DAN-0048576 – DAN-0048678 – DAN-0048968 – DAN-0049480 – DAN-0049907 – ERR007873 **Removed ERRATA**: – ERR007791 – DAN-0041154 – DAN-0048196 – DAN-0047602
10-Dec-2019	7.0	**Reworded Errata:** – DAN-0041120 (PS2857) **New Errata:** – DAN-0048664 – DAN-0049972 (Security) – DAN-0050273 – DAN-0050583 – DAN-0050632 – ERR010436
06-Jul-2020	8.0	**New Errata:** – DAN-0051367 – DAN-0051392 – ERR009658 – ERR010542 **Reworded Errata:** – DAN-0042615