

## M24C64X-FCU and M24C64X-FCP read operations on chip enable register update

### Silicon identification

This errata sheet applies to M24C64X-FCU and M24C64X-FCP, 64-Kbit serial I<sup>2</sup>C bus EEPROMs, with configurable device address and software write protection, delivered in 4-ball CSP.

[Table 1](#) gives the list of the available part numbers impacted by this change.

**Table 1. Device summary**

Reference	Part number
M24C64X-FCU	M24C64X-FCU6T/TF
M24C64X-FCP	M24C64X-FCP6T/TF

# 1 Description of the change

This errata sheet refers to the section and figure detailing the read operations on chip enable register of the datasheet M24C64X-FCU M24C64X-FCP Rev 6 (DS12107).

The section must be modified from:

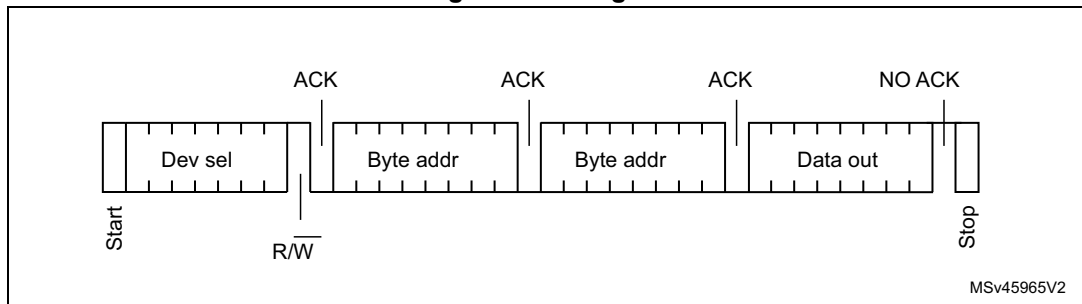
“Following a start condition the bus master sends a device select code with the R/W bit (RW) set to 1. The device acknowledges this and waits for the address bytes where the register is located. The device responds to each address byte with an acknowledge bit and then the master sends additional clock pulse so that the device outputs the byte of data.”

to:

“Following a start condition the bus master sends a device select code with the R/W bit (RW) set to 0. The device acknowledges this and waits for the address bytes where the register is located. The device responds to each address byte with an acknowledge. Then, the bus master sends another start condition, and repeats the device select code with the RW bit set to 1. The device acknowledges this, and outputs the contents of the chip enable register.”

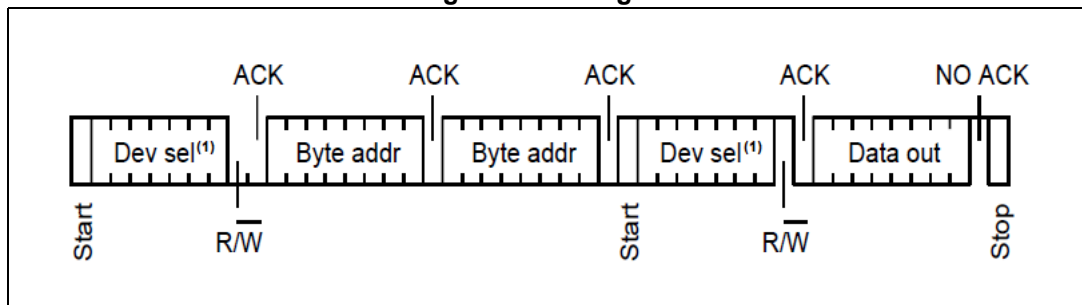
The figure must be modified as a standard random address read from:

**Figure 1. Old figure**



to:

**Figure 2. New figure**



1. The seven most significant bits of the device select code of a random read (in the first and fourth bytes) must be identical.

## 2 Revision history

**Table 2. Document revision history**

Date	Revision	Changes
11-Jul-2019	1	Initial release.

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