ST10F271B/E, ST10F272B/E
Errata sheet

BAG silicon version

Introduction

This errata sheet describes all the functional and electrical problems known in the BAG silicon version of ST10F271B, ST10F271E, ST10F272B and ST10F272E microcontrollers (MCUs).

Note: The ST10F271B, ST10F271E, ST10F272B and ST10F272E devices are commercial products based on the same silicon. Therefore the present errata sheet is valid for the four devices.

The major revision of the device can be read in the IDCHIP register (@F07Ch) which is set to 1102h for all these devices.

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1.1 Functional problems summary of the ST10F271B/E

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IDLE.1	Flash wake-up from Idle mode
PWRDN.1	Execution of PWRDN instruction
PWRDN.4	Flash wake-up from Power Down mode

Table 2. Functional problems of the ST10F271E-BAG

Functional Problem	Short Description
BUS.9	Spurious BREQ pulse in Slave mode during external bus arbitration phase
IDLE.1	Flash wake-up from Idle mode
PWRDN.1	Execution of PWRDN instruction
PWRDN.4	Flash wake-up from Power Down mode

1.2 Functional problems summary of the ST10F272B/E

Table 3. Functional problems of the ST10F272B-BAG

Functional Problem	Short Description
BUS.9	Spurious BREQ pulse in Slave mode during external bus arbitration phase
IDLE.1	Flash wake-up from Idle mode
PWRDN.1	Execution of PWRDN instruction
PWRDN.4	Flash wake-up from Power Down mode

Table 4. Functional problems of the ST10F272E-BAG

Functional Problem	Short Description
BUS.9	Spurious BREQ pulse in Slave mode during external bus arbitration phase
IDLE.1	Flash wake-up from Idle mode
PWRDN.1	Execution of PWRDN instruction
PWRDN.4	Flash wake-up from Power Down mode

2 Functional problems description

BUS.9 Spurious BREQ pulse in slave mode during external bus arbitration phase

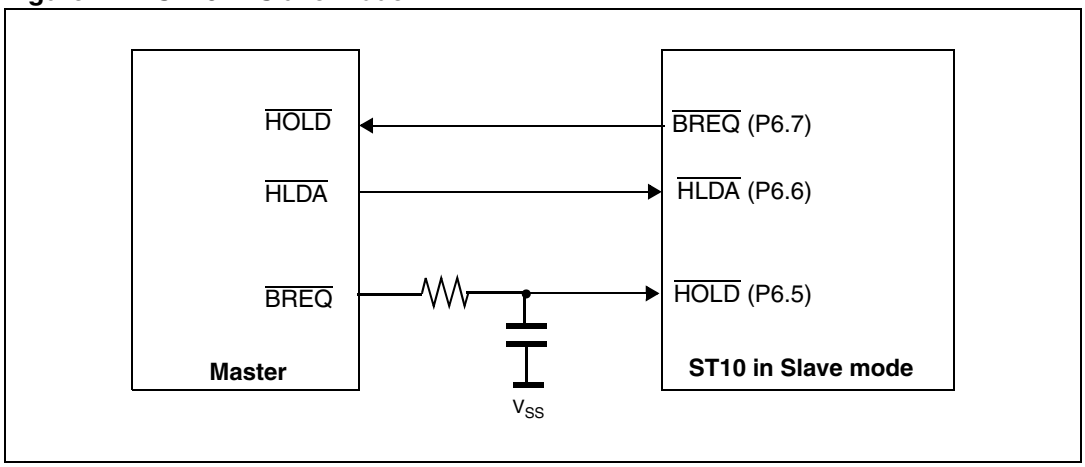
Description: When using external bus arbitration via the HOLD function with the ST10F271B/E - ST10F272B/E configured as a slave, sporadic bus errors may occur.

After the slave has been granted the bus, the slave deactivates BREQ sporadically for a short time, even though the bus access of the slave has not been completed. The master then starts its own bus access, leading to a bus conflict between master and slave.

Workaround: In order not to produce any spurious BREQ pulse during a Slave External Bus Arbitration Phase, it is necessary to guarantee that the time between the HOLDA assertion (Bus Acknowledge from Master device) and the following HOLD falling edge (Bus Request from Master) is greater than three clock cycles.

This can be implemented by delaying the HOLD signal with an RC circuit as shown in *Figure 1*.

Figure 1. ST10 in Slave mode



IDLE.1 Flash wake-up from Idle mode

Description: When coming back from Idle mode, the Flash response time is slower than in running mode. This can lead to an incorrect data read or code fetch when the CPU frequency is greater than 55 MHz.

As a consequence, the use of IDLE instruction is not allowed for frequencies greater than 55 MHz.

Workaround: There is no workaround for frequencies greater than 55 MHz.

PWRDN.1 Execution of PWRDN instruction

Description: When instruction PWRDN is executed while pin $\overline{\text{NMI}}$ is at a high level (if PWDCFG bit is cleared in SYSCON register) or while at least one of the Port 2 pins used to exit from Power Down mode (if PWDCFG bit is set in SYSCON register) is at the active level, Power Down mode is not entered and the PWRDN instruction is ignored.

However, under the conditions described below, the PWRDN instruction is not ignored, and no further instructions are fetched from external memory, that is, the CPU is in a quasi-idle state.

This problem only occurs in the following situations:

– The instructions following the PWRDN instruction are located in an external memory and a **multiplexed bus** configuration **with memory tristate waitstate** (bit MTTCx = 0) is used.

– The instruction preceding the PWRDN instruction **writes** to external memory or an XPeripheral (such as XRAM or CAN) and the instructions following the PWRDN instruction are located in external memory. In this case, the problem occurs for any bus configuration.

Note: The on-chip peripherals still work correctly, in particular the Watchdog Timer. If the Watchdog Timer is not disabled, it resets the device upon an overflow. Interrupts and PEC transfers, however, cannot be processed. If $\overline{\text{NMI}}$ is asserted low while the device is in this quasi-idle state, Power Down mode is entered.

No problem occurs if the $\overline{\text{NMI}}$ pin is low (if PWDCFG = 0) or if all Port 2 pins used to exit from Power Down mode are at inactive level (if PWDCFG = 1): The chip normally enters Power Down mode.

Workaround: Ensure that no instruction that writes to external memory or to an XPeripheral precedes the PWRDN instruction. Otherwise, insert a NOP instruction in front of PWRDN. When a multiplexed bus with memory tristate wait state is used, the PWRDN instruction must be executed from internal RAM or XRAM.

PWRDN.4 Flash wake-up from Power Down mode

Description: When waking up from interruptible Power Down mode, the Flash response time is slower than in Running mode. This can lead to an incorrect data read or code fetch when the CPU frequency is greater than 55 MHz.

As a consequence, exiting from Interruptible Power Down mode with an external interrupt is not supported for frequencies greater than 55 MHz.

Workaround: There is no workaround for frequencies greater than 55 MHz.

Note: Exiting from Interruptible Power Down mode with an external reset is supported at all frequencies.

3 Specification issues

3.1 Documentation update

Previous references: *ST10272B/E Datasheet (Custom data)*, Rev. 2.0, September 2005
ST10272B/E Datasheet, Rev. 0.9, September 2005

New references: *ST10272B/E Datasheet*, Rev. 1, July 2006

3.2 DC and AC parameters modifications

The following parameters are corrected and are now compliant with the target specifications:

- V_{HYS} (Input Hysteresis in TTL threshold): This parameter is now 400mV instead of 500mV.
- **VCO frequency range**: The VCO frequency range is now 64 to 128 MHz instead of 40 to 128 MHz.
- t_{LOCK}: The PLL Lock-in time for x10 multiplication factor is now 300µs instead of 250µs.

3.3 Flash commands timings updated

Characterization and validation results show that the typical programming and erasing times for the Flash are longer than the values previously specified in the ST10F272 Preliminary Data. This point was formerly referenced as FLASH.3 in the errata sheet of the previous silicon versions of the ST10.

Timings for erase and programing are corrected.

3.4 Main voltage regulator must be OFF in Power Down mode

Characterization and validation results show that the main voltage regulator must be switched off during Power Down to meet power consumption specification and avoid possible CPU wake-up. This point was formerly referenced as PWRDN.3 in the errata sheet of the previous silicon versions of the ST10.

The main voltage regulator must be turned off in Power Down by setting bit VREGOFF in XMISC register (bit XMISC.3). The new documentation is fully compliant with this specification change.

4 Revision history

Table 5. Revision history

Date	Revision	Description of changes
27-Nov-2006	1	Initial release for the BAG silicon version
25-Sep-2013	2	Updated disclaimer.