

Silicon identification

This errata sheet applies to the STMicroelectronic's SPIRIT1.

The full list of part numbers is shown in the table below.

Table 1: Device summary

Part numbers	Device info (stored in register 0xF0 and 0xF1)	Comment
SPIRIT1QTR	0x0130	Cut 3.0

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1 Limitations

1.1 Automatic VCO calibration

1.1.1 Part number affected

SPIRIT1QTR.

1.1.2 Description

In sporadic cases, the VCO calibrator sets an inaccurate calibration word. This can cause the inability to communicate.

1.1.3 Workaround

The following workaround is to use manual calibration and store the calibration word in the micro for each center frequency that the application intends to use. This manual calibration procedure should be repeated periodically to compensate for the temperature variation.

The steps are as follows:

1. Set the T split time to the longest value (3.47 ns) to facilitate calibrator operation, write 1 in SEL_TSPLIT, register SYNTH_CONFIG[0] (register address 0x9F). It is recommended to set this register during radio initialization.
2. If the reference clock is 48 MHz, 50 MHz or 52 MHz and the reference divider is not enabled, it must be enabled. Write 1 in the REFDIV bitfield, register SYNTH_CONFIG (register address 0x9E), and set the center frequency using the reference divider.
3. The VCO current must be increased by writing 0x25 in the register VCO_CONFIG (register address 0xA1).
4. Enable automatic calibration of the VCO, writing 1 in VCO_CALIBRATION, register PROTOCOL[2] (register address 0x50).
5. This step must be carried out only when the device is used as a transmitter.
 - a. Send a LOCKTX command and wait for the SPIRIT1 to go into LOCK state.
 - b. Read the VCO calibration word from VCO_CALIBR_DATA, register RCO_VCO_CALIBR_OUT[0] (register address 0xE5). Write the value read into the VCO_CALIBR_TX, in register RCO_VCO_CALIBR_IN[1] (register address 0x6E); optionally this value can be saved in the micro NVM.
 - c. Send a READY command and wait for SPIRIT1 to go into READY state.
6. This step must be carried out only if the device is used as a receiver.
 - a. Send a LOCKRX command and wait for the SPIRIT1 to go into LOCK state.
 - b. Read the VCO calibration word from VCO_CALIBR_DATA, register RCO_VCO_CALIBR_OUT[0] (register address 0xE5). Write the value read into the VCO_CALIBR_RX, in register RCO_VCO_CALIBR_IN[0] (register address 0x6F); optionally this value can be saved in the micro NVM.
 - c. Send a READY command and wait for SPIRIT1 to go into READY state.
7. Disable the automatic calibration of the VCO, write 0 in VCO_CALIBRATION, register PROTOCOL[2] (register address 0x50).
8. If step 2 was executed, restore the reference divider state. Write 0 in the REFDIV bitfield, register SYNTH_CONFIG (register address 0x9E). Again, set the center frequency.

It is strongly suggested to repeat this sequence if the ambient temperature changes by many degrees.

1.2 Extra current consumption after power-on

1.2.1 Part number affected

SPIRIT1QTR.

1.2.2 Description

In some samples, when a supply voltage below 2.6 V is applied to SPIRIT1 from a no power condition, an extra current is added to the typical current consumption. In the following table, the current consumption in SHUTDOWN state is reported according to the supply voltage.

Table 2: Current consumption in SHUTDOWN state

VBAT [V]	IBAT [μ A]
2.4	~150
2.2	~110
2.0	~74
1.8	~22

1.2.3 Workaround

In order to avoid this extra current, after the supply voltage below 2.6 V is provided to SPIRIT1, SPIRIT1 must exit from the SHUTDOWN state and the following operations must be done:

1. Write 0xCA in the register PM_TEST, register address 0xB2
2. Write 0x04 in the register TEST_SELECT, register address 0xA8
3. Write 0x00 in the register TEST_SELECT, register address 0xA8

Between steps 2 and 3, some microseconds are needed. This small delay is automatically made by the second SPI operation (considering an SPI clock of max 10 MHz).

With this sequence, the extra current is erased. The workaround must be repeated only when a voltage supply below 2.6 V is applied to SPIRIT1 from a no power condition. A reset operation made by the SRES command or by driving the SDN pin to put SPIRIT1 in SHUTDOWN does not cause the issue again.

1.3 With STack packet format, last byte missed from RX FIFO

1.3.1 Part number affected

SPIRIT1QTR.

1.3.2 Description

Using the STack packet format and no CRC field, the reading from RX FIFO to the last received byte, is not possible.

1.3.3 Workaround

By configuring the packet handler with at least one byte of CRC, the problem is solved. If the CRC is not required in the application, configure one byte of CRC in the receiver only, to read the payload correctly from RX FIFO.

1.4 Transmission issue after a reception with auto ACK

1.4.1 Part number affected

SPIRIT1QTR.

1.4.2 Description

The problem appears when the STack packet format and the automatic acknowledgment are used. If, during a receipt operation, no packet is correctly received and therefore no ACK packet is sent, at the next transmission of the packet with an ACK request (automatic acknowledgement must be disabled in this condition), the automatic reception phase is aborted.

1.4.3 Workaround

Making a dummy transmission (with PA off and the highest data rate) between the reception phase with no ACK packet transmitted and the desired transmission with ACK request.

1.5 Termination of CSMA algorithm in back off mode

1.5.1 Part number affected

SPIRIT1QTR.

1.5.2 Description

The maximum number of reached back offs does not indicate the end of the algorithm: another transmission is tried after this event.

1.5.3 Workaround

In order to correctly detect the event of the maximum number of reached back offs, the following steps are suggested:

1. Set the desired maximum number of back offs and add one
2. When the event of the maximum number of back offs occurs:
 - a. disable the CSMA
 - b. send the SABORT command

This allows the CSMA, in back off mode, to be ended in a controlled way

1.6 Failure of TX FIFO auto-reload during the automatic retransmission

1.6.1 Part number affected

SPIRIT1QTR.

1.6.2 Description

Under the following conditions:

- STack packet format
- Automatic re-transmission
- Maximum number of re-transmissions greater than 1

Occasionally, the third packet transmitted and the next consecutive packets have the payload shifted by two bytes.

1.6.3 Workaround

The situation can be detected and the corrupted re-transmissions avoided using the following procedure.

At the second RX phase waiting the ACK packet, if the ACK packet is not received correctly and the number of bytes into the TX FIFO is not 0, then the NMAX_RETX must be changed to 1 to abort the retransmission.

1.7 Sensitivity issue at low battery voltage

1.7.1 Part number affected

SPIRIT1QTR.

1.7.2 Description

The RX sensitivity performance of SPIRIT1 is degraded when the VBAT goes below 1.9 V. The sensitivity degrades proportional down to 1.8 V where the worst sensitivity performance is achieved. The following table shows an example of the impact of VBAT on sensitivity performances.

Table 3: Impact of VBAT on sensitivity performances

VBAT (mV)	Sensitivity (dBm)
1800	-82
1820	-85.5
1840	-96
1860	-104
1880	-105.5
1900	-105.5
1920	-105
1940	-105.5
1960	-105

Test conditions

Modulation: 2FSK, Datarate: 38.4 kbps, Frequency deviation: 20 kHz, Channel bandwidth: 100 kHz, and PER: 1 %.

1.7.3 Workaround

No workaround exists for this issue and customers are recommended to use VBAT \geq 2 V if the sensitivity degradation is not acceptable in their application.

1.8 Unwanted VCO calibration issue

1.8.1 Part number affected

SPIRIT1QTR.

1.8.2 Description

While performing a transmission with the calibration disabled (VCO_CALIBRATION bit set to 0 in register PROTOCOL[2]) a calibration procedure may be started anyway.

As a result the first bit of the transmission for about 50 μ s may be affected by the VCO instability during the unwanted calibration.

1.8.3 Workaround

In order to avoid such bit corruption the transmission can be delayed to wait for the completion of the possible unwanted calibration. To delay the transmission by 60 μ s, write 0x22 in the register 0xBC during the radio configuration.

2 Revision history

Table 4: Document revision history

Date	Revision	Changes
04-May-2012	1	Initial release
08-May-2012	2	Updated device information in <i>Table 1: "Device summary"</i>
05-Oct-2012	3	Updated device information in <i>Table 1: "Device summary"</i> Inserted <i>Section 1.1: "Automatic VCO calibration"</i> Minor text changes
06-Feb-2013	4	Added <i>Section 1.3: "With SStack packet format, last byte missed from RX FIFO"</i> , <i>Section 1.4: "Transmission issue after a reception with auto ACK"</i> , <i>Section 1.5: "Termination of CSMA algorithm in back off mode"</i> , <i>Section 1.6: "Failure of TX FIFO auto-reload during the automatic retransmission"</i> . Minor text changes
21-Mar-2013	5	Added <i>Section 1.2: "Extra current consumption after power-on"</i>
28-Jan-2015	6	Added <i>Section 1.7: "Sensitivity issue at low battery voltage"</i> . Minor text changes
07-Oct-2016	7	Removed all reference to preliminary engineering samples.

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