

STM32F76xxx and STM32F77xxx device errata

Applicability

This document applies to the part numbers of STM32F76xxx and STM32F77xxx devices listed in [Table 1](#) and their variants shown in [Table 2](#).

[Section 1](#) gives a summary and [Section 2](#) a description of / workaround for device errata, with respect to the device datasheet and reference manual RM0410.

Deviation of the real device behavior from the intended device behavior is considered to be a device limitation. Deviation of the description in the reference manual or the datasheet from the intended device behavior is considered to be a documentation erratum. The term “errata” applies both to limitations and documentation errata.

Table 1. Device summary

Reference	Part numbers
STM32F76xxx	STM32F765BG, STM32F765BI, STM32F765IG, STM32F765II, STM32F765NG, STM32F765NI, STM32F765VG, STM32F765VI, STM32F765ZG, STM32F765ZI, STM32F767BG, STM32F767BI, STM32F767IG, STM32F767II, STM32F767NG, STM32F767NI, STM32F767VG, STM32F767VI, STM32F767ZG, STM32F767ZI, STM32F768AI, STM32F769AG, STM32F769AI, STM32F769BG, STM32F769BI, STM32F769IG, STM32F769II, STM32F769NG, STM32F769NI
STM32F77xxx	STM32F777BI, STM32F777II, STM32F777NI, STM32F777VI, STM32F777ZI, STM32F778AI, STM32F779AI, STM32F779BI, STM32F779II, STM32F779NI

Table 2. Device variants

Reference	Silicon revision codes	
	Device marking ⁽¹⁾	REV_ID ⁽²⁾
STM32F76xxx, STM32F77xxx	A	0x1000
	Z	0x1001

1. Refer to the device data sheet for how to identify this code on different types of package.
2. REV_ID[15:0] bit field of DBGMCU_IDCODE register. Refer to the reference manual.

Contents

1	Summary of device errata	5
2	Description of device errata	8
2.1	Arm® 32-bit Cortex®-M7 core	8
2.1.1	Cortex®-M7 data corruption when using data cache configured in write-through	8
2.2	System	9
2.2.1	Internal noise impacting the ADC accuracy	9
2.2.2	Wakeup from Standby mode when the back-up SRAM regulator is enabled	10
2.2.3	Full JTAG configuration without NJTRST pin cannot be used	10
2.2.4	LSE high driving and low driving capability is not usable for TFBGA216 package under certain conditions	10
2.2.5	DTCM-RAM not accessible in read when the MCU is in Sleep mode (WFI/WFE)	11
2.2.6	PC13 signal transitions disturb LSE	11
2.3	FMC	11
2.3.1	Dummy read cycles inserted when reading synchronous memories	11
2.3.2	Wrong data read from a busy NAND memory	11
2.3.3	Spurious clock stoppage with continuous clock feature enabled	12
2.3.4	Data read might be corrupted when the write FIFO is disabled	12
2.4	QUADSPI	13
2.4.1	First nibble of data not written after a dummy phase	13
2.4.2	Wrong data from memory-mapped read after an indirect mode operation	13
2.4.3	Memory-mapped read operations may fail when timeout counter is enabled.	14
2.5	ADC	14
2.5.1	ADC sequencer modification during conversion	14
2.6	DAC	14
2.6.1	DMA underrun flag management	14
2.6.2	DMA request not automatically cleared by clearing DMAEN	15
2.7	DSI Host	15
2.7.1	When used over the DSI link, the tearing effect interrupt flag is set when an acknowledge trigger is received from the display	15

2.7.2	The time to activate the clock between HS transmissions is not calculated correctly	16
2.7.3	The immediate update procedure may fail	16
2.8	JPEG	17
2.8.1	False EOI marker is inserted after clearing the HDR bit	17
2.8.2	No DMA transfer complete generated at the end of the encoding process after clearing the HDR bit	17
2.8.3	JPEG FIFO might be corrupted	17
2.9	TIM	18
2.9.1	TIM12 input XOR function not available	18
2.10	LPTIM	18
2.10.1	MCU may remain stuck in LPTIM interrupt when entering Stop mode	18
2.11	RTC	19
2.11.1	RTC calendar registers are not locked properly	19
2.11.2	Setting GPIO properties of PC13 used as RTC_ALARM open-drain output	19
2.12	I2C	20
2.12.1	Wrong data sampling when data setup time ($t_{\text{SU, DAT}}$) is shorter than one I2C kernel clock period	20
2.12.2	Spurious bus error detection in master mode	21
2.12.3	10-bit master mode: new transfer cannot be launched if first part of the address is not acknowledged by the slave	21
2.12.4	Last-received byte loss in reload mode	21
2.13	USART	22
2.13.1	nRTS is active while RE or UE = 0	22
2.14	SPI/I2S	23
2.14.1	I2S slave in PCM short pulse mode sensitive to timing between WS and CK	23
2.14.2	BSY bit may stay high at the end of a data transfer in Slave mode	23
2.15	SDMMC	24
2.15.1	Wrong CCRCFAIL status after a response without CRC is received	24
2.15.2	MMC stream write of less than 8 bytes does not work correctly	24
2.16	BxCAN	25
2.16.1	BxCAN time triggered mode communication not supported	25
2.17	Ethernet	25
2.17.1	Incorrect layer 3 (L3) checksum is inserted in transmitted IPv6 packets without TCP, UDP or ICMP payloads	25

2.17.2	The Ethernet MAC processes invalid extension headers in the received IPv6 frames	26
2.17.3	MAC stuck in the Idle state on receiving the TxFIFO flush command exactly 1 clock cycle after a transmission completes	26
2.17.4	Transmit frame data corruption	27
2.17.5	Successive write operations to the same register might not be fully taken into account	27
2.17.6	Ethernet erroneous data received in RMI configuration	30
3	Revision history	31

1 Summary of device errata

The following table gives a quick references to all documented device errata of STM32F76xxx and STM32F77xxx and their status:

A = workaround available

N = no workaround available

P = partial workaround available

“-” = errata absent

Applicability of a workaround may depend on specific conditions of target application. Adoption of a workaround may cause restrictions to target application. Workaround for a limitation is deemed partial if it only reduces the rate of occurrence and/or consequences of the limitation, or if it is fully effective for only a subset of instances on the device or in only a subset of operating modes, of the function concerned.

Table 3. Summary of device errata

Function	Section	Limitation	Status	
			Rev. A	Rev. Z
Arm® 32-bit Cortex®-M7 core	2.1.1	Cortex®-M7 data corruption when using data cache configured in write-through	A	A
System	2.2.1	Internal noise impacting the ADC accuracy	A	A
	2.2.2	Wakeup from Standby mode when the back-up SRAM regulator is enabled	A	A
	2.2.3	Full JTAG configuration without NJTRST pin cannot be used	A	A
	2.2.4	LSE high driving and low driving capability is not usable for TFBGA216 package under certain conditions	A	-
	2.2.5	DTCM-RAM not accessible in read when the MCU is in Sleep mode (WFI/WFE)	A	-
	2.2.6	PC13 signal transitions disturb LSE	N	N
FMC	2.3.1	Dummy read cycles inserted when reading synchronous memories	N	N
	2.3.2	Wrong data read from a busy NAND memory	A	A
	2.3.3	Spurious clock stoppage with continuous clock feature enabled	A	A
	2.3.4	Data read might be corrupted when the write FIFO is disabled	A	A
QUADSPI	2.4.1	First nibble of data not written after a dummy phase	A	A
	2.4.2	Wrong data from memory-mapped read after an indirect mode operation	A	A
	2.4.3	Memory-mapped read operations may fail when timeout counter is enabled.	A	A
ADC	2.5.1	ADC sequencer modification during conversion	A	A

Table 3. Summary of device errata (continued)

Function	Section	Limitation	Status	
			Rev. A	Rev. Z
DAC	2.6.1	DMA underrun flag management	A	A
	2.6.2	DMA request not automatically cleared by clearing DMAEN	A	A
DSI Host	2.7.1	When used over the DSI link, the tearing effect interrupt flag is set when an acknowledge trigger is received from the display	A	A
	2.7.2	When used over the DSI link, the tearing effect interrupt flag is set when an acknowledge trigger is received from the display	A	A
	2.7.3	The immediate update procedure may fail	A	A
JPEG	2.8.1	False EOI marker is inserted after clearing the HDR bit	A	A
	2.8.2	No DMA transfer complete generated at the end of the encoding process after clearing the HDR bit	A	A
	2.8.3	JPEG FIFO might be corrupted	A	A
LPTIM	2.10.1	MCU may remain stuck in LPTIM interrupt when entering Stop mode	A	A
RTC	2.11.1	RTC calendar registers are not locked properly	A	A
I2C	2.12.1	Wrong data sampling when data setup time ($t_{SU, DAT}$) is shorter than one I2C kernel clock period	A	A
	2.12.2	Spurious bus error detection in master mode	A	A
	2.12.3	10-bit master mode: new transfer cannot be launched if first part of the address is not acknowledged by the slave	A	A
	2.12.4	Last-received byte loss in reload mode	A	A
USART	2.13.1	nRTS is active while RE or UE = 0	A	A
SPI/I2S	2.14.1	I2S slave in PCM short pulse mode sensitive to timing between WS and CK	A	A
	2.14.2	BSY bit may stay high at the end of a data transfer in Slave mode	A	A
SDMMC	2.15.1	Wrong CCRCFAIL status after a response without CRC is received	A	A
	2.15.2	MMC stream write of less than 8 bytes does not work correctly	A	A
BxCAN	2.16.1	BxCAN time triggered mode communication not supported	N	N
Ethernet	2.17.1	Incorrect layer 3 (L3) checksum is inserted in transmitted IPv6 packets without TCP, UDP or ICMP payloads	A	A
	2.17.2	The Ethernet MAC processes invalid extension headers in the received IPv6 frames	N	N
	2.17.3	MAC stuck in the Idle state on receiving the TxFIFO flush command exactly 1 clock cycle after a transmission completes	A	A
	2.17.4	Transmit frame data corruption	A	A
	2.17.5	Successive write operations to the same register might not be fully taken into account	A	A
	2.17.6	Ethernet erroneous data received in RMII configuration	A	-

The following table gives a quick reference to the documentation errata.

Table 4. Summary of device documentation errata

Function	Section	Documentation erratum
<i>System</i>	<i>2.2.1</i>	<i>Setting GPIO properties of PC13 used as RTC_ALARM open-drain output</i>
<i>TIM</i>	<i>2.9.1</i>	<i>TIM12 input XOR function not available</i>

2 Description of device errata

The following sections describe errata of the applicable devices with Arm^{®(a)} core and provide workarounds if available. They are grouped by device functions.



2.1 Arm[®] 32-bit Cortex[®]-M7 core

An errata notice of the STM32F76xxx and STM32F77xxx core is available from <http://infocenter.arm.com>.

All the described limitations are minor and related to the revision r1p0 of the Cortex[®]-M7 core. Refer to:

- Arm processor Cortex[®]-M7 (AT610) and Cortex[®]-M7 with FPU (AT611) software developer errata notice
- Arm embedded trace macrocell CoreSight ETM-M7 (TM975) software developer errata notice

[Table 5](#) summarizes these limitations and their implications on the behavior of STM32F76xxx and STM32F77xxx devices.

Table 5. Cortex[®]-M7 core limitations and impact on microcontroller behavior

Arm ID	Arm category	Impact on STM32F76xxx and STM32F77xxx devices
851031	Cat C	Minor
850725	Cat C	Minor
850724	Cat C	Minor

2.1.1 Cortex[®]-M7 data corruption when using data cache configured in write-through

Description

This limitation is registered under Arm[®] ID number 1259864 and classified into “Category A”.

If a particular sequence of stores and loads is performed to write-through memory, and some timing-based internal conditions are met, then a load might not get the last data stored to that address.

a. Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

This erratum only occurs if the loads and stores are to write-through memory. This is due to any of the following:

- The MPU has been programmed to set this address as write-through.
- The default memory map is being used and this address is write-through in that map.
- The memory is cacheable, and the CM7_CACR.FORCEWT bit is set.
- The memory is cacheable, shared, and the CM7_CACR.SIWT bit is set.

The following sequence is required for this erratum to occur:

1. The address of interest must be in the cache.
2. A write-through store to the same doubleword as the address of interest.
3. One of the following:
 - A linefill is started (to a different cacheline to the address of interest) that allocates to the same set as the address of interest.
 - An ECC error.
 - A cache maintenance operation without a following DSB.
4. A store to the address of interest.
5. A load from the address of interest.

If certain specific timing conditions are met, the load gets the data from the first store, or from what was in the cache at the start of the sequence instead of the data from the second store.

The effect of this erratum is that load operations can return incorrect data.

Workaround

There is no direct workaround for this erratum.

Where possible, Arm® recommends the use of the MPU to change the attributes on any write-through memory to write-back memory. If this is not possible, it might be necessary to disable the cache for sections of code that access write-through memory.

2.2 System

2.2.1 Internal noise impacting the ADC accuracy

Description

An internal noise generated on V_{DD} supplies and propagated internally may impact the ADC accuracy.

This noise is always active whatever the power mode of the MCU (Run or Sleep).

Workaround

To adapt the accuracy level to the application requirements, set one of the following options:

- Option1
Set the ADCDC1 bit in the PWR_CR register.
- Option2
Set the corresponding ADCxDC2 bit in the SYSCFG_PMC register.

Only one option can be set at a time.

For more details on option1 and option2 mechanisms, refer to AN4073

2.2.2 Wakeup from Standby mode when the back-up SRAM regulator is enabled

Description

When writing to the PWR_CSR1 register to enable or disable the back-up SRAM regulator, if the EIWUP bit is overwritten 0, the RTC wakeup event (alarm, RTC Tamper, RTC TimeStamp or RTC wakeup time) does not wake up the system from Standby mode.

Workaround

For each write access on the PWR_CSR1 register to enable or disable the back-up SRAM regulator, the EIWKUP bit must be set to 1 in order to enable a wakeup from Standby mode using RTC events.

2.2.3 Full JTAG configuration without NJTRST pin cannot be used

Description

When using the JTAG debug port in debug mode, the connection with the debugger is lost if the NJTRST pin (PB4) is used as a GPIO. Only the 4-wire JTAG port configuration is impacted.

Workaround

Use the SWD debug port instead of the full 4-wire JTAG port.

2.2.4 LSE high driving and low driving capability is not usable for TFBGA216 package under certain conditions

Description

On the TFBGA216 package when the LSE low driving capability or LSE high driving capability is selected (LSEDRV[1:0]=00 or LSEDRV[1:0]=11 in the RCC_BDCR register, respectively) for the LSE oscillator, the oscillation stability is impacted by toggling the MCU pins near the LSE input pin at relatively high-frequency.

The TFBGA216 pins impacting the LSE stability are: PF0, PF1, PI11 and PI12

Impact: under the above described conditions, intermittent LSE clock pulse losses (in low driving capability) or intermittent LSE clock pulse add-ons (in high driving capability) are possible.

Workaround

On the TFBGA216 package do not select the LSE high driving capability or the LSE low driving capability, and:

- Use the LSE medium high driving capability (LSEDRV[1:0]=01 in the RCC_BDCR register)
- Or the LSE medium low driving capability (LSEDRV[1:0]=10 in the RCC_BDCR register)

2.2.5 DTCM-RAM not accessible in read when the MCU is in Sleep mode (WFI/WFE)

Description

- The DTCM-RAM is not accessible in read during Sleep mode (when the CPU clock is gated). When a read access to the DTCM-RAM is performed by an AHB bus master (that are the DMAs) while the CPU is in sleep mode (CPU clock is gated), the data is not transmitted to the AHB bus and the AHB master reads 0x0000_0000.
- There is no issue when a write is performed to the DTCM-RAM while the CPU is in sleep mode, the data is correctly written in the DTCM-RAM.

Workaround

Use the AXI SRAM1 or SRAM2 for DMA data read transfers and use the AXI DTCM-RAM for DMA data write transfers in Sleep mode.

2.2.6 PC13 signal transitions disturb LSE

Description:

The PC13 port toggling disturbs the LSE clock. It may not be usable when LSE is used.

Workaround:

None.

2.3 FMC

2.3.1 Dummy read cycles inserted when reading synchronous memories

Description

When performing a burst read access from a synchronous memory, two dummy read accesses are performed at the end of the burst cycle whatever the type of burst access. The extra data values read are not used by the FMC and there is no functional failure.

Workaround

None.

2.3.2 Wrong data read from a busy NAND memory

Description

When a read command is issued to the NAND memory, the R/B signal gets activated upon the de-assertion of the chip select. If a read transaction is pending, the NAND controller might not detect the R/B signal (connected to NWAIT) previously asserted and sample a wrong data. This problem occurs only when the MEMSET timing is configured to 0x00 or when ATTHOLD timing is configured to 0x00 or 0x01.

Workaround

Either configure MEMSET timing to a value greater than 0x00 or ATTHOLD timing to a value greater than 0x01.

2.3.3 Spurious clock stoppage with continuous clock feature enabled**Description**

With the continuous clock feature enabled, the FMC_CLK clock may spuriously stop when:

- the FMC_CLK clock is divided by 2, and
- an FMC bank set as 32-bit is accessed with a byte access.

division ratio set to 2, the FMC_CLK clock may spuriously stop upon an

Note: *With static memories, a spuriously stopped clock can be restarted by issuing a synchronous transaction or any asynchronous transaction different from a byte access on 32-bit data bus width.*

Workaround

With the continuous clock feature enabled, do not set the FMC_CLK clock division ratio to 2 when accessing 32-bit asynchronous memories with byte access.

2.3.4 Data read might be corrupted when the write FIFO is disabled**Description**

When the write FIFO is disabled, the FIFO empty event is generated for every write access. During a write access, if a new read access occurs, the FMC grants the read access and waits till the FIFO gets empty. If another read access occurs in a very short window (one cycle the FIFO empty event), the returned data are corrupted. This issue occurs only when the write FIFO is disabled (the WFDIS bit in the FMC_BCR1 register is set).

Workaround

Enable the write FIFO.

2.4 QUADSPI

2.4.1 First nibble of data not written after a dummy phase

Description

The first nibble of data to be written to the external Flash memory is lost when the following conditions are met:

- The QUADSPI is used in the indirect write mode
- At least one dummy cycle is used

Workaround

Use alternate bytes instead of dummy phase to add latency between the address phase and the data phase. This works only if the number of dummy cycles to substitute corresponds to a multiple of eight bits of data.

Example:

- To substitute one dummy cycle, send one alternate byte (only possible in DDR mode with four data lines).
- To substitute two dummy cycles, send one alternate byte in SDR mode with four data lines.
- To substitute four dummy cycles, send two alternate bytes in SDR mode with four data lines, or one alternate byte in SDR mode with two data lines.
- To substitute eight dummy cycles, send one alternate byte in SDR mode with one data line.

2.4.2 Wrong data from memory-mapped read after an indirect mode operation

Description

The first memory-mapped read in indirect mode can yield wrong data if the QUADSPI peripheral enters memorymapped mode with bits ADDRESS[1:0] of the QUADSPI_AR register both set.

Workaround

Before entering memory-mapped mode, apply the following measure, depending on access mode:

- Indirect read mode: clear the QUADSPI_AR register then issue an abort request to stop reading and to clear the BUSY bit.
- Indirect write mode: clear the QUADSPI_AR register.

Caution: The QUADSPI_DR register must not be written after clearing the QUADSPI_AR register.

2.4.3 Memory-mapped read operations may fail when timeout counter is enabled.

Description

In memory-mapped mode with the timeout counter enabled (by setting the TCEN bit of the QUADSPI_CR register), the QUADSPI peripheral may hang and the memory-mapped read operations fail. This occurs if the timeout flag TOF is set at the same clock edge as a new memory-mapped read request..

Workaround

Disable the timeout counter. To raise the chip select, perform an abort at the end of each memory-mapped read operation.

2.5 ADC

2.5.1 ADC sequencer modification during conversion

Description

If an ADC conversion is started by software (writing the SWSTART bit), and if the ADC_SQRx or ADC_JSQRx registers are modified during the conversion, the current conversion is reset and the ADC does not restart a new conversion sequence automatically. If an ADC conversion is started by hardware trigger, this limitation does not apply. The ADC restarts a new conversion sequence automatically.

Workaround

When an ADC conversion sequence is started by software, a new conversion sequence can be restarted only by setting the SWSTART bit in the ADC_CR2 register.

2.6 DAC

2.6.1 DMA underrun flag management

Description

If the DMA is not fast enough to input the next digital data to the DAC, as a consequence, the same digital data is converted twice. In these conditions, the DMAUDR flag is set, which usually leads to disable the DMA data transfers. This is not the case: the DMA is not disabled by DMAUDR=1, and it keeps serving the DAC.

Workaround

To disable the DAC DMA stream, reset the EN bit (corresponding to the DAC DMA stream) in the DMA_SxCR register.

2.6.2 DMA request not automatically cleared by clearing DMAEN

Description

Upon an attempt to stop a DMA-to-DAC transfer, the DMA request is not automatically cleared by clearing the DAC channel bit of the DAC_CR register (DMAEN) or by disabling the DAC clock.

If the application stops the DAC operation while the DMA request is pending, the request remains pending while the DAC is reinitialized and restarted, with the risk that a spurious DMA request is serviced as soon as the DAC is enabled again.

Workaround

Apply the following sequence to stop the current DMA-to-DAC transfer and restart the DAC::

1. Check if DMAUDR bit is set in DAC_CR.
2. Clear the DAC channel DMAEN bit.
3. Disable the DAC clock.
4. Reconfigure the DAC, DMA and the triggers.
5. Restart the application.

2.7 DSI Host

2.7.1 When used over the DSI link, the tearing effect interrupt flag is set when an acknowledge trigger is received from the display

Description

In the adapted command mode, when the tearing effect mechanism is used over the DSI link, the tearing effect interrupt Flag (TEIF) of the DSI wrapper interrupt status register (DSI_WISR) is asserted when an acknowledge trigger is received from the display.

An acknowledge trigger can be received from the display:

- For each packet when the acknowledge request enable (ARE) bit of the DSI Host command mode configuration register (DSI_CMCR) is set,
- When a response is awaited from the display.

Workaround

Do not use the tearing effect over the link but use the dedicated TE pin.

When using the tearing effect over the link, do not use the tearing effect interrupt nor the automatic refresh mode, but launch the display refresh immediately after a set_tear_on or a set_scanline DCS command (as the display is driving the DSI link until the tearing effect occurs, the refresh is automatically stalled until the tearing effect).

2.7.2 The time to activate the clock between HS transmissions is not calculated correctly

Description

In the automatic clock lane control mode, the DSI Host can turn off the clock lane between two high-speed transmissions.

To do so, the DSI Host calculates the time required for the clock lane to change from high-speed to low-power and from low-power to high-speed.

These timings are configured by the HS2LP_TIME and LP2HS_TIME in the DSI Host clock lane timer configuration Register (DSI_CLTCR). The DSI Host is not calculating LP2HS_TIME + HS2LP_TIME but 2 x HS2LP_TIME instead.

Workaround

Configure HS2LP_TIME and LP2HS_TIME with the same value as the max between HS2LP_TIME and LP2HS_TIME.

As an example, if HS2LP_TIMER = 44 and LP2HS_TIME = 113 configure the register fields as follows:

- HS2LP_TIME = 113,
- LP2HS_TIME = 113.

2.7.3 The immediate update procedure may fail

Description

The immediate update procedure implies that both the update register (UR) and the enable (EN) bits of the DSI Host video shadow control register (DSI_VSCR) are initially cleared, and are set by the same instruction.

Because of a race condition between the two signals, this immediate update procedure may fail in few cases, leading the DSI Host to wait until the next frame end before updating the configuration.

Workaround

After an immediate update procedure, verify if the configuration is updated by reading the auto-cleared bit UR.

If the UR bit is not cleared, repeat the process by writing first 0x0000 then 0x0101 in DSIHOST_VSCR.

2.8 JPEG

2.8.1 False EOI marker is inserted after clearing the HDR bit

Description

An extra end of image (EOI) marker (0xFFD9) is written automatically into the output FIFO at the end of an encoding process with header processing. If the HDR mode is enabled and when the software clears the HDR bit at the end of the encoding process before making a software reset, an extra data (EOI marker = 0xFFD9) is inserted into the output FIFO. it implies that the extra data might be outputted from the FIFO and stored in a RAM

Workaround

The software must clear the EOC flag and perform a software reset before changing the HDR bit configuration in the JPEG codec configuration register 1 (JPEG_CONFR1).

2.8.2 No DMA transfer complete generated at the end of the encoding process after clearing the HDR bit

If the JPEG is configured as the DMA flow controller, the DMA might enter an infinite wait due to the fact that the JPEG does not generate the correct last data request for it.

The JPEG might not generate the correct last request if the following conditions are met:

- The software clears the HDR bit at the end of the encoding process
- The encoding process has the header processing enabled (the EOC flag is asserted and no software reset is performed)
- And the FIFO level is equal to the threshold.

Workaround

- The software must clear the EOC flag and perform a software reset before changing the HDR bit configuration in the JPEG codec configuration register 1 (JPEG_CONFR1).
- Or use the DMA as the flow controller

2.8.3 JPEG FIFO might be corrupted

Description

The JPEG can be accessed in a concurrent way with another peripherals (OTGFS, RNG, HASH, CRYPT and DCMI) on the same AHB bus. This might result in a dummy read/write access to the JPEG peripheral. as a consequence it can lead to a wrong data written into the input FIFO, or a data loss from the output FIFO.

Workaround

Avoid a concurrent access between the JPEG access and other peripherals on the same AHB bus.

2.9 TIM

2.9.1 TIM12 input XOR function not available

Description

The reference manual states incorrectly that for TIM12 a timer input XOR function is enabled with the TI1S bit of the TIM12_CR2 register. This feature is not available. Nevertheless the TIM12_CR2 register description is correct.

This is a documentation issue rather than a product limitation.

Workaround

No application workaround is required.

2.10 LPTIM

2.10.1 MCU may remain stuck in LPTIM interrupt when entering Stop mode

Description

This limitation occurs when disabling the low power timer (LPTIM).

When the firmware clears the LPTIM_CR.ENABLE bit within a small time window around one LPTIM interrupt occurrence, then the LPTIM interrupt signal used to wake up the MCU from Stop mode may be frozen in active state. Consequently, when trying to enter Stop mode, this limitation prevents the MCU from entering low-power mode and the firmware remains stuck in the LPTIM interrupt routine.

This limitation applies to all Stop modes and to all instances of the LPTIM. Note that the occurrence of this issue is very low.

Workaround

In order to disable a low power timer (LPTIMx) peripheral, do not clear its ENABLE bit in its respective LPTIMx_CR register. Instead, reset the whole LPTIMx peripheral via the RCC controller by setting and resetting its respective LPTIMxRST bit in the RCC_APBxRSTRz register.

2.11 RTC

2.11.1 RTC calendar registers are not locked properly

Description

When reading the calendar registers with BYPSHAD = 0, the RTC_TR and RTC_DR registers may not be locked after reading the RTC_SSR register. This happens if the read operation is initiated one APB clock period before the shadow registers are updated. This can result in a non-consistency of the three registers. Similarly, the RTC_DR register can be updated after reading the RTC_TR register instead of being locked.

Workaround

Apply one of the following measures:

1. Use BYPSHAD = 1 mode (bypass shadow registers), or
2. If BYPSHAD = 0, read the RTC_SSR register again after reading the RTC_SSR, RTC_TR, RTC_DR registers to confirm that RTC_SSR is still the same, otherwise read the values again.

2.11.2 Setting GPIO properties of PC13 used as RTC_ALARM open-drain output

Description

Some reference manual revisions may omit the information that the PC13 GPIO must be set as input when the RTC_OR register configures PC13 as open-drain output of the RTC_ALARM signal.

Note: Enabling the internal pull-up function through the PC13 GPIO settings allows sparing an external pull-up resistor.

This is a documentation issue rather than a product limitation.

Workaround

No application workaround is required provided that the described GPIO setting is respected.

2.12 I2C

2.12.1 Wrong data sampling when data setup time ($t_{\text{SU;DAT}}$) is shorter than one I2C kernel clock period

Description

The I²C-bus specification and user manual specify a minimum data setup time ($t_{\text{SU;DAT}}$) as:

- 250 ns in Standard mode
- 100 ns in Fast mode
- 50 ns in Fast mode Plus

The MCU does not correctly sample the I²C-bus SDA line when $t_{\text{SU;DAT}}$ is smaller than one I2C kernel clock (I²C-bus peripheral clock) period: the previous SDA value is sampled instead of the current one. This can result in a wrong receipt of slave address, data byte, or acknowledge bit.

Workaround

Increase the I2C kernel clock frequency to get I2C kernel clock period within the transmitter minimum data setup time. Alternatively, increase transmitter's minimum data setup time. If the transmitter setup time minimum value corresponds to the minimum value provided in the I2C-bus standard, the minimum I2CCLK frequencies are as follows:

- In Standard mode, if the transmitter minimum setup time is 250 ns, the I2CCLK frequency must be at least 4 MHz.
- In Fast mode, if the transmitter minimum setup time is 100 ns, the I2CCLK frequency must be at least 10 MHz.
- In Fast-mode Plus, if the transmitter minimum setup time is 50 ns, the I2CCLK frequency must be at least 20 MHz.

2.12.2 Spurious bus error detection in master mode

Description

In master mode, a bus error can be detected spuriously, with the consequence of setting the BERR flag of the I2C_SR register and generating bus error interrupt if such interrupt is enabled. Detection of bus error has no effect on the I²C-bus transfer in master mode and any such transfer continues normally.

Workaround

If a bus error interrupt is generated in master mode, the BERR flag must be cleared by software. No other action is required and the ongoing transfer can be handled normally.

2.12.3 10-bit master mode: new transfer cannot be launched if first part of the address is not acknowledged by the slave

Description

An I²C-bus master generates STOP condition upon non-acknowledge of I²C address that it sends. This applies to 7-bit address as well as to each byte of 10-bit address.

When the MCU set as I²C-bus master transmits a 10-bit address of which the first byte (5-bit header + 2 MSBs of the address + direction bit) is not acknowledged, the MCU duly generates STOP condition but it then cannot start any new I²C-bus transfer. In this spurious state, the NACKF flag of the I2C_ISR register and the START bit of the I2C_CR2 register are both set, while the START bit should normally be cleared.

Workaround

In 10-bit-address master mode, if both NACKF flag and START bit get simultaneously set, proceed as follows:

1. Wait for the STOP condition detection (STOPF = 1 in I2C_ISR register).
2. Disable the I2C peripheral.
3. Wait for a minimum of three APB cycles.
4. Enable the I2C peripheral again.

2.12.4 Last-received byte loss in reload mode

Description

If in master receiver mode or slave receive mode with SBC = 1 the following conditions are all met:

- I²C-bus stretching is enabled (NOSTRETCH = 0)
- RELOAD bit of the I2C_CR2 register is set
- NBYTES bitfield of the I2C_CR2 register is set to N greater than 1
- byte N is received on the I²C-bus, raising the TCR flag
- N - 1 byte is not yet read out from the data register at the instant TCR is raised,

then the SCL line is pulled low (I²C-bus clock stretching) and the transfer of the byte N from the shift register to the data register inhibited until the byte N-1 is read and NBYTES bitfield reloaded with a new value, the latter of which also clears the TCR flag. As a consequence,

the software cannot get the byte N and use its content before setting the new value into the NBYTES field.

For I2C instances with independent clock, the last-received data is definitively lost (never transferred from the shift register to the data register) if the data N - 1 is read within four APB clock cycles preceding the receipt of the last data bit of byte N and thus the TCR flag raising. Refer to the product reference manual or datasheet for the I2C implementation table.

Workaround

- In master mode or in slave mode with SBC = 1, use the reload mode with NBYTES = 1.
- In master receiver mode, if the number of bytes to transfer is greater than 255 bytes, do not use the reload mode. Instead, split the transfer into sections not exceeding 255 bytes and separate them with repeated START conditions.
- Make sure, for example through the use of DMA, that the byte N - 1 is always read before the TCR flag is raised. Specifically for I2C instances with independent clock, make sure that it is always read earlier than four APB clock cycles before the receipt of the last data bit of byte N and thus the TCR flag raising.

The last workaround in the list must be evaluated carefully for each application as the timing depends on factors such as the bus speed, interrupt management, software processing latencies, and DMA channel priority.

2.13 USART

2.13.1 nRTS is active while RE or UE = 0

Description

The nRTS line is driven low as soon as the RTSE bit is set, even if the USART is disabled (UE = 0) or the receiver is disabled (RE = 0), that is, not ready to receive data.

Workaround

Upon setting the UE and RE bits, configure the I/O used for nRTS into alternate function.

2.14 SPI/I2S

2.14.1 I2S slave in PCM short pulse mode sensitive to timing between WS and CK

Description

When the device is configured in I2S slave PCM short frame mode (I2SMOD = 1, I2SCFG[1:0] = 00 or 01, I2SSTD[1:0] = 11, PCMSYNC = 0), with the asynchronous start disabled (ASTREN = 0), then if the master does not respect the WS hold time versus clock, the data transmitted and received by the device get desynchronized (shifted by one bit). This results in discarding two frames instead of one, irrespectively of the clock polarity.

Workaround

Use legacy mode (ASTERN = 1), while ensuring a perfect synchronization between the master and the slave.

2.14.2 BSY bit may stay high at the end of a data transfer in Slave mode

Description

The BSY flag may sporadically remain high at the end of a data transfer in slave mode. This occurs upon coincidence of internal CPU clock and external SCK clock provided by master.

In such an event, if the software only relies on BSY flag to detect the end of SPI slave data transaction (for example to enter low-power mode or to change data line direction in half-duplex bidirectional mode), the detection fails.

As a conclusion, the BSY flag is unreliable for detecting the end of data transactions.

Workaround

Depending on SPI operating mode, use the following means for detecting the end of transaction:

- When NSS hardware management is applied and NSS signal is provided by master, use NSS flag.
- In SPI receiving mode, use the corresponding RXNE event flag.
- In SPI transmit-only mode, use the BSY flag in conjunction with a timeout expiry event. Set the timeout such as to exceed the expected duration of the last data frame and start it upon TXE event that occurs with the second bit of the last data frame. The end of the transaction corresponds to either the BSY flag becoming low or the timeout expiry, whichever happens first.

Prefer one of the first two measures to the third as they are simpler and less constraining. Alternatively, apply the following sequence to ensure reliable operation of the BSY flag in SPI transmit mode:

1. Write last data to data register
2. Poll the TXE flag until it becomes high, which occurs with the second bit of the data frame transfer
3. Disable SPI by clearing the SPE bit mandatorily before the end of the frame transfer
4. Poll the BSY bit until it becomes low, which signals the end of transfer

Note: The alternative method can only be used with relatively fast CPU speeds versus relatively slow SPI clocks or/and long last data frames. The faster is the software execution, the shorter can be the duration of the last data frame.

2.15 SDMMC

2.15.1 Wrong CCRCFAIL status after a response without CRC is received

Description

The CRC is calculated even if the response to a command does not contain any CRC field. As a consequence, after the SDIO command IO_SEND_OP_COND (CMD5) is sent, the CCRCFAIL bit of the SDIO_STA register is set.

Workaround

The CCRCFAIL bit in the SDIO_STA register must be ignored by the software. CCRCFAIL must be cleared by setting the CCRCFAILC bit in the SDIO_ICR register after reception of the response to the CMD5 command.

2.15.2 MMC stream write of less than 8 bytes does not work correctly

Description

When the SDMMC host starts a stream write (WRITE_DAT_UNTIL_STOP CMD20), the number of bytes to transfer is not known by the card.

The card writes data from the host until a STOP_TRANSMISSION (CMD12) command is received.

Use the WAITRESP value equal to "00" to indicate to SDMMC CPSM that no response is expected.

The WAITPEND bit 9 of the SDMMC_CMD register is set to synchronize the sending of the STOP_TRANSMISSION (CMD12) command with the data flow.

When WAITPEND is set, the transmission of this command stays pending until 50 data bits (including the Stop bit) remain to transmit.

For a stream write of less than 8 bytes, the STOP_TRANSMISSION (CMD12) command must be started before the data transfer starts. Instead of this, the data write and the command sending are started simultaneously.

It implies that when less than 8 bytes must be transmitted, (8 - DATALENGTH) bytes are programmed to 0xFF in the card after the last byte programmed (where DATALENGTH is the number of data bytes to be transferred).

Workaround

Do not use stream write WRITE_DAT_UNTIL_STOP (CMD20) with a DATALENGTH less than 8 bytes. Use set block length (SET_BLOCKLEN: CMD16) followed by the single block write command (WRITE_BLOCK_CMD24) instead of the stream write (CMD20) with the desired block length.

2.16 BxCAN

2.16.1 BxCAN time triggered mode communication not supported

Description

The time triggered communication mode described in the reference manual is not supported. As a result the time stamp values are not available. The TTCM bit of the CAN-MCR register must be kept cleared (time-triggered communication mode disabled).

Workaround

None.

2.17 Ethernet

2.17.1 Incorrect layer 3 (L3) checksum is inserted in transmitted IPv6 packets without TCP, UDP or ICMP payloads

Description

The application provides the per-frame control to instruct the MAC to insert the L3 checksums for TCP, UDP and ICMP packets. When an automatic checksum insertion is enabled and the input packet is an IPv6 packet without the TCP, UDP or ICMP payload, then the MAC may incorrectly insert a checksum into the packet. For IPv6 packets without a TCP, UDP or ICMP payload, the MAC core considers the next header (NH) field as the extension header and continues to parse the extension header. Sometimes, the payload data in such packets matches the NH field for TCP, UDP or ICMP and, as a result, the MAC core inserts a checksum.

Workaround

When the IPv6 packets have a TCP, UDP or ICMP payload, enable checksum insertion for transmit frames, or bypass checksum insertion by using the CIC (checksum insertion control) bits in TDES0 (bits 23:22).

2.17.2 The Ethernet MAC processes invalid extension headers in the received IPv6 frames

Description

In the IPv6 frames, there can be zero or some extension headers preceding the actual IP payload. The Ethernet MAC processes the following extension headers defined in the IPv6 protocol: hop-by-hop options header, routing header and destination options header. All the extension headers, except the hop-by-hop extension header, can be present multiple times and in any order before the actual IP payload. The hop-by-hop extension header, if present, has to come immediately after the IPv6's main header.

The Ethernet MAC processes all (valid or invalid) extension headers including the hop-by-hop extension headers that are present after the first extension header. For this reason, the GMAC core accepts IPv6 frames with invalid hop-by-hop extension headers. As a consequence, it accepts any IP payload as valid IPv6 frames with TCP, UDP or ICMP payload, and then incorrectly update the receive status of the corresponding frame.

Workaround

None.

2.17.3 MAC stuck in the Idle state on receiving the TxFIFO flush command exactly 1 clock cycle after a transmission completes

Description

When the software issues a TxFIFO flush command, the transfer of frame data stops (even in the middle of a frame transfer). The TxFIFO read controller goes into the idle state (TFRS=00 in ETH_MACDBGR) and then resumes its normal operation.

However, if the TxFIFO read controller receives the TxFIFO flush command exactly one clock cycle after receiving the status from the MAC, the controller remains stuck in the Idle state and stops transmitting frames from the TxFIFO. The system can recover from this state only with a reset (e.g. a soft reset).

Workaround

Do not use the TxFIFO flush feature.

If TxFIFO flush is really needed, wait until the TxFIFO is empty prior to using the TxFIFO flush command.

2.17.4 Transmit frame data corruption

The frame data is corrupted when the TxFIFO is repeatedly transitioning from non empty to empty and then back to non empty.

Description

The frame data may get corrupted when the TxFIFO is repeatedly transitioning from non empty to empty for a very short period, and then from empty to non empty, without causing an underflow.

This transitioning from non empty to empty and back to non empty happens when the rate at which the data is being written to the TxFIFO is almost equal to or a little less than the rate at which the data is being read.

This corruption cannot be detected by the receiver when the CRC is inserted by the MAC, as the corrupted data is used for the CRC computation.

Workaround

Use the Store-and-Forward mode: TSF=1 (bit 21 in ETH_DMAOMR). In this mode, the data is transmitted only when the whole packet is available in the TxFIFO.

2.17.5 Successive write operations to the same register might not be fully taken into account

Description

A write to a register might not be fully taken into account if a previous write to the same register is performed within a time period of four TX_CLK/RX_CLK clock cycles. When this error occurs, reading the register returns the most recently written value, but the Ethernet MAC continues to operate as if the latest write operation never occurred.

See [Table 6: Impacted registers and bits](#) for the registers and bits impacted by this limitation.

Table 6. Impacted registers and bits

Register name	Bit number	Bit name
DMA registers		
ETH_DMABMR	7	EDFE
ETH_DMAOMR	26	DTCEFD
	25	RSF
	20	FTF
	7	FEF
	6	FUGF
	4:3	RTC
GMAC registers		

Table 6. Impacted registers and bits (continued)

Register name	Bit number	Bit name
ETH_MACCR	25	CSTF
	23	WD
	22	JD
	19:17	IFG
	16	CSD
	14	FES
	13	ROD
	12	LM
	11	DM
	10	IPCO
	9	RD
	7	APCS
	6:5	BL
	4	DC
	3	TE
2	RE	
ETH_MACFFR	-	MAC frame filter register
ETH_MACHTHR	31:0	Hash Table High Register
ETH_MACHTLR	31:0	Hash Table Low Register
ETH_MACFCR	31:16	PT
	7	ZQPD
	5:4	PLT
	3	UPFD
	2	RFCE
	1	TFCE
	0	FCB/BPA
ETH_MACVLANTR	16	VLANTC
	15:0	VLANTI
ETH_MACRWUFR	-	all remote wakeup registers
ETH_MACPMTCSR	31	WFFRPR
	9	GU
	2	WFE
	1	MPE
	0	PD
ETH_MACA0HR	-	MAC address 0 high register

Table 6. Impacted registers and bits (continued)

Register name	Bit number	Bit name
ETH_MACA0LR	-	MAC address 0 low register
ETH_MACA1HR	-	MAC address 1 high register
ETH_MACA1LR	-	MAC address 1 low register
ETH_MACA2HR	-	MAC address 2 high register
ETH_MACA2LR	-	MAC address 2 low register
ETH_MACA3HR	-	MAC address 3 high register
ETH_MACA3LR	-	MAC address 3 low register
IEEE 1588 time stamp registers		
ETH_PTPTSCR	18	TSPFFMAE
	17:16	TSCNT
	15	TSSMRME
	14	TSSEME
	13	TSSIPV4FE
	12	TSSIPV6FE
	11	TSSPTPOEFE
	10	TSPTPPSV2E
	9	TSSSR
	8	TSSARFE
	5	TSARU
	3	TSSTU
	2	TSSTI
	1	TSFCU
0	TSE	

Workarounds

Two workarounds can be applicable:

- Ensure a delay of four TX_CLK/RX_CLK clock cycles between the successive write operations to the same register.
- Make several successive write operations without delay, then read the register when all the operations are complete, and finally reprogram it after a delay of four TX_CLK/RX_CLK clock cycles.

2.17.6 Ethernet erroneous data received in RMIi configuration

Description

- In the reduced media-independent interface (RMIi) configuration, an erroneous data might be received on the RXD0 signal (PC4). The bit received might flip from 0 to 1 and lead to a received frame with a CRC error. The ETH_MMCRFCECR register increments each time a frame is received. This is related to internal timing constraints on the reference clock generated after the sync divider.
- Using the RMIi reference clock of 50 MHz, the error is seen for both cases:
 - 100-Mbit/s operating rate (sync divider = div2)
 - 10-Mbit/s operating rate (sync divider = div20)
- The issue is not present in the MII mode with a direct reference clock from the pad (no division).

Workaround

Using the MAC management counters, the software can identify if the RMIi is correctly initialized or not.

- If too many errors are detected during the initialization (received frames with CRC error counter), reset the RMIi interface and restart the monitoring.
- If a good frame is received after initialization (received good unicast frame counter register), the RMIi is correctly initialized and stop the monitoring.

3 Revision history

Table 7. Document revision history

Date	Revision	Changes
18-Feb-2016	1	Initial release.
21-Apr-2016	2	Added QUADSPI peripheral limitation: Section 2.4.1: First nibble of data not written after a dummy phase . Added system limitation: Section 2.2.4: LSE high driving and low driving capability is not usable for TFBGA216 package under certain conditions .
29-Sep-2016	3	Added system limitation: Section 2.2.5: DTCM-RAM not accessible in read when the MCU is in Sleep mode (WFI/WFE) . Added ethernet limitation: Section 2.17.6: Ethernet erroneous data received in RMII configuration . Added JPEG limitations: – Section 2.8.1: False EOI marker is inserted after clearing the HDR bit . – Section 2.8.2: No DMA transfer complete generated at the end of the encoding process after clearing the HDR bit . Added I2C limitation: Section 2.12.3: 10-bit master mode: new transfer cannot be launched if first part of the address is not acknowledged by the slave . Removed USART limitations: – Start bit detected too soon when sampling for NACK signal from the smartcard. – Break request can prevent the Transmission Complete flag (TC) from being set. Updated Table 1: Device summary adding STM32F765xx devices.
21-Oct-2016	4	Added revision Z: – Updated Table 1: Device summary . – Updated Table 3: Summary of device errata with two system limitations and one ethernet limitation marked as 'fixed'.

Table 7. Document revision history (continued)

Date	Revision	Changes
18-Jul-2018	5	<p>FMC limitation:</p> <ul style="list-style-type: none"> – Added Section 2.3.4: Data read might be corrupted when the write FIFO is disabled. <p>QUADSPI limitation:</p> <ul style="list-style-type: none"> – Updated Section 2.4.1: First nibble of data not written after a dummy phase. – Added Section 2.4.2: Wrong data from memory-mapped read after an indirect mode operation. – Added Section 2.4.3: Memory-mapped read operations may fail when timeout counter is enabled.. <p>JPEG limitation:</p> <ul style="list-style-type: none"> Added Section 2.8.3: JPEG FIFO might be corrupted. <p>I2S/SPI limitations:</p> <ul style="list-style-type: none"> – Moved Section 2.14.2: BSY bit may stay high at the end of a data transfer in Slave mode from I2C limitation to I2S/SPI limitation. – Updated Section 2.14.1: I2S slave in PCM short pulse mode sensitive to timing between WS and CK. <p>RTC limitations:</p> <ul style="list-style-type: none"> – Added Section 2.11.1: RTC calendar registers are not locked properly. <p>I2C limitations:</p> <ul style="list-style-type: none"> – Added Section 2.12.4: Last-received byte loss in reload mode. – Updated Section 2.12.1: Wrong data sampling when data setup time ($t_{SU,DAT}$) is shorter than one I2C kernel clock period. <p>ETHERNET limitation:</p> <ul style="list-style-type: none"> – Updated Section 2.17.6: Ethernet erroneous data received in RMII configuration.
17-Jul-2019	6	<p>Added:</p> <ul style="list-style-type: none"> – Section 2.1.1: Cortex[®]-M7 data corruption when using data cache configured in write-through. – Section 2.2.3: Full JTAG configuration without NJTRST pin cannot be used.
09-Mar-2021	7	<p>Added:</p> <ul style="list-style-type: none"> – Section 2.2.6: PC13 signal transitions disturb LSE. – Section 2.9.1: TIM12 input XOR function not available. – Section 2.11.2: Setting GPIO properties of PC13 used as RTC_ALARM open-drain output.

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