STM32WB5MMG

STM32WB5MMG module product errata

Applicability

This document applies to the STM32WB5MMG module product.

It gives a summary and a description of module-specific errata, with respect to the module product datasheet DS13252 available on www.st.com.

Deviation of the real module product properties from the intended module product properties is considered to be a module product limitation. Deviation of the description in the module product datasheet from the intended module product properties is considered to be a documentation erratum. The terms *"erratum"* and *"errata"* apply both to limitations and documentation errata.

The module integrates the STM32WB55VG microcontroller with Arm® core. For errata of the microcontroller device, refer to its errata sheet ES0394 on www.st.com.

Note: *Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.*

arm

Table 1. Module variants

Reference	Module variant
STM32WB5MMG	Y
	X

ES0525 - Rev 3 - February 2023
For further information contact your local STMicroelectronics sales office.

www.st.com

1 Summary of module-specific errata

The following table gives a quick reference to the documentation errata.

Table 2. Summary of module-specific documentation errata

Function	Section	Documentation erratum
System	2.1.1	LSE frequency shift
	2.1.2	PB0 and PB1 swapped in datasheet pinning

2 Description of module-specific errata

The following sections describe module-specific errata of the module product.

2.1 System

2.1.1 LSE frequency shift

Description

Some versions of the datasheet omit the information that the LSE frequency of the microcontroller mounted on the module is shifted to 32774 Hz (+183ppm), versus the nominal 32768 Hz. The application software must reflect this module characteristic if the on-chip peripherals such as RTC and BLE use LSE as a clock reference.

This is a documentation issue rather than a product limitation.

Workaround

No application workaround is applicable provided that the application already takes the frequency shift into account.

2.1.2 PB0 and PB1 swapped in datasheet pinning

Description

In some datasheet versions pinning has incorrect assignments of PB0 and PB1. The correct assignment is PB1 on 43 and PB0 on 44.

Workaround

None.

Assignment in CubeMx is correct.

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Revision history

Table 3. Document revision history

Date	Version	Changes
09-Mar-2020	1	Initial release.
16-Dec-2021	2	Added documentation erratum LSE frequency shift.
24-Feb-2023	3	Added: • Section Important security notice • Documentation erratum Section 2.1.2 PB0 and PB1 swapped in datasheet pinning

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IMPORTANT NOTICE – READ CAREFULLY