ST25DV04K, ST25DV16K and ST25DV64K device limitations

Silicon identification

The ST25DV-I2C series is a dynamic NFC/RFID tag ICs with 4, 16 or 64-Kbit EEPROM and Fast transfer mode capability.

Table 1 shows the full list of impacted part numbers (hereinafter referred to as ST25DVxxK). These parts are identified physically by their marking or directly in the application by reading the I²C product revision byte.

Table 1. Device summary

References	Package	Ordering code	IC reference	Product code
ST25DV04K	SO8N	ST25DV04K-IER6S3	24h	24h
		ST25DV04K-IER8S3		
	TSS0P8	ST25DV04K-IER6T3		
		ST25DV04K-IER8T3		
	UFDFPN8	ST25DV04K-IER6C3		
		ST25DV04K-IER8C3		
	UFDFPN12	ST25DV04K-JFR6D3		25h
		ST25DV04K-JFR8D3		
	Unsawn wafer	ST25DV04K-JFR6U3		
	WLCSP	ST25DV04K-JFR6L3		
ST25DV16K	SO8N	ST25DV16K-IER6S3	26h	26h
		ST25DV16K-IER8S3		
	TSS0P8	ST25DV16K-IER6T3		
		ST25DV16K-IER8T3		
	UFDFPN12	ST25DV16K-JFR6D3		27h
		ST25DV16KC-JFR8D3		
ST25DV64K	SO8N	ST25DV64K-IER6S3	26h	26h
		ST25DV64K-IER8S3		
	TSS0P8	ST25DV64KC-IER6T3		
		ST25DV64KC-IER8T3		
	UFDFPN12	ST25DV64K-JFR6D3		27h
		ST25DV64K-JFR8D3		

The IC reference (IC_REF register) is read from I²C at address 0017h (device select code E2 = 1) or from RF by issuing a *Get System Information* or an *Extended Get System Information* command.

The product code is read from I²C at address 001Dh or from RF by issuing an *Inventory*, a *Get System Information* or an *Extended Get System Information* command and is the third byte of the UID (after E0h 02h).

The product revision (IC_REV register) is read from I²C at address 0020h (device select code E2 = 1).

1 Limitations

Table 2 gives quick references to all documented device limitations of ST25DVxxK and their status:

- A = workaround available
- N = no workaround available
- P = partial workaround available
- '-' = fixed

Applicability of a workaround depends on specific conditions of the target application. Adoption of a workaround may cause restrictions to the target application. Workaround for a limitation is deemed partial if it only reduces the rate of occurrence and/or consequences of the limitation, or if it is fully effective for only a subset of instances on the device or in only a subset of operating modes, of the concerned function.

Table 2. Summary of silicon limitations

Links to silicon limitations		Workaround(1)	Workaround(2)
RF commands limitations	Fast extended read single block RF command not functional for block addresses above 255 (00FFh)	A	A
	Manage GPO command can affect GPO pin state of all ST25DV-I2C tags present in the RF field	A	A
	Write message and fast write message commands can affect GPO pin state of other ST25DV-I2C tags present in the RF field when address_flag is set	A	A
	Write message and fast write message commands can overwrite mailbox content of ST25DV-I2C tags present in the RF field	A	A
Tearing robustness limitations	Wrong memory address potentially overwritten after tearing during an RF write in EEPROM when V_{CC} is present	A	-
	Wrong memory address potentially overwritten after V_{CC} off during an I^2C write in EEPROM when RF field is present	N	-
	Potential communication lock after tearing during an RF write in EEPROM when V_{CC} is present	N	-
	Potential communication lock after V_{CC} off during an I^2C write in EEPROM when RF field is present	N	-
	RF access to EEPROM potentially locked after tearing during an RF read in EEPROM when V_{CC} is present	A	-
I^2C RF arbitration limitations	I^2C busy state not released after an I^2C error	A	-
	RF response corrupted during I^2C programming cycle when I^2C is busy	N	-
Power supply	Potential RF and I^2C lock if V_{CC} gets disconnected then reconnected when RF field is present	A	A
Communication limitation	Communication limitation on a marginal portion of production parts (sub-carrier frequency drift)	A	A

Links to silicon limitations		Workaround(1)	Workaround(2)
Fast transfer mode limitation	Fast transfer mode watchdog not started correctly after an I²C write message in mailbox	A	A
	RF_PUT_MSG bit wrongly cleared after I²C reading MB_LEN_Dyn if message is 256 bytes long	A	A

1. *For product code 25h and 27h*
2. *For product code 24h and 26h*

1.1 RF commands limitations

1.1.1 Fast extended read single block RF command not functional for block addresses above 255 (00FFh)

Impacetd devices: All ST25DVxxK with IC Reference 26h

Description

When a fast extended read single block RF command is received with a Block Number field value above 255 (00FFh), the ST25DV16K and ST25DV64K return a wrong block value.

The most significant byte of the requested block number of the fast extended read single block command is ignored, and the ST25DV16K and ST25DV64K return the value of the block number pointed by the least significant byte of the requested block number.

Workaround

The same functionality of the fast extended read single block command can be achieved using the fast extended read multiple block command and requesting only one block. To achieve this, set the number of blocks field of the fast extended read multiple block command to 0000h.

1.1.2 Manage GPO command can affect GPO pin state of all ST25DV-I2C tags present in the RF field

Impacetd devices: All ST25DVxxK

Description

The Manage GPO command received by a tag, if correctly formatted, is always executed by the tag.

This means that the command can be executed (but is not answered) in the following incorrect cases:

- When command is sent in addressed mode and UID in the command does not match
- When command is sent in selected mode and tag is not in selected state
- When tag is in quiet state

As a consequence, if RF_GPO_USER or RF_GPO_INTERRUPT interrupts are enabled and if GPO output is enabled too (GPO_EN bit set to 1), the GPO pin state of the tag can be affected by any correctly formatted Manage GPO command destined to another tag.

Workaround

To avoid undesired state change on GPO pin, the reader can enable GPO output per tag, only on demand.

For this, the GPO_EN bit can be used. The tag must have the GPO output disabled by default (GPO_EN set to 0). The reader enables GPO output (GPO_EN set to 1) before sending a Manage GPO command to this tag. After Manage GPO command is sent, the GPO output is disabled again to avoid any undesired GPO state change due to any Manage GPO commands sent to another tag.

To change value of the GPO_EN bit, reader must first open the configuration security session by presenting the password 0, and then use the Write Configuration command to write in the GPO system register.

Workaround for ST25DV-I2C devices with CMOS GPO pin only (product codes 25h and 27h)

For product versions with CMOS GPO pin, it is possible to use energy harvesting to control the GPO output of the tag, by controlling its power supply (VDCG pin).

For this, the VDCG pin is connected to the V_EH pin. GPO output can then be controlled by enabling or disabling energy harvesting (by writing EH_EN bit in EH_CTRL_Dyn register).

The EH_EN bit of EH_CTRL_Dyn register then acts as output enable/disable bit, just like the GPO_EN bit would do, but with the advantage of not having to present the configuration password before updating it.

1.1.3 Write message and fast write message commands can affect GPO pin state of other ST25DV-I2C tags present in the RF field when address_flag is set

Impacetd devices: All ST25DVxxK

Description

A write message, or fast write message command received by a tag, if correctly formatted, is always executed by the tag and can affect the GPO pin state if the address_flag set to 1, even if the UID does not match.

The GPO pin state of the tag can be affected by a correctly formatted write message or fast write message command destined to another tag if the following conditions are met:

- Write message or fast write message is sent with address_flag set to 1 and non-matching UID
- RF_PUT_MSG interruption is enabled
- GPO output is enabled (GPO_EN bit set to 1)
- mailbox is enabled (MB_MODE set to 1 and MB_EN set to 1)

Workaround

To avoid undesired state change on GPO pin when receiving the write message command, the reader can enable mailbox only on demand. It is the recommended way of using fast transfer mode.

For this, the MB_EN bit (bit 0 of MB_CRTL_Dyn register) can be used. The tag must have the mailbox disabled by default (MB_EN set to 0), and enabled only when fast transfer mode exchange session is ongoing between this tag and the reader.

If this method cannot be put in place, then the reader can temporarily enable/disable the GPO output, as described in the workaround of Section 1.1.2 Manage GPO command can affect GPO pin state of all ST25DV-I2C tags present in the RF field.

1.1.4 Write message and fast write message commands can overwrite mailbox content of ST25DV-I2C tags present in the RF field

Impacetd devices: All ST25DVxxK

Description

A write message, or fast write message command received by a tag, if correctly formatted is always executed by the tag. This means that the command can be executed (but not answered) in the following incorrect cases:

- When command is sent in address mode and UID in the command does not match
- When command is sent in selected mode and tag is not in selected state
- When tag is in quiet state

As a consequence, content of the mailbox can be overwritten by a correctly formatted write message or fast write message command destined to another tag if the following conditions are met:

- mailbox is enabled (MB_MODE set to 1 and MB_EN set to 1)
- a message from RF is already present in the mailbox

If mailbox is enabled and no message is present, or if message present is from I²C host, the content of mailbox is not modified.

Workaround

To avoid undesired corruption of the mailbox content when receiving the write message command, the reader can enable mailbox only on demand. It is the recommended way of using fast transfer mode.

For this, the MB_EN bit (bit 0 of MB_CRTL_Dyn register) can be use. The tag must have the mailbox disabled by default (MB_EN set to 0), and enabled only when fast transfer mode exchange session is ongoing between this tag and the reader.

1.2 Tearing robustness limitations

1.2.1 Wrong memory address potentially overwritten after tearing during an RF write in EEPROM when V_{CC} is present

Impacted devices: All ST25DVxxK devices with product code 25h and 27h

Description

If the following conditions are met:

- V_{CC} is powered during the complete operation
- RF field is lost during the EEPROM programming phase of any RF write command to EEPROM
- next RF command is any command that reads data from the EEPROM

Then, depending on the tearing timing in the programming phase, the memory content can potentially be overwritten at block address pointed by the RF read command that follows the tearing.

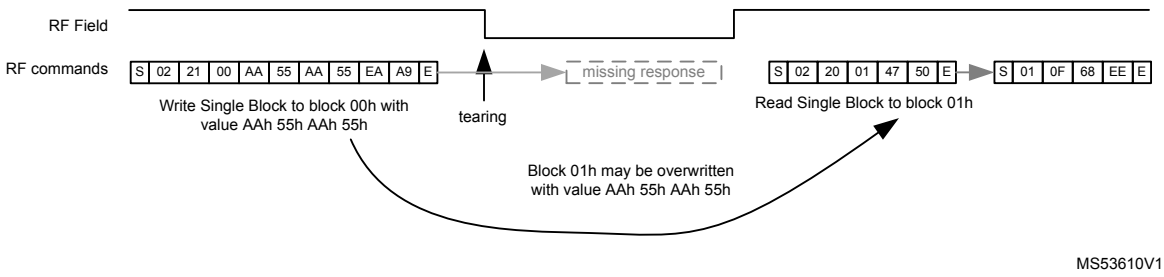
Any memory address can be overwritten, including read-only addresses.

There is no risk for write and read commands that do not access the EEPROM.

RF commands that write into EEPROM are:

- Write single block
- Lock block
- Write multiple blocks
- Write AFI
- Lock AFI
- Write DSFID
- Lock DSFID
- Extended write single block
- Extended lock block
- Extended write multiple blocks
- Write configuration
- Write password

Figure 1. Wrong memory address potentially overwritten after tearing during an RF write in EEPROM when V_{CC} is present



Workaround

This limitation has been fixed in devices with product codes 24h and 26h in revision 13h.

For devices with product codes 25h and 27h the following workaround can be used.

The LPD pin must be permanently kept at high level when V_{CC} is present, and must be pulled to low level only during transmission of I^2C commands to the ST25DV-I2C.

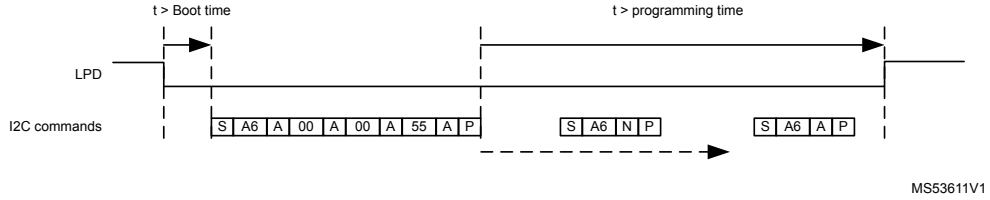
To allow ST25DV-I2C to execute properly the I^2C command, the I^2C master must:

- wait for internal regulator turn on time
- wait for internal LPD boot time after pulling LPD from high to low level, before starting to send I^2C commands

For more details about turning on time of internal regulator and LPD boot time, refer to Dynamic NFC/RFID tag IC with 4-Kbit, 16-Kbit or 64-Kbit EEPROM, and fast transfer mode capability (DS10925) datasheet.

To allow ST25DV-I2C to program correctly EEPROM after a valid I^2C write command in EEPROM, the I^2C master must wait the end of programming time before rising LPD from low to high level. For programming time tw definition refer to Dynamic NFC/RFID tag IC with 4-Kbit, 16-Kbit or 64-Kbit EEPROM, and fast transfer mode capability (DS10925) datasheet

Figure 2. Workaround of wrong memory address potentially overwritten after tearing during an RF write in EEPROM when V_{CC} is present (product codes 25h and 27h in rev 12h)



1.2.2 Wrong memory address potentially overwritten after V_{CC} off during an I^2C write in EEPROM when RF field is present

Impacted devices: All ST25DVxxK devices with product code 25h and 27h

Description

If the following conditions are met:

- RF field is powering the tag during the complete operation
- V_{CC} is lost during the EEPROM programming phase of any I^2C write command to EEPROM
- next I^2C command is a read that accesses data from the EEPROM

Then, depending on the tearing timing in the programming phase, the memory content can potentially be overwritten at memory address pointed by the I^2C read command that follows the tearing.

Any memory address can be overwritten, including read-only addresses.

There is no risk for write and read commands that do not access the EEPROM.

Workaround

There is no workaround for product with product code 25h and 27h.

This limitation has been fixed in product with product code 24h and 26h in revision 13h.

1.2.3 Potential communication lock after tearing during an RF write in EEPROM when V_{CC} is present

Impacted devices: All ST25DVxxK devices with product code 25h and 27h.

Description

If the following conditions are met:

- V_{CC} is powered during the complete operation
- RF field is lost during the EEPROM programming phase of any RF write command to EEPROM
- next RF command is a command that writes data to the EEPROM.

Then, depending on the tearing timing in the programming phase, both RF and I^2C communication to the device can potentially get blocked.

No overwrite of memory occurs in this case, and data from the last write command is not programmed into memory.

In order to recover communication with the device, a complete power-off/power-on cycle must be performed (with both RF field and V_{CC} removed from the device).

There is no risk of blocking if at least one of the two write commands does not access the EEPROM.

RF commands that write into the EEPROM are:

- Write single block
- Lock block
- Write multiple blocks
- Write AFI
- Lock AFI
- Write DSFID
- Lock DSFID
- Extended write single block
- Extended lock block
- Extended write multiple blocks
- Write configuration
- Write password

Workaround

There is no workaround for product with product code 25h and 27h.

This limitation has been fixed in product with product code 24h and 26h and revision 13h.

1.2.4 Potential communication lock after V_{CC} off during an I^2C write in EEPROM when RF field is present

Impacted devices: All ST25DVxxK devices with product code 25h and 27h.

Description

If the following conditions are met:

- RF field is powering the tag during the complete operation
- V_{CC} is lost during the EEPROM programming phase of any I^2C write command to EEPROM
- next I^2C command is a read that accesses data from the EEPROM

Then, depending on the tearing timing in the programming phase, both RF and I^2C communication with the device can potentially get blocked.

No overwrite of memory occurs in this case, and data from the last write command is not programmed into memory.

In order to recover communication with the device, a complete power-off/power-on cycle must be performed (with both RF field and V_{CC} removed from the device).

There is no risk of blocking if at least one of the two write commands does not access the EEPROM.

Workaround

There is no workaround for product with product code 25h and 27h.

This limitation has been fixed in product with product code 24h and 26h and revision 13h.

1.2.5 RF access to EEPROM potentially locked after tearing during an RF read in EEPROM when V_{CC} is present

Impacted devices: All ST25DVxxK devices with product code 25h and 27h.

Description

If the following conditions are met:

- V_{CC} is powered during the complete operation
- RF field is lost during the EEPROM read phase of any RF read command to EEPROM (EEPROM is read during RF response)
- RF field lost is immediately followed by an I^2C command with a device slave address different from A6h/A7h or AEh/AFh (I^2C commands for another slave device).

Then, depending on the tearing timing in the EEPROM reading phase, the access to EEPROM from RF can be blocked: any RF command that reads data into EEPROM is answered with all data values to 0.

RF commands that read into EEPROM are:

- Inventory
- Read single block
- Read multiple blocks
- Extended read single block
- Extended read multiple blocks
- Get system info
- Extended get system info
- Get multiple block security status
- Extended get multiple block security status
- Read configuration
- Present password
- Fast read single block
- Fast read multiple block
- Fast extended read single block
- Fast extended read multiple block

Workaround

This limitation has been fixed in product with product codes 24h and 26h in revision 13h.

For product with product codes 25h and 27h, the following workaround can be used.

The LPD pin must be permanently kept at high level when V_{CC} is present, and must be pulled to low level only during transmission of I^2C commands to the ST25DV-I2C.

To allow ST25DV-I2C to execute properly the I^2C command, the I^2C master must:

- wait for internal regulator turn on time
- wait for internal LPD boot time after pulling LPD from high to low level, before starting to send an I^2C command.

For more details about turning on time of internal regulator and LPD boot time, refer to Dynamic NFC/RFID tag IC with 4-Kbit, 16-Kbit or 64-Kbit EEPROM, and fast transfer mode capability (DS10925) datasheet.

To allow ST25DV-I2C to program correctly EEPROM after a valid I^2C write command in EEPROM, the I^2C master must wait the end of programming time before rising LPD from low to high level. For programming time tw definition refer to Dynamic NFC/RFID tag IC with 4-Kbit, 16-Kbit or 64-Kbit EEPROM, and fast transfer mode capability (DS10925) datasheet.

1.3 I^2C RF arbitration limitations

1.3.1 I^2C busy state not released after an I^2C error

Impacted devices: All ST25DVxxK devices with product code 25h and 27h.

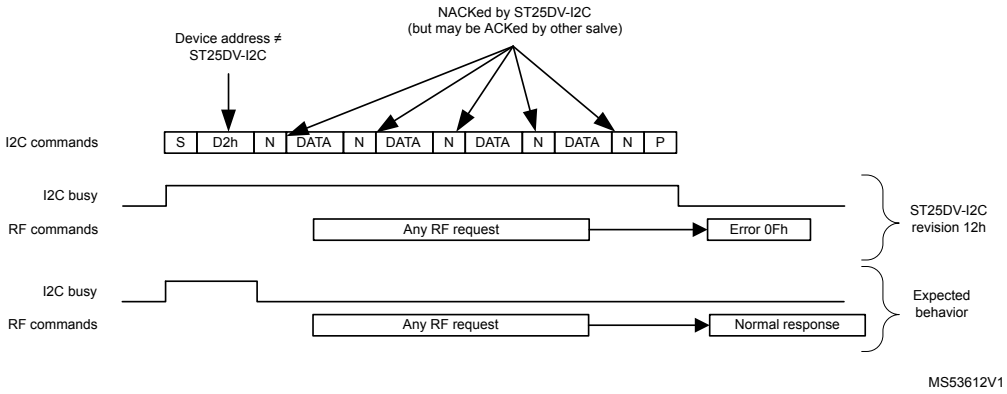
Description

When an error occurs in any I^2C frame (implying the return of a no ACK bit by the ST25DV-I2C), the arbitration does not release the exclusive access and stays in I^2C busy state until the stop condition (or the I^2C timeout condition) is reached.

As a consequence, any RF command received after a no ACK condition and before the I^2C stop condition (or I^2C timeout), is not answered or answered with error 0Fh.

In case of intense traffic on the I²C bus (i.e. multiple slave devices with several frequent accesses), this limitation can create latency or difficult communication from RF.

Figure 3. I²C busy state not released after an I²C error



Workaround

This limitation has been fixed in devices with product codes 24h and 26h in revision 13h.

For devices with product codes 25h and 27h, the following workaround can be used.

The LPD pin must be permanently kept at high level when VCC is present, and must be pulled to low level only during transmission of I²C commands to the ST25DV-I2C.

To allow ST25DV-I2C to execute properly the I²C command, the I²C master must:

- wait for internal regulator turn on time
- wait for internal LPD boot time after pulling LPD from high to low level, before starting to send I²C command

For more details about turning on time of internal regulator and LPD boot time, refer to *Dynamic NFC/RFID tag IC with 4-Kbit, 16-Kbit or 64-Kbit EEPROM, and fast transfer mode capability* (DS10925) datasheet.

To allow ST25DV-I2C to program correctly EEPROM after a valid I²C write command in EEPROM, the I²C master must wait the end of programming time before rising LPD from low to high level. For programming time tw definition refer to *Dynamic NFC/RFID tag IC with 4-Kbit, 16-Kbit or 64-Kbit EEPROM, and fast transfer mode capability* (DS10925) datasheet.

1.3.2 RF response corrupted during I²C programming cycle when I²C is busy

Impacted devices: All ST25DVxxK devices with product code 25h and 27h.

Description

If an RF command is received during an I²C write command to EEPROM (when I²C is busy), and if the RF response occurs during the programing phase following the I²C write command (right after the STOP bit condition), then the RF response gets corrupted after the I²C STOP condition and returns random values instead of the expected values (01h, 0Fh, 68h, FEh).

This does not lock access to the device, neither RF nor I²C and does not corrupt any data.

Workaround

There is no workaround for product with product code 25h and 27h.

This limitation has been fixed in product with product code 24h and 26h in revision 13h.

1.4 Power supply limitations

1.4.1 Potential RF and I²C lock if V_{CC} gets disconnected then reconnected when RF field is present

Impacted devices: All ST25DVxxK devices.

Description

When the device is powered both by V_{CC} and RF field, if V_{CC} pin gets disconnected and left floating (i.e. V_{CC} is connected to a microcontroller GPIO, and the GPIO configuration is changed from output to HiZ), the ST25DVxxK enter an unexpected state where approximately 1.4 V is present on the floating V_{CC} pin.

Once the unexpected V_{CC} at 1.4 V state is reached, the ST25DV-I2C returns to its normal state in the following conditions:

- If RF field disappears (the ST25DV-I2C goes completely off and restarts in normal state when either RF field or V_{CC} power come back)
- If any RF command is received (V_{CC} then goes to 0 V)
- If V_{CC} rises again to its nominal value (>1.8 V).

Nevertheless, if during this unexpected V_{CC} at 1.4 V state, the V_{CC} is pulled down to 0 V and then to its nominal value (1.4 V, then 0 V, then above 1.8 V), the ST25DV-I2C can enter a deadlock state where all I²C accesses are not acknowledged and any RF command is answered with error 0Fh.

The trigger of the deadlock is dependent upon the duration of the negative pulse on V_{CC}.

The negative pulse is acting as a discharge of internal capacitors of the ST25DV-I2C. If the pulse is shorter than 1 ms, the capacitors are not fully discharged and correct internal reset is not occurring, setting the ST25DV-I2C in deadlock state.

Workaround

Several workarounds are available:

- Proper reset is done on V_{CC} side before disconnecting V_{CC} (before configuring the GPIO that controls V_{CC} to HiZ), with duration >1 ms
- Proper reset is done on V_{CC} side before connecting again V_{CC} (before configuring the GPIO that controls V_{CC} from HiZ to its nominal value), with duration >1 ms
- If the glitch to 0 V on V_{CC} that triggers the deadlock state is short enough, an additional capacitor on V_{CC} with time constant longer than the glitch can filter it
- On ST25DV-I2C versions with product codes 51h and 53h, it is possible to properly reset the device by setting the LPD pin high

1.5 Communication limitation

1.5.1 Communication limitation on a marginal portion of production parts (sub-carrier frequency drift)

Impacted device: All ST25DVxxK devices.

Description

In a limited portion of the reading range, and on marginal portion of production parts, communications between some NFC readers and the ST25 products listed above may be lost (communication hole). The communication loss is more likely to occur as the ambient temperature decreases.

The reader and the tag antennas dimensions are impacting the distance where the communication hole happens. The failure mechanism is a loss of clock cycles during the tag back-scattering under some field conditions. Therefore, the tag response may be transmitted with a sub-carrier frequency drift and not be decoded properly by some readers.

Workarounds

- As the communication hole happens only at certain field strength, moving the tag closer or farther to the reader can allow communication with the tag. Applications where the ST25DV is in movement (“tap” gesture, moving parts in production line,…) are less likely to experience the communication loss, as the communication protocol includes retries
- As the temperature has an impact on the issue, using the tag in higher temperature can allow communication with the tag
- Replacing device with a ST25DVxxKC revision 13h (please contact your local ST sales office for availability on specific options).
- Some RF readers are not sensitive to a sub-carrier frequency drift. Reading hole is not seen when using those readers. Recommended readers: ST25R3916, ST25R3916B, ST25R3917, ST25R3917B, ST25R3918, ST25R3919B, ST25R3911B, ST25R3912, ST25R3914, ST25R3915, ST25R3920, and ST25R3920B

1.6 Fast transfer mode limitation

1.6.1 Fast transfer mode watchdog not started correctly after an I²C write message in mailbox

Impacted devices: All ST25DVxxK devices.

Description

At the end of a valid RF write message command in mailbox, the RF_PUT_MSG flag is set in MB_CTRL_Dyn register. This flag must be cleared only if the mailbox is deactivated or if the I²C has read the complete message, or if the watchdog is triggered. But if the message is 256 bytes long, and if the first I²C command after the RF has written the message is a read of MB_LEN_Dyn register (user address 2007h), the RF_PUT_MSG flag is wrongly cleared.

Workaround

After the RF has written a message in the mailbox, it is recommended to check the MB_CTRL_Dyn register to verify if a message is present, before reading MB_LEN_Dyn to check its size. Therefore, it is recommended for the I2C host to read first MB_CTRL_Dyn, then MB_LEN_dyn, then the message in mailbox. This can be done in a single read sequential command, starting at address 2006h (MB_CTRL_Dyn) and ending at end of the mailbox (258 bytes are read). This sequentially reads the MB_CTRL_Dyn register, the MB_LEN_Dyn register and the full mailbox content.

1.6.2 RF_PUT_MSG bit wrongly cleared after I²C reading MB_LEN_Dyn if message is 256 bytes long

Impacted devices: All ST25DVxxK devices.

Description

At the end of a valid RF Write Message command in mailbox, the RF_PUT_MSG flag is set in MB_CTRL_Dyn register. This flag must be cleared only if the mailbox is deactivated or if the I²C has read the complete message, or if the watchdog is triggered. But if the message is 256 bytes long, and if the first I²C command after the RF has written the message is a read of MB_LEN_Dyn register (user address 2007h), the RF_PUT_MSG flag is wrongly cleared.

Workaround

After the RF has written a message in the mailbox, it is recommended to check the MB_CTRL_Dyn register to verify if a message is present, before reading MB_LEN_Dyn to check its size. Therefore, it is recommended for the I²C host to read first MB_CTRL_Dyn, then MB_LEN_dyn, then the message in mailbox. This can be done in a single read sequential command, starting at address 2006h (MB_CTRL_Dyn) and ending at end of the mailbox (258 bytes are read). This sequentially reads the MB_CTRL_Dyn register, the MB_LEN_Dyn register and the full mailbox content.

Revision history

Table 3. **Document revision history**

Date	Version	Changes
07-Jul-2023	1	Initial release.

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