



## STM32WBA50xx device errata

## Applicability

This document applies to the part numbers of STM32WBA50xx devices and the device variants as stated in this page.

It gives a summary and a description of the device errata, with respect to the device datasheet and reference manual RM0493.

Deviation of the real device behavior from the intended device behavior is considered to be a device limitation. Deviation of the description in the reference manual or the datasheet from the intended device behavior is considered to be a documentation erratum. The term “*errata*” applies both to limitations and documentation errata.

**Table 1. Device summary**

Reference	Part numbers
STM32WBA50xx	STM32WBA50KG

**Table 2. Device variants**

Reference	Silicon revision codes	
	Device marking <sup>(1)</sup>	REV_ID <sup>(2)</sup>
STM32WBA50xx	B	0x2000

1. Refer to the device datasheet for how to identify this code on different types of package.
2. REV\_ID[15:0] bitfield of DBGMCU\_IDCODE register.

# 1 Summary of device errata

The following table gives a quick reference to the STM32WBA50xx device limitations and their status:

A = limitation present, workaround available

N = limitation present, no workaround available

P = limitation present, partial workaround available

“-” = limitation absent

Applicability of a workaround may depend on specific conditions of target application. Adoption of a workaround may cause restrictions to target application. Workaround for a limitation is deemed partial if it only reduces the rate of occurrence and/or consequences of the limitation, or if it is fully effective for only a subset of instances on the device or in only a subset of operating modes, of the function concerned.

**Table 3. Summary of device limitations**

Function	Section	Limitation	Status
			Rev. B
Core	2.1.1	Access permission faults are prioritized over unaligned Device memory faults	N
System	2.2.1	Device-specific authentication ID is not accessible in RDP Level 0	A
	2.2.2	HSEPRE cannot be changed while HSE is set as system clock or PLL source	A
	2.2.3	Bit LPWRRSTF of RCC_CSR can always be read	N
	2.2.4	Glitches on PA2 and PA7 in retention Standby mode	A
	2.2.5	ICACHE clock requires register RCC_AHB1ENR to have a non-zero value	A
	2.2.6	Reset can cause the system to get stuck in Standby mode	N
	2.2.7	RTC clocked by LSI stops working when a reset is triggered from the NRST pad	A
	2.2.8	Fast-mode Plus cannot be activated using SYSCFG_CFGR1 register	N
	2.2.9	Longer HSE32 stabilization time when the clock is stopped for a time between 2 and 5 ms	A
	2.2.10	ICACHE fails after exiting Stop 1 mode	A
Radio system	2.3.1	Bluetooth® Low Energy frequency deviation (DF1)	P
	2.3.2	Nonlinear behavior of Bluetooth® Low Energy RSSI reporting	N
LPTIM	2.6.1	Device may remain stuck in LPTIM interrupt when entering Stop mode	A
	2.6.2	ARRM and CMPM flags are not set when APB clock is slower than kernel clock	A
	2.6.3	Interrupt status flag is cleared by hardware upon writing its corresponding bit in LPTIM_DIER register	N
RTC	2.7.1	Alarm flag may be repeatedly set when the core is stopped in debug	N
I2C	2.8.1	Wrong data sampling when data setup time ( $t_{SU, DAT}$ ) is shorter than one I2C kernel clock period	P
	2.8.2	Spurious bus error detection in controller mode	A
USART	2.9.1	Wrong data received by SPI slave receiver in autonomous mode with CPOL = 1	A
	2.9.2	Received data may be corrupted upon clearing the ABREN bit	A
	2.9.3	Noise error flag set while ONEBIT is set	N
LPUART	2.10.1	Possible LPUART transmitter issue when using low BRR[15:0] value	P
SPI	2.11.1	RDY output failure at high serial clock frequency	N

The following table gives a quick reference to the documentation errata.

**Table 4. Summary of device documentation errata**

Function	Section	Documentation erratum
Radio system	2.3.3	HSE overconsumption for radio
TSC	2.4.1	Inhibited acquisition in short transfer phase configuration
SAES	2.5.1	Data transfer from TAMP_BKPxR to key registers must be done only in ascending order when KEYSEL[2:0] is set to 010 or 100

## 2 Description of device errata

The following sections describe the errata of the applicable devices with Arm® core and provide workarounds if available. They are grouped by device functions.

*Note:* Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

arm

### 2.1 Core

Reference manual and errata notice for the Arm® Cortex®-M33 core revision r0p1 is available from <http://infocenter.arm.com>.

#### 2.1.1 Access permission faults are prioritized over unaligned Device memory faults

##### Description

A load or store which causes an unaligned access to Device memory will result in an UNALIGNED UsageFault exception. However, if the region is not accessible because of the MPU access permissions (as specified in MPU\_RBAR.AP), then the resulting MemManage fault will be prioritized over the UsageFault.

The failure occurs when the MPU is enabled and:

- A load/store access occurs to an address which is not aligned to the data type specified in the instruction.
- The memory access hits one region only.
- The region attributes (specified in the MAIR register) mark the location as Device memory.
- The region access permissions prevent the access (that is, unprivileged or write not allowed).

The MemManage fault caused by the access permission violation will be prioritized over the UNALIGNED UsageFault exception because of the memory attributes.

##### Workaround

None. However, it is expected that no existing software is relying on this behavior since it was permitted in Armv7-M.

### 2.2 System

#### 2.2.1 Device-specific authentication ID is not accessible in RDP Level 0

##### Description

The AUTH\_ID bitfield of the DBGMCU\_DBG\_AUTH\_DEVICE register is not accessible in RDP Level 0. The read value is always 0. Therefore, this bitfield cannot be used to discriminate between different devices.

##### Workaround

Increase the RDP to Level 1 before reading the device-specific authentication ID. Then, decrease the RDP back to Level 0.

#### 2.2.2 HSEPRE cannot be changed while HSE is set as system clock or PLL source

##### Description

The clock divider may produce glitches if changed while HSE is running.

##### Workaround

Set the system clock temporarily to HSI, then change the HSEPRE setting of the divider.

### 2.2.3 Bit LPWRRSTF of RCC\_CSR can always be read

#### Description

Bit LPWRRSTF of RCC\_CSR can be always read regardless of the privilege level set in the RCC\_PRIVCFGR register.

#### Workaround

None

### 2.2.4 Glitches on PA2 and PA7 in retention Standby mode

#### Description

PA2 and PA7 correspond with ADC4\_IN7 and ADC4\_IN2. When coming into or coming out of Standby mode with retention, these signals may show glitches.

#### Workaround

Discard the IO retention feature, and force the pull-down on these two signals.

### 2.2.5 ICACHE clock requires register RCC\_AHB1ENR to have a non-zero value

#### Description

ICACHE can be configured to perform an address remap to SRAM.

The ICACHE clock is disabled when all the bits of the RCC\_AHB1ENR register are at zero.

A deadlock can occur when:

- code and data are stored in SRAM2,
- ICACHE is configured to remap the addresses 0x0A00/0x0E00 to 0x2000/0x3000,
- all the register RCC\_AHB1ENR bits are at zero, and
- the CPU attempts to reboot from 0x0A00/0x0E00.

The device does not boot.

#### Workaround

Ensure that at least one bit of the RCC\_AHB1ENR register is set.

### 2.2.6 Reset can cause the system to get stuck in Standby mode

#### Description

If NRESET is activated after a few nanoseconds of an internal standby request, the system may be unable to exit Standby mode, in which case a POR is necessary.

#### Workaround

None.

### 2.2.7 RTC clocked by LSI stops working when a reset is triggered from the NRST pad

#### Description

An external trigger from the NRST pad resets the LSI1ON, LSI1PREDIV, and RADIOSTSEL bits of the RCC\_BDCR1 register, causing RTC and TAMP to stop functioning.

#### Workaround

Use LSE as the clock for RTC.

## 2.2.8 Fast-mode Plus cannot be activated using SYSCFG\_CFGR1 register

### Description

The activation of the Fast-mode Plus mode on GPIO PB3, PA15, PA7, or PA6 by setting the corresponding bit in the SYSCFG\_CFGR1 register is ineffective.

### Workaround

None.

## 2.2.9 Longer HSE32 stabilization time when the clock is stopped for a time between 2 and 5 ms

### Description

When the HSE32 is restarted after having been off within a window of time between 2 and 5 ms, it may be not ready even if the HSERDY bit is set in the RCC\_CR register. This may result in a CPU hard fault, wrong timer counting, or an incorrect behavior of the other peripherals that use the HSE32 clock.

In this case, the HSE32 oscillator stabilization time  $t_{STAB}$  may be increased by 1 ms (360  $\mu$ s typical).

### Workaround

Apply the following measure in applications where the HSE32 clock is stopped for more than 2 ms and less than 5 ms:

1. Before stopping the HSE32 clock, deselect HSE32 for all the peripherals that use this clock as kernel clock:
  - SYSCLK via the SW[1:0] bitfield of the RCC\_CFGR1 register
  - PLL1 via the PLL1SRC[1:0] bitfield of the RCC\_PLL1CFGR register
  - RTC and TAMP via the RTCSEL[1:0] bitfield in the RCC\_BDCR1 register
  - ADC4 via the ADCSEL[2:0] bitfield of the RCC\_CCIPR3 register
  - 2.4 GHz RADIO sleep clock via the RADIOSTSEL[1:0] bitfield of the RCC\_BDCR1 register.
  - 2.4 GHz RADIO baseband kernel clock shall be disabled via the BBCLKEN bitfield of the RCC\_RADIOENR register.
2. Wait until HSERDY is set, then wait for an additional time of 200  $\mu$ s before using HSE32 again for the SYSCLK, PLL1, RTC, TAMP, ADC4, 2.4 GHz RADIO sleep clock, or 2.4 GHz RADIO baseband clock.
3. Keep the HSE clock security disabled, by clearing the HSECSSON bit in the RCC\_CR register.

The above measure does not prevent the 2.4 GHz RADIO to occasionally miss some packets when  $t_{STAB}$  is higher than 360  $\mu$ s and smaller than 1 ms). To prevent this issue for occurring, the 2.4 GHz RADIO wake-up can be anticipated by 600  $\mu$ s.

## 2.2.10 ICACHE fails after exiting Stop 1 mode

### Description

If the ICACHE content is not retained, its content may be invalid after exiting the Stop 1 mode. This may lead to a wrong cache hit.

### Workaround

Apply one of the following measures:

- Retain the ICACHE content.
- Force the invalidation when exiting Stop 1.

## 2.3 Radio system

### 2.3.1 Bluetooth® Low Energy frequency deviation (DF1)

#### Description

Channel 15 and 31 frequencies are out of specifications.

**Workaround**

Discard channels 15 and 31 by issuing an HCI update channel map command HCI\_LE\_SET\_HOST\_CHANNEL\_CLASSIFICATION.

**2.3.2 Nonlinear behavior of Bluetooth® Low Energy RSSI reporting**

**Description**

The RSSI is linear only in the range [-32 dBm; -70 dBm].

**Workaround**

None.

**2.3.3 HSE overconsumption for radio**

**Description**

The product datasheet indicates an incorrect value for the power consumption when using the HSE clock. The actual value exceeds the indicated value by 200 µA, for both Tx and Rx cycles.

**Workaround**

No application workaround is required.

**2.4 TSC**

**2.4.1 Inhibited acquisition in short transfer phase configuration**

**Description**

Some revisions of the reference manual may omit the information that the following configurations of the TSC\_CR register are forbidden:

- The PGPSC[2:0] bitfield set to 000 and the CTPL[3:0] bitfield to 0000 or 0001
- The PGPSC[2:0] bitfield set to 001 and the CTPL[3:0] bitfield to 0000

Failure to respect this restriction leads to an inhibition of the acquisition.

This is a documentation inaccuracy issue rather than a product limitation.

**Workaround**

No application workaround is required.

**2.5 SAES**

**2.5.1 Data transfer from TAMP\_BKPxR to key registers must be done only in ascending order when KEYSEL[2:0] is set to 010 or 100**

**Description**

The KEYSEL[2:0] bitfield of the SAES\_CR register defines the source of the key information to use in the SAES cryptographic core:

- When KEYSEL[2:0] is set to 010, the boot hardware key (BHK), stored in tamper-resistant secure backup registers, is entirely transferred into the key registers upon a secure application performing a single read of all TAMP\_BKPxR registers (x = 0 to 3 for KEYSIZE = 0, x = 0 to 7 for KEYSIZE = 1).
- When KEYSEL[2:0] is set to 100, the XOR combination of DHUK and BHK is entirely transferred into the key registers upon a secure application performing a single read of all TAMP\_BKPxR registers (x = 0 to 3 for KEYSIZE = 0, x = 0 to 7 for KEYSIZE = 1).

Some revisions of the reference manual may wrongly specify that the read operation can be performed either in ascending or descending order, while it must be performed always in **ascending** order.

This is a documentation issue rather than a product limitation.

#### Workaround

No application workaround is required, provided that the read operation to the TAMP\_BKPxR registers is always done in ascending order.

## 2.6 LPTIM

### 2.6.1 Device may remain stuck in LPTIM interrupt when entering Stop mode

#### Description

This limitation occurs when disabling the low-power timer (LPTIM).

When the user application clears the ENABLE bit in the LPTIM\_CR register within a small time window around one LPTIM interrupt occurrence, then the LPTIM interrupt signal used to wake up the device from Stop mode may be frozen in active state. Consequently, when trying to enter Stop mode, this limitation prevents the device from entering low-power mode and the firmware remains stuck in the LPTIM interrupt routine.

This limitation applies to all Stop modes and to all instances of the LPTIM. Note that the occurrence of this issue is very low.

#### Workaround

In order to disable a low power timer (LPTIMx) peripheral, do not clear its ENABLE bit in its respective LPTIM\_CR register. Instead, reset the whole LPTIMx peripheral via the RCC controller by setting and resetting its respective LPTIMxRST bit in the relevant RCC register.

### 2.6.2 ARRM and CMPM flags are not set when APB clock is slower than kernel clock

#### Description

When LPTIM is configured in one shot mode and APB clock is lower than kernel clock, there is a chance that ARRM and CMPM flags are not set at the end of the counting cycle defined by the repetition value REP[7:0]. This issue can only occur when the repetition counter is configured with an odd repetition value.

#### Workaround

To avoid this issue the following formula must be respected:

$$\{ARR, CMP\} \geq KER\_CLK / (2 * APB\_CLK),$$

where APB\_CLK is the LPTIM APB clock frequency, and KER\_CLK is the LPTIM kernel clock frequency. ARR and CMP are expressed in decimal value.

**Example:** The following example illustrates a configuration where the issue can occur:

- APB clock source (MSI) = 1 MHz , Kernel clock source (HSI) = 16 MHz
- Repetition counter is set with REP[7:0] = 0x3 (odd value)

The above example is subject to issue, unless the user respects:

$$\{CMP, ARR\} \geq 16 \text{ MHz} / (2 * 1 \text{ MHz})$$

→ ARR must be  $\geq 8$  and CMP must be  $\geq 8$

*Note:* REP set to 0x3 means that effective repetition is REP+1 (= 4) but the user must consider the parity of the value loaded in LPTIM\_RCR register (=3, odd) to assess the risk of issue.

### 2.6.3 Interrupt status flag is cleared by hardware upon writing its corresponding bit in LPTIM\_DIER register

#### Description

When any interrupt bit of the LPTIM\_DIER register is modified, the corresponding flag of the LPTIM\_ISR register is cleared by hardware.



**Workaround**

None.

**2.7 RTC**
**2.7.1 Alarm flag may be repeatedly set when the core is stopped in debug**
**Description**

When the core is stopped in debug mode, the clock is supplied to subsecond RTC alarm downcounter even when the device is configured to stop the RTC in debug.

As a consequence, when the subsecond counter is used for alarm condition (the MASKSS[3:0] bitfield of the RTC\_ALRMASR and/or RTC\_ALRMBSSR register set to a non-zero value) and the alarm condition is met just before entering a breakpoint or printf, the ALRAF and/or ALRBF flag of the RTC\_SR register is repeatedly set by hardware during the breakpoint or printf, which makes any attempt to clear the flag(s) ineffective.

**Workaround**

None.

**2.8 I2C**
**2.8.1 Wrong data sampling when data setup time ( $t_{SU, DAT}$ ) is shorter than one I2C kernel clock period**
**Description**

The I<sup>2</sup>C-bus specification and user manual specify a minimum data setup time ( $t_{SU, DAT}$ ) as:

- 250 ns in Standard mode
- 100 ns in Fast mode
- 50 ns in Fast mode Plus

The device does not correctly sample the I<sup>2</sup>C-bus SDA line when  $t_{SU, DAT}$  is smaller than one I2C kernel clock (I<sup>2</sup>C-bus peripheral clock) period: the previous SDA value is sampled instead of the current one. This can result in a wrong receipt of target address, data byte, or acknowledge bit.

**Workaround**

Increase the I2C kernel clock frequency to get I2C kernel clock period within the transmitter minimum data setup time. Alternatively, increase transmitter's minimum data setup time. If the transmitter setup time minimum value corresponds to the minimum value provided in the I<sup>2</sup>C-bus standard, the minimum I2CCLK frequencies are as follows:

- In Standard mode, if the transmitter minimum setup time is 250 ns, the I2CCLK frequency must be at least 4 MHz.
- In Fast mode, if the transmitter minimum setup time is 100 ns, the I2CCLK frequency must be at least 10 MHz.
- In Fast-mode Plus, if the transmitter minimum setup time is 50 ns, the I2CCLK frequency must be at least 20 MHz.

**2.8.2 Spurious bus error detection in controller mode**
**Description**

In controller mode, a bus error can be detected spuriously, with the consequence of setting the BERR flag of the I2C\_SR register and generating bus error interrupt if such interrupt is enabled. Detection of bus error has no effect on the I<sup>2</sup>C-bus transfer in controller mode and any such transfer continues normally.

### Workaround

If a bus error interrupt is generated in controller mode, the BERR flag must be cleared by software. No other action is required and the ongoing transfer can be handled normally.

## 2.9 USART

### 2.9.1 Wrong data received by SPI slave receiver in autonomous mode with CPOL = 1

#### Description

The SPI slave receiver device receives wrong data when all the following conditions are met:

- The USART is used in SPI master transmitter mode
- The autonomous mode is used
- The CPOL bit of the USART\_CR2 register is set

#### Workaround

When the autonomous mode is used, do not set the CPOL bit in USART\_CR2.

### 2.9.2 Received data may be corrupted upon clearing the ABREN bit

#### Description

The USART receiver may miss data or receive corrupted data when the auto baud rate feature is disabled by software (ABREN bit cleared in the USART\_CR2 register) after an auto baud rate detection, while a reception is ongoing.

#### Workaround

Do not clear the ABREN bit.

### 2.9.3 Noise error flag set while ONEBIT is set

#### Description

When the ONEBIT bit is set in the USART\_CR3 register (one sample bit method is used), the noise error (NE) flag must remain cleared. Instead, this flag is set upon noise detection on the START bit.

#### Workaround

None.

*Note: Having noise on the START bit is contradictory with the fact that the one sample bit method is used in a noise free environment.*

## 2.10 LPUART

### 2.10.1 Possible LPUART transmitter issue when using low BRR[15:0] value

#### Description

The LPUART transmitter bit length sequence is not reset between consecutive bytes, which could result in a jitter that cannot be handled by the receiver device. As a result, depending on the receiver device bit sampling sequence, a desynchronization between the LPUART transmitter and the receiver device may occur resulting in data corruption on the receiver side.

This happens when the ratio between the LPUART kernel clock and the baud rate programmed in the LPUART\_BRR register (BRR[15:0]) is not an integer, and is in the three to four range. A typical example is when the 32.768 kHz clock is used as kernel clock and the baud rate is equal to 9600 baud, resulting in a ratio of 3.41.

**Workaround**

Apply one of the following measures:

- On the transmitter side, increase the ratio between the LPUART kernel clock and the baud rate. To do so:
  - Increase the LPUART kernel clock frequency, or
  - Decrease the baud rate.
- On the receiver side, generate the baud rate by using a higher frequency and applying oversampling techniques if supported.

**2.11 SPI****2.11.1 RDY output failure at high serial clock frequency****Description**

When acting as slave with RDY alternate function enabled through setting the RDIOM bit of the SPI\_CFG2 register, the device may fail to indicate its *Not ready* status in time through the RDY output signal to suspend communication. This may then lead to data overrun and/or underrun on the device side. The failure occurs when the serial clock frequency exceeds:

- twice the APB clock frequency, with data sizes from 8 to 15 bits
- six times the APB clock frequency, with data sizes from 16 to 23 bits
- fourteen times the APB clock frequency, with data sizes from 24 to 32 bits

**Workaround**

None.

## Important security notice

The STMicroelectronics group of companies (ST) places a high value on product security, which is why the ST product(s) identified in this documentation may be certified by various security certification bodies and/or may implement our own security measures as set forth herein. However, no level of security certification and/or built-in security measures can guarantee that ST products are resistant to all forms of attacks. As such, it is the responsibility of each of ST's customers to determine if the level of security provided in an ST product meets the customer needs both in relation to the ST product alone, as well as when combined with other components and/or software for the customer end product or application. In particular, take note that:

- ST products may have been certified by one or more security certification bodies, such as Platform Security Architecture ([www.psacertified.org](http://www.psacertified.org)) and/or Security Evaluation standard for IoT Platforms ([www.trustcb.com](http://www.trustcb.com)). For details concerning whether the ST product(s) referenced herein have received security certification along with the level and current status of such certification, either visit the relevant certification standards website or go to the relevant product page on [www.st.com](http://www.st.com) for the most up to date information. As the status and/or level of security certification for an ST product can change from time to time, customers should re-check security certification status/level as needed. If an ST product is not shown to be certified under a particular security standard, customers should not assume it is certified.
- Certification bodies have the right to evaluate, grant and revoke security certification in relation to ST products. These certification bodies are therefore independently responsible for granting or revoking security certification for an ST product, and ST does not take any responsibility for mistakes, evaluations, assessments, testing, or other activity carried out by the certification body with respect to any ST product.
- Industry-based cryptographic algorithms (such as AES, DES, or MD5) and other open standard technologies which may be used in conjunction with an ST product are based on standards which were not developed by ST. ST does not take responsibility for any flaws in such cryptographic algorithms or open technologies or for any methods which have been or may be developed to bypass, decrypt or crack such algorithms or technologies.
- While robust security testing may be done, no level of certification can absolutely guarantee protections against all attacks, including, for example, against advanced attacks which have not been tested for, against new or unidentified forms of attack, or against any form of attack when using an ST product outside of its specification or intended use, or in conjunction with other components or software which are used by customer to create their end product or application. ST is not responsible for resistance against such attacks. As such, regardless of the incorporated security features and/or any information or support that may be provided by ST, each customer is solely responsible for determining if the level of attacks tested for meets their needs, both in relation to the ST product alone and when incorporated into a customer end product or application.
- All security features of ST products (inclusive of any hardware, software, documentation, and the like), including but not limited to any enhanced security features added by ST, are provided on an "AS IS" BASIS. AS SUCH, TO THE EXTENT PERMITTED BY APPLICABLE LAW, ST DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, unless the applicable written and signed contract terms specifically provide otherwise.

## Revision history

**Table 5. Document revision history**

Date	Version	Changes
16-Sep-2024	1	Initial release
14-Jan-2025	2	Added: <ul style="list-style-type: none"> <li>• Section 2.2.8: Fast-mode Plus cannot be activated using SYSCFG_CFGR1 register</li> <li>• Section 2.2.9: Longer HSE32 stabilization time when the clock is stopped for a time between 2 and 5 ms</li> <li>• Section 2.2.10: ICACHE fails after exiting Stop 1 mode</li> <li>• Section 2.4.1: Inhibited acquisition in short transfer phase configuration</li> <li>• Section 2.5.1: Data transfer from TAMP_BKPxR to key registers must be done only in ascending order when KEYSEL[2:0] is set to 010 or 100</li> <li>• Section 2.11.1: RDY output failure at high serial clock frequency</li> </ul>

## Contents

<b>1</b>	<b>Summary of device errata</b>	<b>2</b>
<b>2</b>	<b>Description of device errata</b>	<b>4</b>
2.1	Core	4
2.1.1	Access permission faults are prioritized over unaligned Device memory faults	4
2.2	System	4
2.2.1	Device-specific authentication ID is not accessible in RDP Level 0	4
2.2.2	HSEPRE cannot be changed while HSE is set as system clock or PLL source	4
2.2.3	Bit LPWRRSTF of RCC_CSR can always be read	5
2.2.4	Glitches on PA2 and PA7 in retention Standby mode	5
2.2.5	ICACHE clock requires register RCC_AHB1ENR to have a non-zero value	5
2.2.6	Reset can cause the system to get stuck in Standby mode	5
2.2.7	RTC clocked by LSI stops working when a reset is triggered from the NRST pad	5
2.2.8	Fast-mode Plus cannot be activated using SYSCFG_CFGR1 register	6
2.2.9	Longer HSE32 stabilization time when the clock is stopped for a time between 2 and 5 ms	6
2.2.10	ICACHE fails after exiting Stop 1 mode	6
2.3	Radio system	6
2.3.1	Bluetooth® Low Energy frequency deviation (DF1)	6
2.3.2	Nonlinear behavior of Bluetooth® Low Energy RSSI reporting	7
2.3.3	HSE overconsumption for radio	7
2.4	TSC	7
2.4.1	Inhibited acquisition in short transfer phase configuration	7
2.5	SAES	7
2.5.1	Data transfer from TAMP_BKPxR to key registers must be done only in ascending order when KEYSEL[2:0] is set to 010 or 100	7
2.6	LPTIM	8
2.6.1	Device may remain stuck in LPTIM interrupt when entering Stop mode	8
2.6.2	ARRM and CMPM flags are not set when APB clock is slower than kernel clock	8
2.6.3	Interrupt status flag is cleared by hardware upon writing its corresponding bit in LPTIM_DIER register	8
2.7	RTC	9
2.7.1	Alarm flag may be repeatedly set when the core is stopped in debug	9
2.8	I2C	9
2.8.1	Wrong data sampling when data setup time ( $t_{SU,DAT}$ ) is shorter than one I2C kernel clock period	9
2.8.2	Spurious bus error detection in controller mode	9
2.9	USART	10

---

2.9.1	Wrong data received by SPI slave receiver in autonomous mode with CPOL = 1 . . . . .	10
2.9.2	Received data may be corrupted upon clearing the ABREN bit. . . . .	10
2.9.3	Noise error flag set while ONEBIT is set . . . . .	10
2.10	LPUART . . . . .	10
2.10.1	Possible LPUART transmitter issue when using low BRR[15:0] value. . . . .	10
2.11	SPI . . . . .	11
2.11.1	RDY output failure at high serial clock frequency . . . . .	11
<b>Important security notice . . . . .</b>		<b>12</b>
<b>Revision history . . . . .</b>		<b>13</b>

**IMPORTANT NOTICE – READ CAREFULLY**

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgment.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to [www.st.com/trademarks](http://www.st.com/trademarks). All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2025 STMicroelectronics – All rights reserved