



ST25R3916B, ST25R3917B, ST25R3919B, and ST25R3920B device limitations

Silicon identification

This errata sheet applies to the ST25R3916B, ST25R3917B, ST25R3919B, and ST25R3920B products.

Identification by SPI or I²C

The part can be identified by reading the product revision code in the IC identity register at address 3Fh.

The limitations described in this document apply to product revision 4.0, which corresponds to an IC identity register readout of 30h.

1 Summary of silicon limitations

The following table gives a quick reference to all documented limitations.

Legend of Table 1:

- A = limitation present, workaround available
- N = limitation present, no workaround available
- P = limitation present, partial workaround available
- '-' limitation absent or fixed

Table 1. Summary of silicon limitations

Function	Silicon limitations	Workaround			
		ST25R3916B	ST25R3917B	ST25R3919B	ST25R3920B
Section 1.1: Interrupt and associated reporting limitations	Section 1.1.1: Serial peripheral interface (SPI)	A	A	A	A

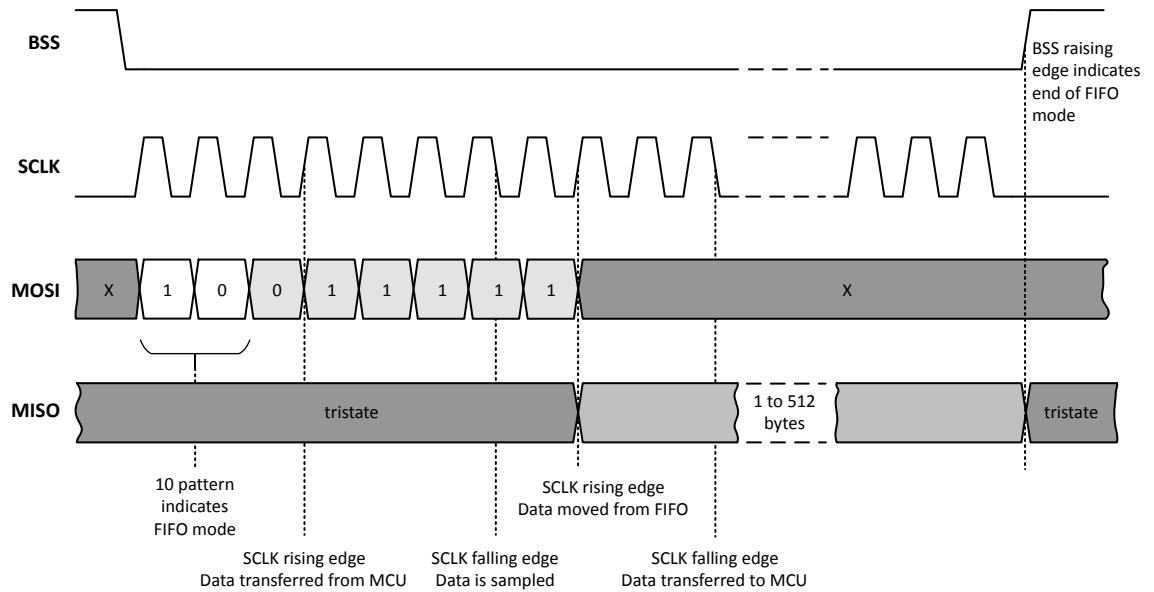
1.1 Interrupt and associated reporting limitations

1.1.1 Serial peripheral interface (SPI)

Description

During the read operation of the interrupt status register, under specific bit patterns of the MOSI line identified as X in Figure 1, the interrupt flags might not be valid, and the interrupt line stays high.

Figure 1. SPI communication: FIFO reading

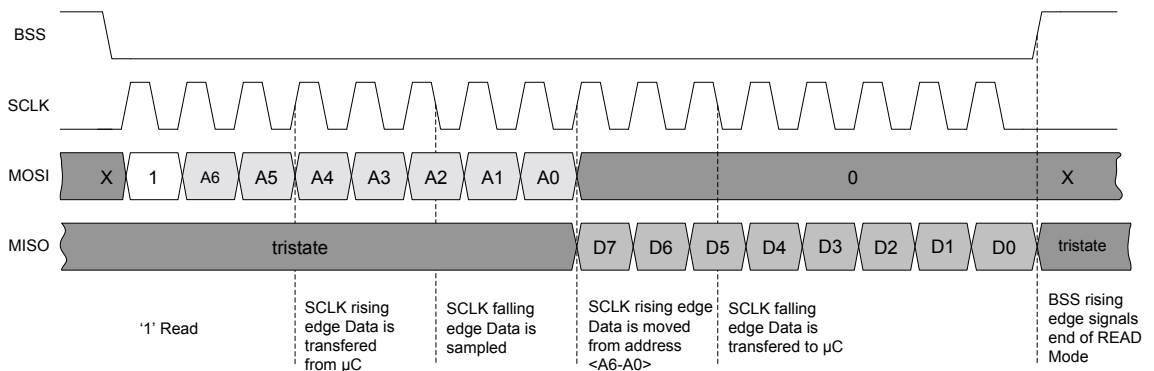


DT53128V1

Workaround

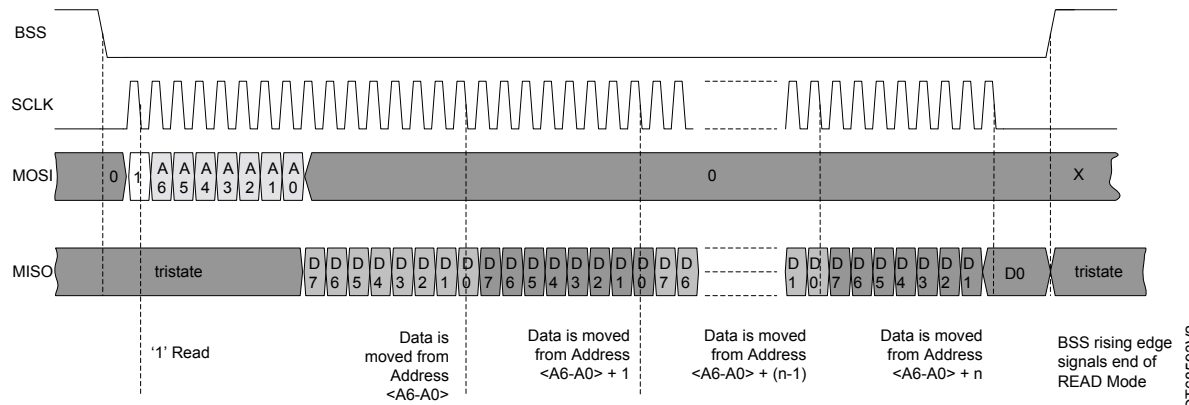
The MOSI line must be driven low after the interrupt status register address bits, as shown in Figure 2 and Figure 3, for reading single and multiple bytes.

Figure 2. SPI communication: reading a single byte



DT68592V2

Figure 3. SPI communication: reading multiple bytes



DT68593V2



Revision history

Table 2. Document revision history

Date	Revision	Changes
28-Jan-2025	1	Initial release.



Contents

1	Summary of silicon limitations	2
1.1	Interrupt and associated reporting limitations	3
1.1.1	Serial peripheral interface (SPI)	3
	Revision history	5
	List of tables	7
	List of figures	8



List of tables

Table 1.	Summary of silicon limitations	2
Table 2.	Document revision history	5



List of figures

Figure 1.	SPI communication: FIFO reading	3
Figure 2.	SPI communication: reading a single byte	3
Figure 3.	SPI communication: reading multiple bytes	4



IMPORTANT NOTICE – READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgment.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2025 STMicroelectronics – All rights reserved