

# Ultra-low clamping voltage 0201 ESD diodes



## This new ultra-low clamping 0201 Z-series completes the existing and large range of ST single ESD protection devices

To protect microcontrollers and ICs against ESD strikes, ST's 0201 single-line protection ICs with snapback effect drastically reduce the clamping voltage down to 7 V for an 8 kV ESD discharge.

As circuits become denser in compliance with Moore's law, technologies become more vulnerable to ESD events. ST satisfies customers' needs for tiny, efficient and robust protection devices.

### KEY FEATURES

- Efficiency and robustness
- Ultra-low clamping voltage: 7 V after 30 ns (IEC 61000-4-2 ESD contact discharge)
- 0201 flexible and standard package (0.6 x 0.3 mm)
- Very low capacitance down to 6 pF
- Very low leakage current below 100 nA
- Up to 18 kV IEC 61000-4-2 ESD contact discharge
- Up to 7 A 8/20  $\mu$ s peak pulse current

### KEY BENEFITS

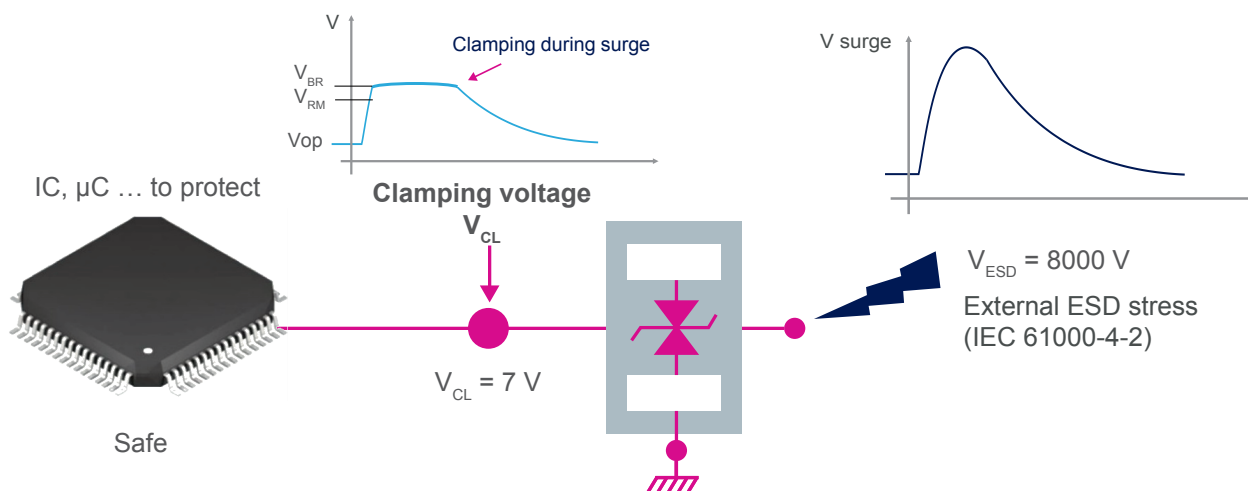
- Easy design and PCB layout
- System immunity against ESD
- Smaller form factor with more functionalities

### KEY APPLICATIONS

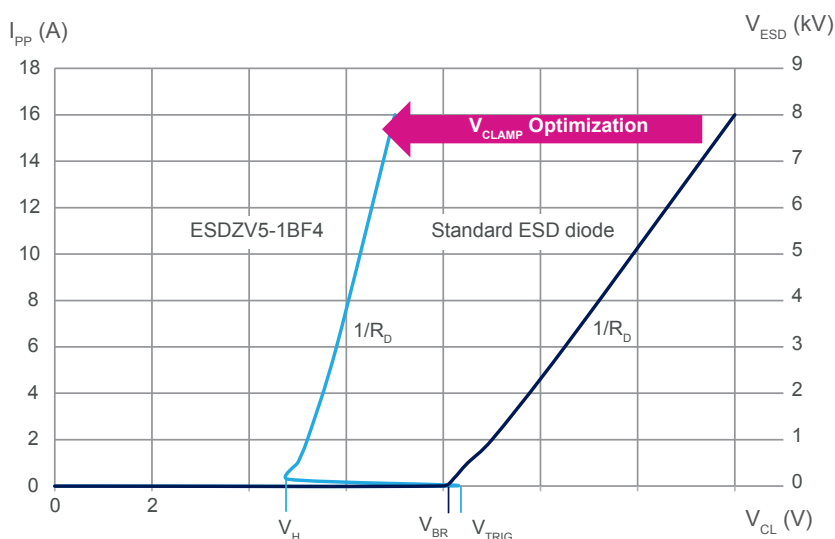
- Smart watches
- Fitness devices
- Wireless speakers
- Access control devices
- Point-of-sale terminals
- Active cables and connectors
- Healthcare devices
- Industrial sensors
- Wearables
- Smartphones and portable devices
- Laptops and peripherals

## GET RID OF ESD HAZARDS

ESD surges of 8 kV are clamped down to 8 V protecting IC or microcontroller from external ESD hazards



Clamping voltage is divided by 2



## ULTRA-LOW CLAMPING VOLTAGE

### Snapback effect

The 0201 Z-series behaves differently from standard ESD diodes, which start to clamp from the breakdown voltage  $V_{BR}$  value (corresponding to the avalanche voltage of the diode) following a slope linked to the dynamic resistance  $R_D$  of the diode. The clamping voltage is given by  $V_{CL} = V_{BR} + R_D \cdot I_{PP}$ , where  $I_{PP}$  is the peak pulse current.

The 0201 Z-series ESD diodes offer a Snapback effect that will not turn on until reaching their trigger voltage ( $V_{TRIG}$ ). Once  $V_{TRIG}$  reached, then the voltage will suddenly decrease down the holding voltage ( $V_H$ ). In this case,  $V_{CL} = V_H + R_D \cdot I_{PP}$ . This new protection technology also offers lower dynamic resistance ( $R_D$ ) than standard ESD diodes.

The Snapback effect combined with improved dynamic resistance leads to a drastic reduction of the clamping voltage.

## PRODUCT TABLE

Part number	Directionality	$V_{TRIG}$ min.	$V_H$ min.	$V_{CL}$ (30 ns after IEC 61000-4-2 8 kV contact)	Maximum peak pulse voltage	Typical line capacitance
ESDZV5-1BF4	Bi-directional	5.8 V	4 V	7 V	18 kV	6 pF
ESDZL5-1F4	Uni-directional	5.8 V	4 V	9.5 V	15 kV	7.5 pF



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