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STGAP2SICSN

Isolated single-channel gate driver for SiC MOSFET

Robust, isolated gate driver for optimal SiC MOSFET control in a narrow body, 8-lead SO package

Designed to optimize the control of SiC MOSFETs, the single-channel STGAP2SiCSN gate driver comes in a space-saving narrow-body SO-8 package and delivers robust performance with accurate PWM control.

As SiC technology becomes widely adopted to boost power-conversion efficiency, the STGAP2SiCSN simplifies designs, saves space, and enhances robustness and reliability in energy-conscious power systems, drives, and controls.

KEY FEATURES & BENEFITS

- Compactness
  - On-chip galvanic isolation
  - Compact SO-8N package
- Robustness
  - Optimized UVLO for SiC MOSFETs
  - Watchdog
  - Transient immunity ±100 V/ns in all temperature range
- Performance
  - High-voltage rail up to 1700 V
  - Up to 26 V supply voltage
  - 4 A sink / source driver current capability
  - Miller clamp and separate output options
  - Propagation delay of 75 ns
  - Stand-by function
  - Interlocking function

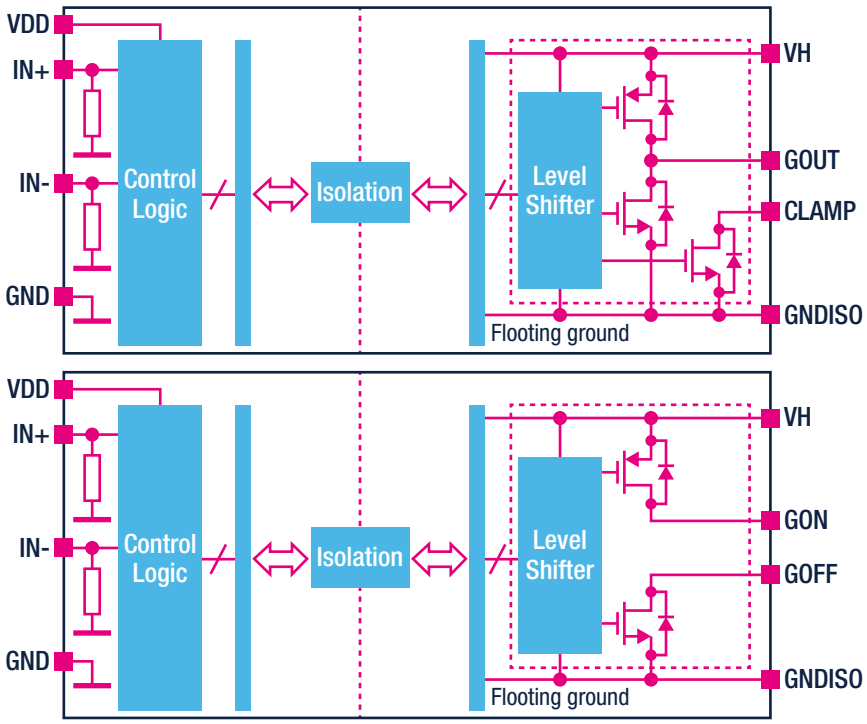
KEY APPLICATIONS

- EV chargers
- Switched mode power supplies
- Motor control
- Factory automation
- Industrial drives and fans
- DC-DC converters
- Uninterruptible power supplies
- Home appliances

Galvanic isolated, single-channel gate driver for SiC FETs in compact SO-8N package

Featuring galvanic isolation between the gate-driving channel and the low-voltage control, the STGAP2SiCSN operates with up to 1700 V on the high-voltage rail. The input-to-output propagation time of less than 75 ns ensures high PWM accuracy, with reliable switching thanks to common-mode transient immunity (CMTI) of ±100 V/ns. Built-in protection includes under-voltage lockout (UVLO), with a threshold tuned to prevent SiC power switches from operating in low-efficiency or unsafe conditions, and thermal shutdown that turns driver output low if excessive junction temperature is detected.
Two optional configurations are available, giving a choice of separate outputs that allow turn-on and turn-off timings to be independently optimized using an external resistor or a single output with active Miller clamp function. The single output configuration enhances stability in high-frequency hard-switching applications, leveraging the Miller clamp to prevent excessive oscillation of the power switch.
The STGAP2SiCSN logic inputs are compatible with TTL and CMOS logic down to 3.3 V, simplifying connections to a host microcontroller or DSP. The driver can sink and source up to 4 A at gate-driving voltage up to 26 V.
The shutdown mode with separate input pin helps minimize system power consumption.
Evaluation boards are available to easily select and modify component values to evaluate driver performance under different application conditions and fine-tune the final application.

STGAP2SICSN block diagrams for Miller clamp and separate output configurations



EVSTGAP2SICSNC

Devices summary

Order code	Description	Package	Packing	Evaluation boards
STGAP2SiCSN	Separate output configurtion	SO-8	Tape and Reel	EVSTGAP2SICSN
STGAP2SiCSNC	Miller clamp configuration			EVSTGAP2SICSNC