

STM32MP21 MPU lines

Optimize performance and power efficiency for industrial IoT applications



Cost-effective STM32MP21x offering efficient performance, low power consumption, strong security, and versatile connectivity

Built on the same architecture as STM32MP25 and STM32MP23, the STM32MP21 offers a single Arm Cortex-A35 core running up to 1.5 GHz and a Cortex-M33 core running up to 300 MHz.

The STM32MP21 lines are optimized for security and connectivity, tailored for edge devices and industrial applications, and offer extended junction temperature tolerance up to 125°C.

ENSURE ROBUST SECURITY AND RELIABLE CONNECTIVITY

- TrustZone® security on both cores, for secure boot and data protection
- SESIP Level 3 target for functional safety in critical industrial applications
- Dual Gigabit Ethernet ports with TSN for deterministic, low-latency communication in smart factory and loT networks
- Multiple industrial interfaces (USB2, dual FDCAN) and MIPI CSI-2 camera interface

REDUCE TIME-TO-MARKET WITH STM32 ECOSYSTEM

- Simplify development and security with OpenSTLinux Distribution,
 Expansion packages and STM32Cube
- Benefit from ST authorized partners for design and integration, reducing project risk
- Baremetal and RTOS flavors coming soon on Cortex-A, complementing existing Cortex-M options
- Choose from multiple RTOS options (FreeRTOS, Zephyr, Px5RTOS) for flexible software development

With STM32MP21, meet security challenges

Strong security for regulatory compliance

Navigate new EU security regulations with STM32MP21 solutions and build devices for the long term: protect users and data, avoid risks and penalties, and reduce costs. ST helps you stay compliant with cryptographic accelerators (AES-128/192/256, SAES with SCA, PKA with DPA protection), extended 5-year maintenance in the OpenSTLinux ecosystem, SESIP and PSA Certified target certifications, and the STM32Trust framework (TF-M, TF-A, OP-TEE).

Resource Isolation Framework (RIF)

This mechanism enables secure isolation of hardware resources such as peripherals, memory regions, and communication interfaces. The RIF

prevents unauthorized use of these resources, limiting the impact of software bugs or attacks to isolated domains. It is designed to support multi-tenant systems, facilitating compliance with stringent security standards while optimizing resource utilization.

Cortex-M33 as trusted domain (M33-TD)

The Cortex®-M33 core can act as the Trusted Domain and dedicated boot processor, integrated into OpenSTLinux. By isolating secure boot functions within its trusted domain, it enhances system security and strengthens protection against attacks, ensuring a robust and reliable boot process.



Dedicated STPMIC2L for power management



STM32MP215C/F block diagram

Arm® Cortex®-A35 1.2GHz / up to 1.5GHz	System	Security	Audio & Analog
L1 32KB I-Cache / 32KB D-Cache 128KB L2 cache NEON TrustZone	Power Supply Regulators	Resource Isolation Framework (RIF)	SPDIF Tx / Rx 4 inputs
	Crystal & Internal oscillators	Octo SPI OTF Decryption	
	Watchdogs (I & W)	DRAM OTF Encryption/Dec	4x SAI
	Cyclic Redundancy Check (CRC)	AES-256 with SCA	
Arm® Cortex®-M33 300MHz	96-bit unique ID		MDF 4 channels / 4 filters
	Up to 123 GPIOs	SHA-256/512, SHA-3, HMAC MDF 4 channels / 4 filters	MDF 4 channels / 4 filters
		PKA ECC/RSA with SCA	2x 12-bit ADC 5 MSPS
16KB I-cache 16KB D-Cache FPU / MPU / NVIC TrustZone	Connectivity	Secure RTC	
	2x 1Gbps ETH w/ TSN EP	Analog true RNG	Temperature sensor
	USB2.0 Host/Dev HS + PHY	12x Tamper pins	
Memory	USB2.0 Host HS + PHY	T°, V, F and 32KHz detection	Timers
	3x SDI04.0 / SD 6.0 / eMMC 5.1		
DDR4 4GB LPDDR4 2GB	1x Octo SPI	Multimedia 2x adv. ctrl + 10x 16-bit	
	16-bit SLC NAND, 8-bit-ECC		2x adv. ctrl + 10x 16-bit timer
DDR3L 1GB Shared RAM 448KB including 128KB Retention RAM	2x FDCAN / TTCAN	24b RGB Disp. 1080p @ 60fps	4x 32-bit timer
	3x I ² C, 3x I ³ C	Camera I/F MIPI CSI-2, 2 lanes	
Backup RAM 8kB / Boot ROM / OTP fuse 12kb	6x SPI, 3x I ² S	Camera I/F 16-bit Parallel	5x 16-bit LP timer
	3x UART, 4x USART	ISP (Camera Pipeline)	

