FIT Rate, FMD and Pin FMA for ALED7709

Introduction

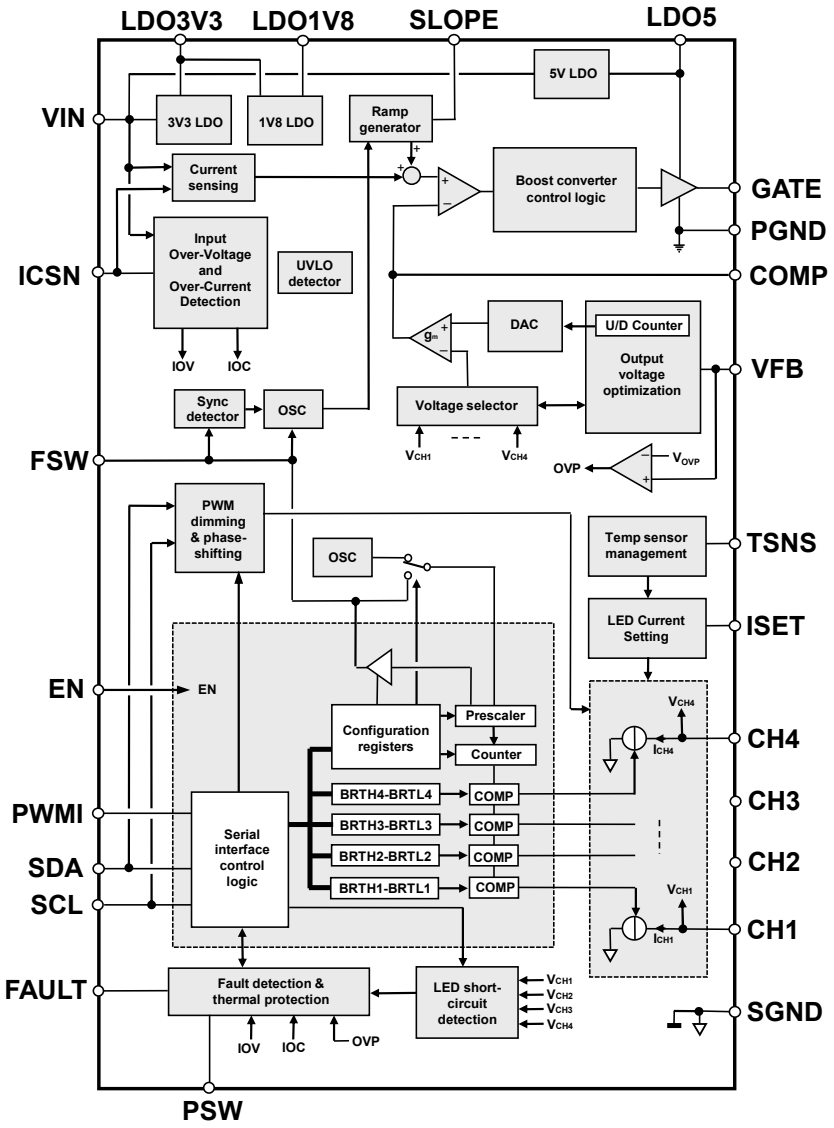
This document contains information related to ALED7709 (QFN24L exposed pad package) to support customers in the design of a functional safety system.

The following information is reported:

- Functional safety Failure In Time (FIT) rates
- Failure Modes with related Distribution (FMD)
- Pin Failure Mode Analysis (Pin FMA)

ALED7709 was not developed in accordance with the IEC 61508 or ISO 26262 standards. However, it was designed using a quality-managed development process.

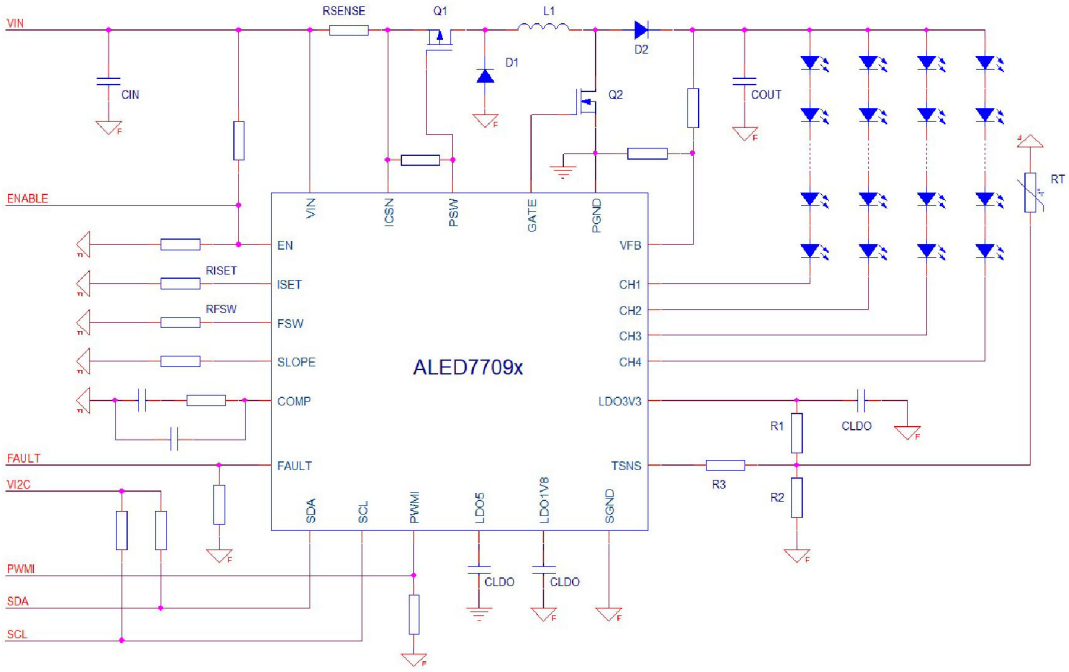
Figure 1. Block diagram



1 Assumptions for the analysis

As the usage conditions affect the metrics, it must be considered that the estimations reported in this document are based on the typical application schematic. The selected value of R_{ISET} is 6.8 kΩ, meaning a maximum channel current of 150 mA. The Boost stage works at 400 kHz supplied with V_{IN} at 12 V and the I^2C pull-ups are connected to 3V3.

Figure 2. Typical application schematic



2 Functional safety Failure In Time (FIT) rates

This section provides the functional safety Failure In Time (FIT) rates for ALED7709 based on two different industry-wide reliability standards:

- Component FIT rates based on Siemens norm SN29500-2 (Table 1)
- Component FIT rates based on IEC TR 62380/ ISO 26262 Part 11 (Table 2)

Table 1. Component FIT rates based on Siemens norm SN29500-2

Table	Category	Ref. FIT (λ_{ref})	Ref. Virtual T_j ($\theta_{vj,1}$)
5	CMOS, BiCMOS (Digital, analog, or mixed)	60	70 °C

The reference failure rate and the virtual junction temperature are taken from SN29500-2 Tables 1 to 5.
The failure rate for operating conditions is computed using the failure rate and virtual junction temperature, following the calculation information in SN29500-2 Section 4.

Table 2. Component FIT rates based on IEC TR 62380/ ISO 26262 Part 11

FIT IEC TR 62380/ ISO 26262	FIT (failures per 10^9 hours)
Die FIT rate	1.9
Package FIT rate	12.4
Total FIT rate	14.3

The failure rate and mission profile information come from reliability modeling for integrated circuits in the reliability data handbook IEC TR 62380/ ISO 26262 Part 1.

- Mission profile: passenger compartment (Table 11)
- Climate type: world-wide (Table 8)
- Power dissipation: 800 mW
- $R_{th(ja)}$: 25.4 °C/W (1) (2)
- Package factor: λ3 (Table 17b)
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

1. *2s2p board as per STD JEDEC spec JESD51-7*
2. *Exposed pad directly soldered to PCB*

3 Failure Mode Distribution (FMD)

In this section of the document, the Failure Mode Distribution (FMD) estimation of ALED7709 is reported.
The analysis has been performed based on the assumptions reported in Section 1.
The estimation is the result of the combination of:

- Common failure modes listed in standards such as IEC 61508 and ISO 26262
- The consideration of sub-circuit function size and complexity
- The best engineering judgment

The failure modes due to random failures and the corresponding distribution are listed in Table 3.
The analysis does not consider any failure events due to overstress or device misuse.

Table 3. Failure Mode and related Distribution (FMD)

Die failure mode	Failure mode distribution [%]
I²C communication fail	2
OUTx out of spec (current)	13
OUTx out of spec (timing)	5
OUTx stuck ON	30
OUTx stuck OFF	40
Fault detection fails: no or false detection	10

4 Pin Failure Mode Analysis (Pin FMA)

This part of the document reports the Failure Mode Analysis for the pins (Pin FMA) of ALED7709.
The typical pin-by-pin failure cases considered are:

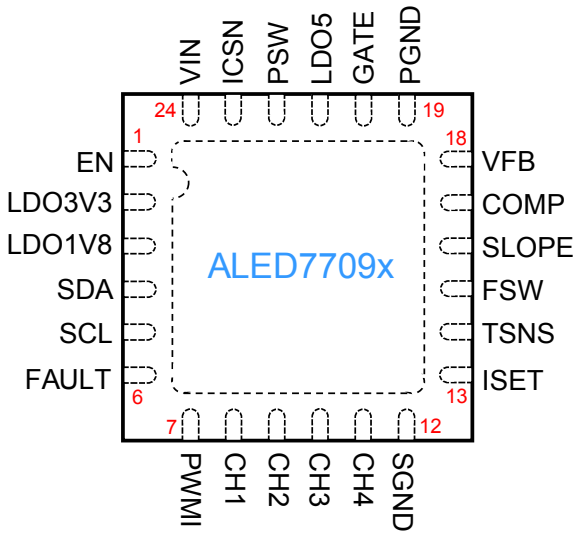
- Pin shorted to ground (GND ≡ SGND ≡ PGND)
- Pin shorted to power supply (V_{IN})
- Pin shorted to an adjacent pin
- Pin open

Table 4 reports the classification of how the considered failure modes affect ALED7709.

Table 4. Classification of failure effects

Class	Failure effect
A	Potential device damage with impact on functionality and performance
B	Loss of functionality, no device damage
C	Performance degradation, no device damage
D	Partial impact on functionality, diagnostic working correctly, no device damage
E	No impact on functionality or performance, no device damage

Figure 3. Pin diagram QFN24L EP



The Pin Failure Mode Analysis (Pin FMA) has been performed with the device running in the typical application as reported in Section 1.

Table 5. Pin Failure Mode Analysis (Pin FMA)

Pin name	Pin #	Failure mode	Failure effect	Classification
EN	1	Shorted to GND	Device always in shutdown	B
		Shorted to VIN	Device cannot enter shutdown	D
		Open	Device always in shutdown	B
		Shorted to LDO3V3	Device cannot enter shutdown	D

Pin name	Pin #	Failure mode	Failure effect	Classification
LDO3V3	2	Shorted to GND	Device cannot start	B
		Shorted to VIN	AMR violation	A
		Open	Wrong regulation, no external capacitor	A
		Shorted to LDO1V8	AMR violation	A
LDO1V8	3	Shorted to GND	Device cannot start	B
		Shorted to VIN	AMR violation	A
		Open	Wrong regulation, no external capacitor	A
		Shorted to SDA	MCU cannot control the device and AMR violation	A
SDA	4	Shorted to GND	MCU cannot control the device	B
		Shorted to VIN	AMR violation	A
		Open	MCU cannot control the device	B
		Shorted to SCL	MCU cannot control the device	B
SCL	5	Shorted to GND	MCU cannot control the device	B
		Shorted to VIN	AMR violation	A
		Open	MCU cannot control the device	B
		Shorted to FAULT	MCU cannot control the device	B
FAULT	6	Shorted to GND	No FAULT indication	A
		Shorted to VIN	AMR violation	A
		Open	No FAULT indication	D
PWMI	7	Shorted to GND	PWMI control not working	B (1)
		Shorted to VIN	AMR violation	A
		Open	PWMI control not working	B (1)
		Shorted to CH1	AMR violation when CH1 is OFF	A
CH1	8	Shorted to GND	Initial FAULT detected, if OUT is forced ON, device detects OPEN Fault	D
		Shorted to VIN	Initial FAULT detected, if OUT is forced ON, device detects SHORT Fault	D
		Open	If OUT is active, device detects OPEN Fault	D
		Shorted to CH2	Mixed out functionality	D (2)
CH2	9	Shorted to GND	Initial FAULT detected, if OUT is forced ON, device detects OPEN Fault	D
		Shorted to VIN	Initial FAULT detected, if OUT is forced ON, device detects SHORT Fault	D
		Open	If OUT is active, device detects OPEN Fault	D
		Shorted to CH3	Mixed out functionality	D (2)
CH3	10	Shorted to GND	Initial FAULT detected, if OUT is forced ON, device detects OPEN Fault	D
		Shorted to VIN	Initial FAULT detected, if OUT is forced ON, device detects SHORT Fault	D
		Open	If OUT is active, device detects OPEN Fault	D
		Shorted to CH4	Mixed out functionality	D (2)
CH4	11	Shorted to GND	Initial FAULT detected, if OUT is forced ON, device detects OPEN Fault	D

Pin name	Pin #	Failure mode	Failure effect	Classification
CH4	11	Shorted to VIN	Initial FAULT detected, if OUT is forced ON, device detects SHORT Fault	D
		Open	If OUT is active, device detects OPEN Fault	D
		Shorted to SGND	Initial FAULT detected, if OUT is forced ON, device detects OPEN Fault	D
SGND	12	Shorted to GND	Correct operation	E
		Shorted to VIN	Device cannot work	B
		Open	Device cannot work	A
ISET	13	Shorted to GND	Channels current out of control	C
		Shorted to VIN	AMR violation	A
		Open	Channels current out of control	C
		Shorted to TSNS	Channels current out of control, NTC not operative	B
TSNS	14	Shorted to GND	Maximum current reduction	B (1)
		Shorted to VIN	AMR violation	A
		Open	NTC control not working	B (1)
		Shorted to FSW	Switching frequency modified, NTC not operative	B (1)
FSW	15	Shorted to GND	Local oscillator not working	B (1)
		Shorted to VIN	AMR violation	A
		Open	Local oscillator not working	B (1)
		Shorted to SLOPE	DC-DC converter loop is affected	B
SLOPE	16	Shorted to GND	DC-DC converter loop is affected	B
		Shorted to VIN	AMR violation	A
		Open	Compensation loop not properly adjusted	C
		Shorted to COMP	DC-DC converter loop is affected	B
COMP	17	Shorted to GND	DC-DC controller cannot start	B
		Shorted to VIN	AMR violation	A
		Open	DC-DC controller loop is unstable	C
		Shorted to VFB	DC-DC controller loop is affected	B
VFB	18	Shorted to GND	Output voltage is pushed up to overvoltage protection	B
		Shorted to VIN	AMR violation	A
		Open	DC-DC is uncontrolled, output voltage could be pushed up to overvoltage protection	B
PGND	19	Shorted to GND	Correct operation	E
		Shorted to VIN	Device cannot work	B
		Open	Device cannot work	A
		Shorted to GATE	DC-DC converter cannot work	A
GATE	20	Shorted to GND	DC-DC converter cannot work	A
		Shorted to VIN	AMR violation	A
		Open	DC-DC converter cannot work	B
		Shorted to LDO5	NMOS always ON	B
LDO5	21	Shorted to GND	Device cannot work	B
		Shorted to VIN	AMR violation	A

Pin name	Pin #	Failure mode	Failure effect	Classification
LDO5	21	Open	Wrong regulation, no external capacitor	A
		Shorted to PSW	LDO5 can go above AMR, PMOS always ON	A
PSW	22	Shorted to GND	PMOS always ON	B
		Shorted to VIN	PMOS always OFF	B
		Open	PMOS always OFF	B
		Shorted to ICSN	PMOS always OFF	B
ICSN	23	Shorted to GND	Device cannot work	B
		Shorted to VIN	R_{SENSE} is shorted, peak current mode controller is stuck	B
		Open	Peak current mode controller is stuck	B
VIN	24	Shorted to GND	Device cannot work	B
		Shorted to VIN	Correct operation	E
		Open	Device cannot work	B

1. *Classification is related to pin enabled by register configuration, otherwise the classification is E.*
2. *Shorted outputs is a possible working condition. If voluntarily shorted, the classification is E.*

Revision history

Table 6. **Document revision history**

Date	Version	Changes
19-Jun-2026	1	Initial release.

Contents

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