

Voltage Translator for STLINK-V3MODS

Reference Design

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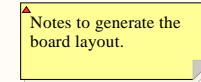
Sheet 1 : Project Overview
Sheet 2 : Voltage translator Part1 (SPI / GPIO)
Sheet 3 : Voltage translator Part2 (USART / CAN / I2C / JTAG SWD)

Legend

General comment such as function title, configuration, ...

Text to be added to silkscreen.

Warning text.



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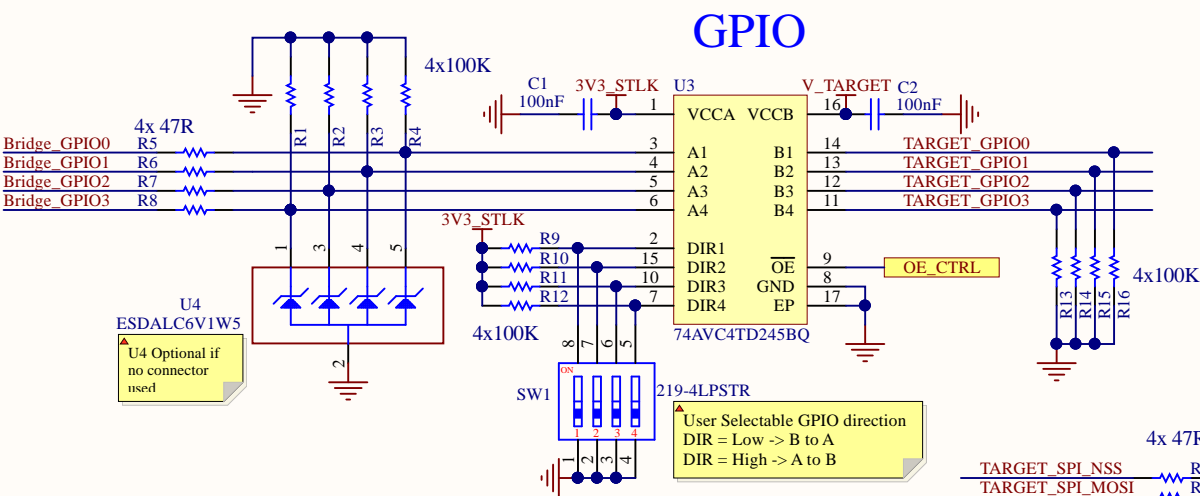
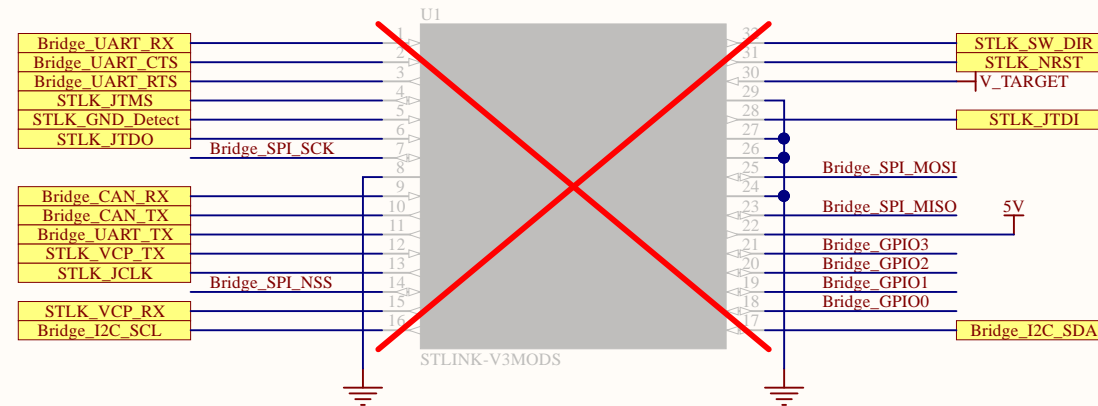
Title: Project overview		
Project: Voltage Translator for STLINK-V3MODS		
Variant: DEFAULT		
Revision: A-01		Reference: N/A
Size: A4	Date: 28-OCT-2021	Sheet: 1 of 3



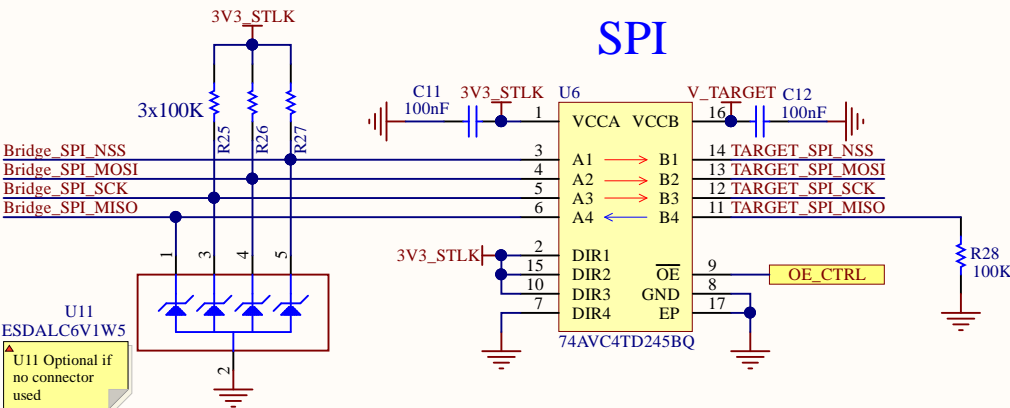
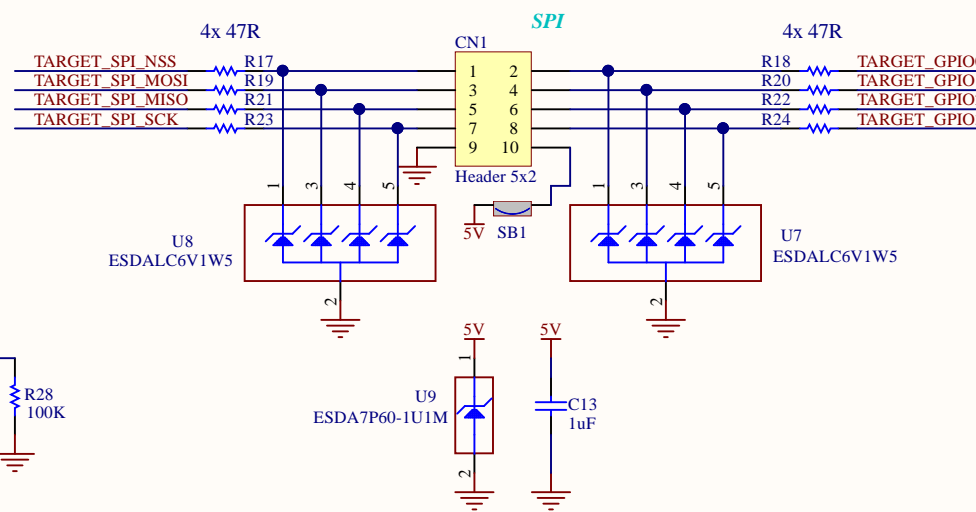
Voltage Translator for STLINK-V3MODS

Target voltage range 1.65V-3.6V, ST-Link voltage 3.3V

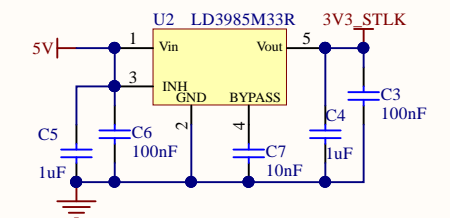
STLINK-V3MODS module



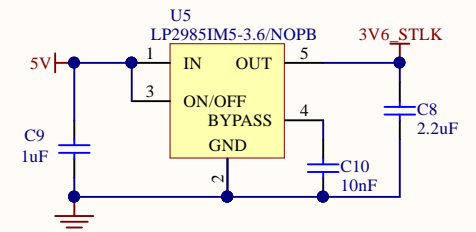
TARGET Side Connectors



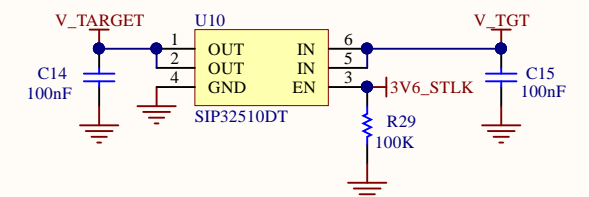
3V3 for ST-LINK Side Only



3V6 for I2C Level Shifter



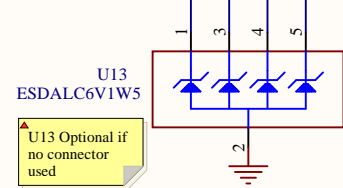
V_TGT to V_TARGET Switch enabled by 3V6_STLK



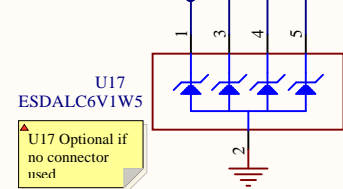
Voltage Translator for STLINK-V3MODS

Target voltage range 1.65V-3.6V, ST-Link voltage 3.3V

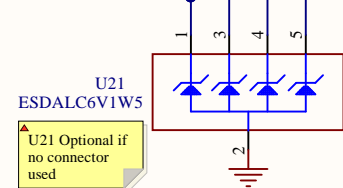
Bridge_UART_CTS
Bridge_UART_TX
Bridge_UART_RX
Bridge_UART_RTS



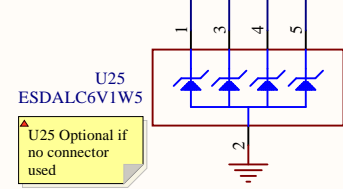
Bridge_I2C_SDA
Bridge_I2C_TX
Bridge_CAN_RX
Bridge_I2C_SCL



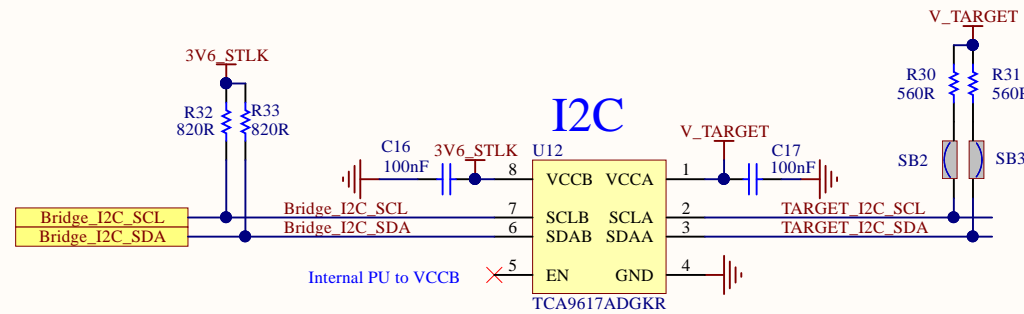
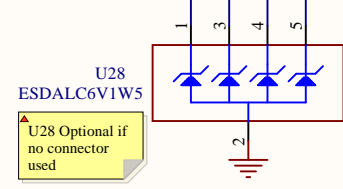
STLK_VCP_TX
STLK_NRST
STLK_JTDI
STLK_JTDO



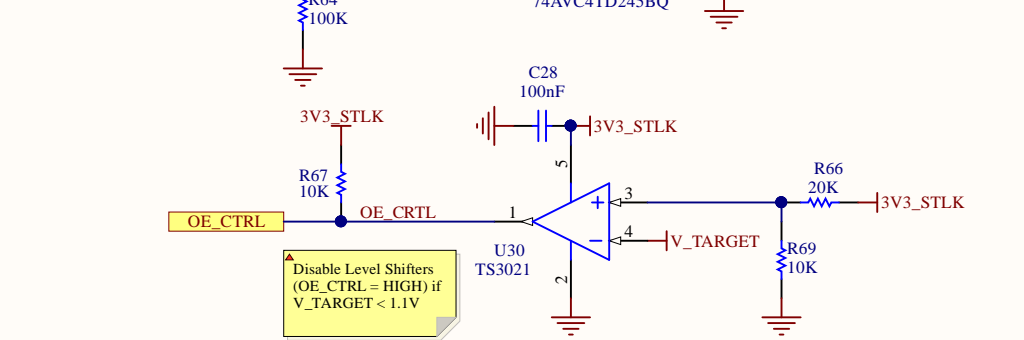
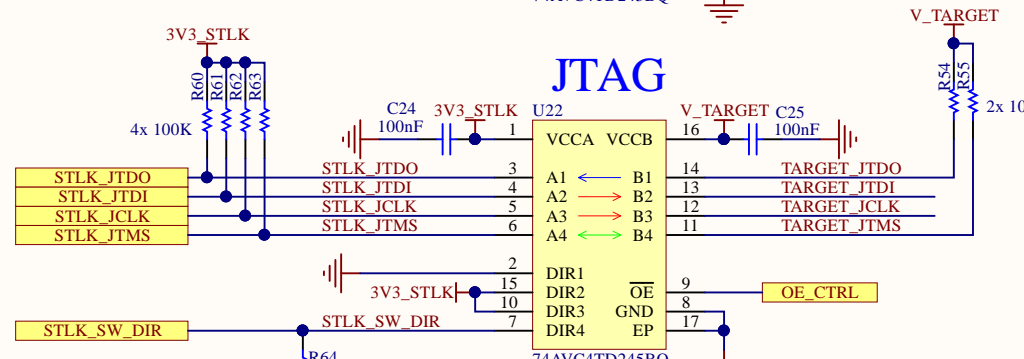
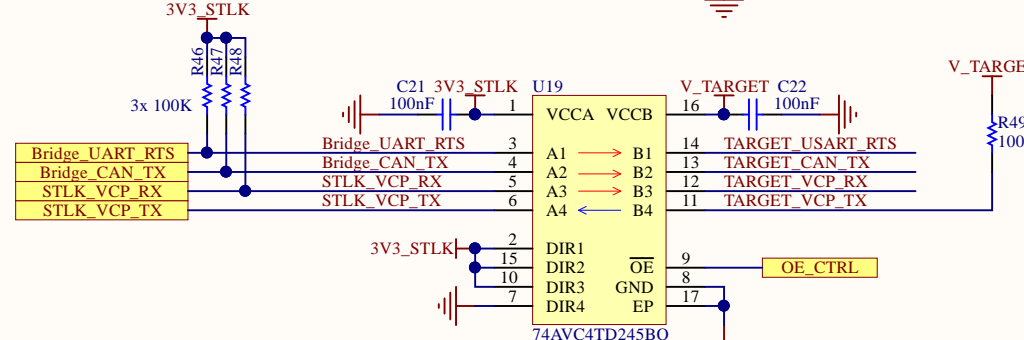
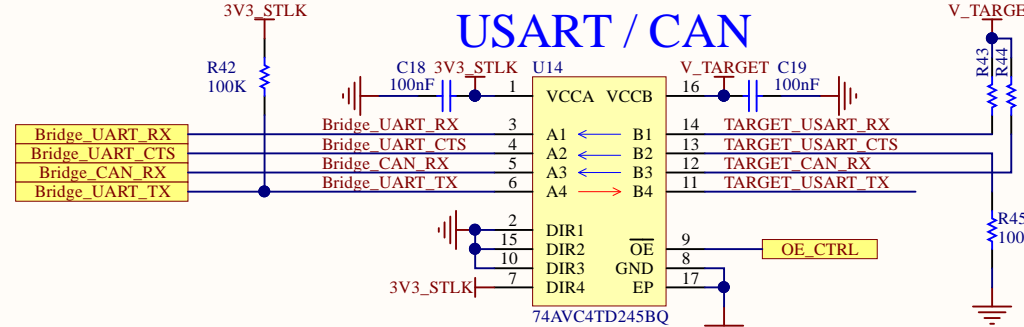
STLK_SW_DIR
STLK_JTMS
STLK_JCLK



STLK_GND_Detect
STLK_VCP_RX

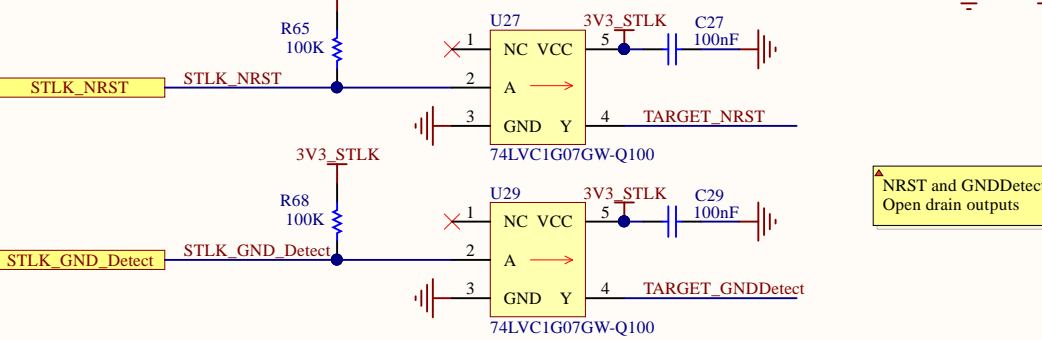
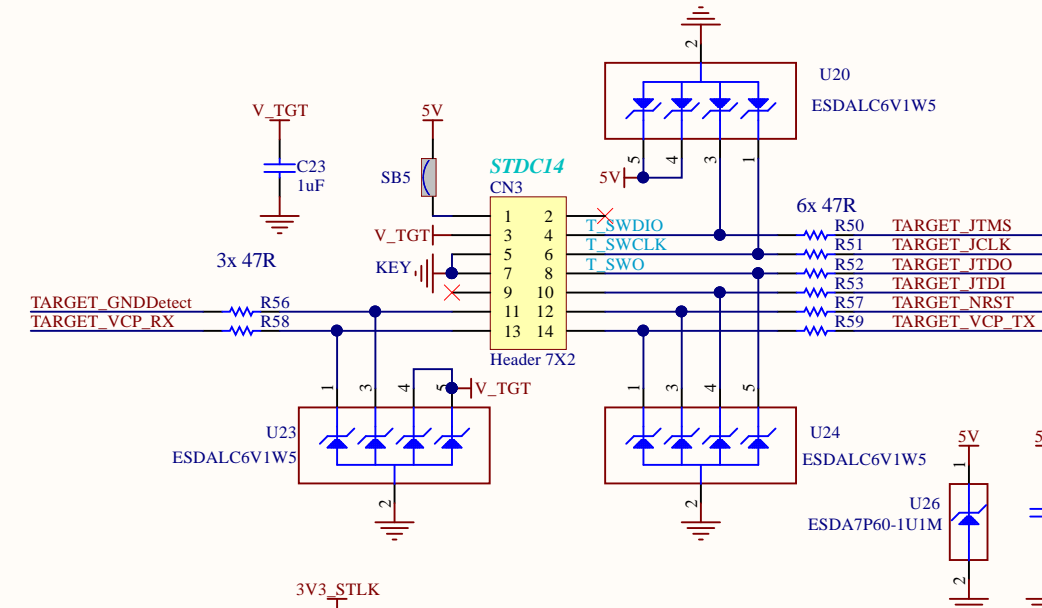
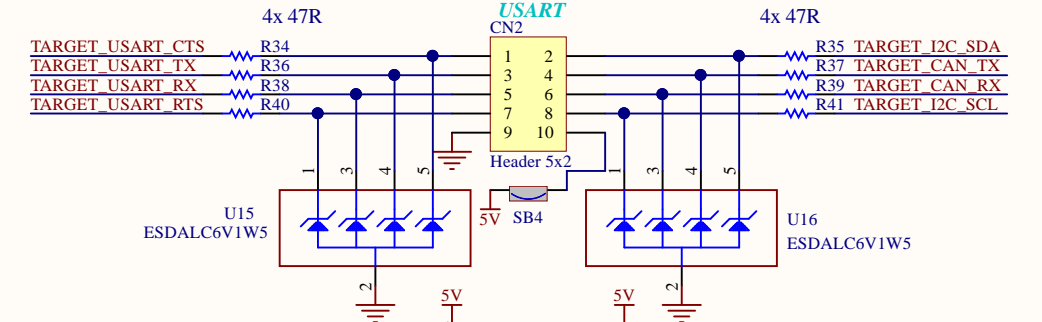


VCCB should always be higher than VCCA. VCCB cannot be lower than VCCA even when the device is disabled. During power-up, VCCB must rise before VCCA



Disable Level Shifters (OE_CTRL = HIGH) if V_TARGET < 1.1V

TARGET Side Connectors



NRST and GNDDetect are Open drain outputs