Multi-Optical Network on Chip for Large Scale MPSoC

***Abstract*—Optical Network on Chip (ONoC) architectures are emerging as promising contenders to solve bandwidth and latency issues in MPSoC. However, current optical interconnect on-chip integration technologies allows to interconnect only dozens of IPs. Scaling with MPSoCs composed by hundreds of IPs thus relies on unpredictable technological innovations. In this work, we propose a method combining multiple ONoCs. Each ONoC is small enough to rely on already existing and proved technologies. We evaluate the approach on various interconnect scenarios, showing that it allows scaling with large MPSoC architectures.**

I. INTRODUCTION

The shift to very high performance distributed Multi-Processor Systems-on-Chip (MPSoC) as mainstream computing devices is the recognized route to reach the execution performances required for future date intensive applications [2]. MPSoC require high-speed communication between processors, which clearly relies upon the existence of an extremely fast and flexible interconnect network. Optical Networks on Chip (ONoC) overcome the limitations of electrical interconnect through the use of Wavelength Division Multiplexing (WDM) [9], which allows concurrently transmitting multiple optical signals on a same waveguide. However, the reliability of such optical communication is mainly driven by the laser output power and the coupling losses occurring in optical switches. Thus, the scalability of the ONoC relies on technological advances in optical on-chip interconnect.

In this paper, we propose to interconnect large scale MPSoC through Multi-ONoC. The method we propose divides a large, not feasible, ONoC into multiple but smaller ONoCs. In the resulting Multi-ONoC architecture, each ONoC is reliable, since it satisfies the specified technological constraints. As drawbacks, extra-electrical routing is required and the number of waveguides increases, leading to a more complex layout on the optical layer.

Several contributions address ONoC design exploiting both electrical and optical NoC technologies. An approach using electrical interconnects for control flow and optical interconnects for data flow was proposed in [4]. In this architecture, the optical signal is preceded by an electrical control signal in charge of reserving the optical path. However, optical communications may be delayed until optical path becomes free, resulting in important contention delay. The same observation is made for the fat tree and the mesh ONoC proposed in [5] and [6] respectively. Compared to these works, the ONoC we are considering is totally contention free. In [3], electrical interconnects manage local communication, while an optical interconnect is responsible for global communications. However, the chosen ring topology implies that each wavelength flowing through the ONoC must be assigned to a given optical network interface, avoiding parallel communications through the same wavelength. Our architecture does not suffer from this inconvenient since the used topology allows parallel communications even using same wavelength.

Section II presents the single ONoC-based architecture and introduces optical on-chip integration technological constraints. Section III presents the Multi-ONoC architecture scaling with large MPSoC systems. In section IV, we present our method defining feasible Multi-ONoC architecture starting from a non-feasible single ONoC-based architecture and we give the experimental results. Section V concludes the paper.

II. SINGLE ONOC ARCHITECTURE

An ONoC interconnects a set of computing and storage resources that are both considered as IPs in the remaining of the paper. ONoC interconnects the IPs according to a binary IP connectivity matrix: a *1* means that a communication is possible from a source IP to a target IP. In the connectivity matrix illustrated in Figure 1 a), 8 IPs are considered and each IP can communicate with all others IPs, except with itself. Others connectivity are possible (e.g. to interconnect a set of processors to a set of memories), as it will be discussed in the experimental results section. Each IP is connected to the ONoC through Optical Network Interface (ONI) which perform electro-optical and opto-electrical conversions. ONI can communicate simultaneously with one or several other ONIs through passive photonic routing structure, so-called λ-router. A communication through the ONoC (i.e. from a source ONI to a target ONI) is performed in three stages: (a) the source ONI converts the data to transmit into an optical signal; (b) the optical signal is routed through the λ-router and (c) the target ONI converts the optical signal into an electrical signal.

The λ-router network consists of N stages of *optical switches*. Each stage is composed of optical switches characterized by a same resonant wavelength and linked through *waveguides*. The waveguides transmit optical signals and the optical switches manage routing of signals into these waveguides. Optical switches realize the key functionality of selecting and redirecting an input signal based on its wavelength. The path followed by the optical signal in the λ-router depends only on the wavelength. WDM technique is used: when multiple signals of various wavelengths are injected at the input, a cumulative state occurs, where individual signals simultaneously obey the routing characteristics of the optical switch according to their individual wavelengths. Because of this property, a contention-free ONoC can be built.

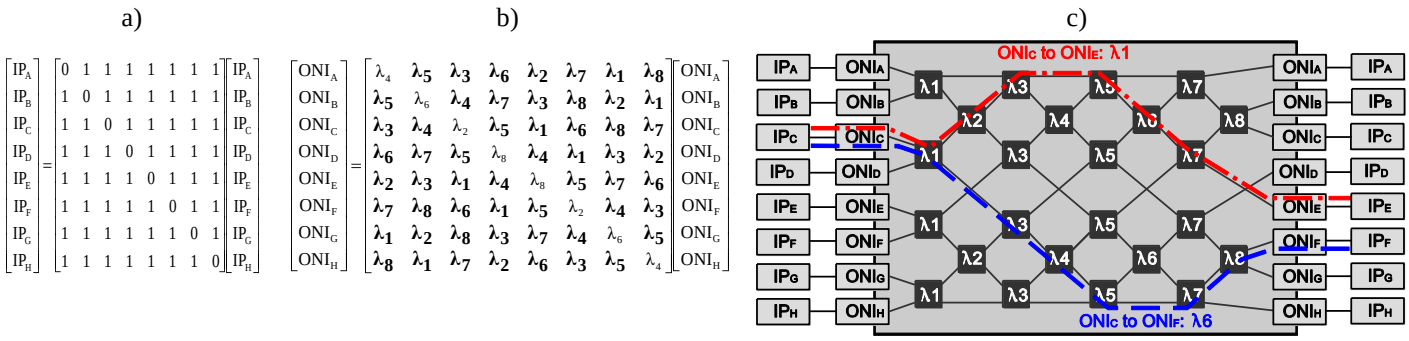

Figure 1 ONoC a) IP connectivity matrix, b) wavelength matrix and b) topology schematic.

Only one physical path associated with a single wavelength exists between a source ONI and a target ONI. The wavelength to be used for each communication is specified in a wavelength matrix. Since this matrix is for a full connectivity between all ONIs, it is superposed to the desired connectivity matrix. Figure 1 b) represents the initial wavelength matrix for an ONoC of 8 ONIs and, in bold, the useful connections to realize the connectivity specified in Figure 1 a). For instance, communications from ONI_C to ONI_E and from ONI_C to ONI_F are respectively realized through the wavelengths λ_1 and λ_6. From these connections, the ONoC is build following the reduction method proposed in [7]. This method adapts ONoC from a given IP connectivity scenario and reduces the implementation complexity of the optical interconnect by suppressing useless optical switches. The resulting ONoC is illustrated in Figure 1 c). The communication path used to realize the communications from IP_C to IP_E and from IP_C to IP_F are illustrated.

The ONoC design feasibility and efficiency is constrained by the propagation losses occurring in the passive photonic components. For current technology, optical switches and waveguides respectively introduce 0.3dB and 2dB/cm losses. To achieve acceptable communications bit error rate, the number of Optical Switches Crossed (nOSC) and the length of waveguides must be limited accordingly to the output power provided by laser source. For instance, a proposed integrated laser output power is around 2.5µW/µm^2 [8], which would make possible to cross 48 optical switches and 1cm waveguide. This allows to fully interconnecting 48 IPs. However, interconnecting hundreds of IPs through a single ONoC relies on unpredictable advances in optical on-chip interconnect integration technologies. The next section presents methodology scaling with large optical interconnect according to already existing and proved technologies.

III. MULTI-ONOC ARCHITECTURE

In order to interconnect large MPSoC with current optical on-chip interconnect integration technologies, multiple (feasible) ONoCs can be combined. The considered architecture, illustrated in Figure 2, is composed by a set of IPs interconnected to Multi-ONoC through Electrical Network Interfaces (ENIs). Each ONoC manages part of the connections specified in the IP connectivity matrix. As a consequence, the packets routing is realized in three steps: (1) electrical routing from a source IP to the relevant ONoC (based on the target IP address), (2) optical routing through the ONoC and (3) electrical routing from the ONoC to the target IP. Electrical routing is realized by address decoder components.

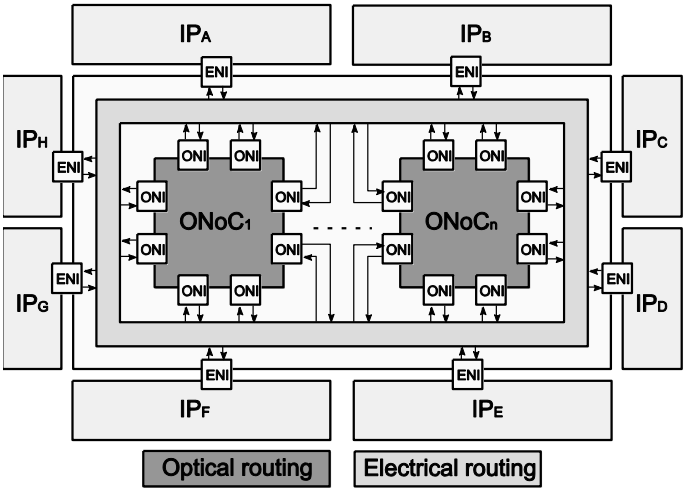

Figure 2 Multi-ONoC architecture interconnecting 8 IPs through *n* ONoCs.

To design feasible Multi-ONoC, the connections specified in the IP connectivity matrix are distributed so that ONoCs manage an equivalent number of wavelengths. Indeed, in ONoC, each stage of the λ-router is associated to a wavelength. By supporting only part of wavelengths, only part of stages is necessary and nOSC can be reduced. For this purpose, the reduction method described in section II is used to reduce the size of each ONoC.

To illustrate the approach, we consider the example illustrated in Figure 1 a), where multiple ONoCs are used to interconnect 8 IPs according to the connectivity matrix. For the 2-ONoCs scenario, $ONoC_1$ manages the connections using λ_1, λ_2, λ_3 or λ_4 and $ONoC_2$ manages the connections using λ_5, λ_6, λ_7 and λ_8. The resulting connectivity matrix and Multi-ONoC architecture are illustrated in Figure 3. Because they use wavelengths λ_1 and λ_7, IP_C to IP_E and IP_C to IP_F communications are realized by different ONoCs. Compared to the reference scenario (i.e. the single ONoC scenario illustrated in Figure 1), the nOSC decreases from 7 (e.g. IP_G to IP_B communication) to 4 (e.g. IP_H to IP_C communication). This improvement helps satisfying design constraints. As drawbacks, the number of required waveguides increases and address decoder are necessary. This leads to additional constraints in the layout and additional latencies in communications.

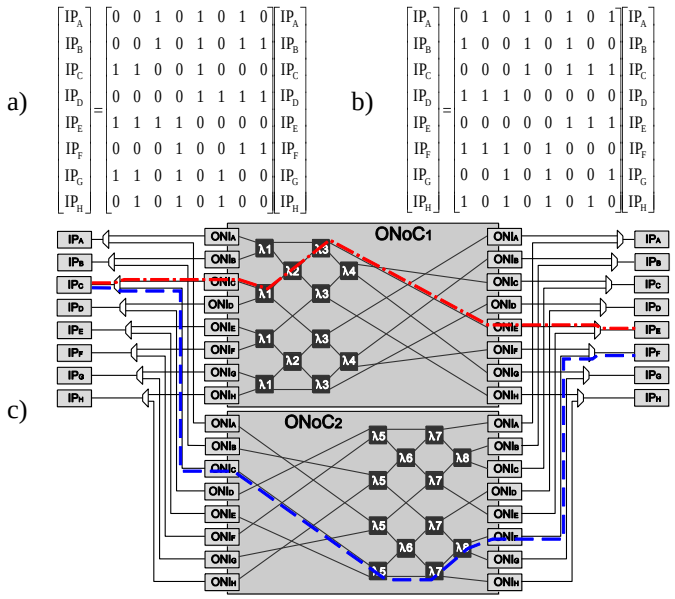

Figure 3 a) $ONoC_1$ and b) $ONoC_2$ connectivity matrixes and c) the resulting Multi-ONoC architecture

Figure 4 illustrates the impact of the number of waveguides on the layout, using a simple example: 4 IPs interconnected through a) one ONoC and b) two ONoCs scenarios. The ONoCs schematic views are illustrated on the left-hand side of Figure 4 and possible layouts are represented on the right-hand side. In case a), the layout can be made so that the 4 waveguides never cross each other. In case b), the layout is more complex and the 8 waveguides necessarily cross each other, resulting in additional coupling losses. Without optimization, the coupling loss per crossing is comparable to the loss occurring in optical switches (i.e. 0.3dB). However, geometric optimization of each crossing using parabolic tapers designed around a 1.55µm wavelength as explored in [10] reduces the loss to the order of 0.05dB at the expense of area (each crossing has a footprint of the order of $10x10\mu m^2$). While difficult to achieve within the λ-router structure, this technique can be applied outside such that the accumulated losses will remain lower for the two ONoCs scenario.

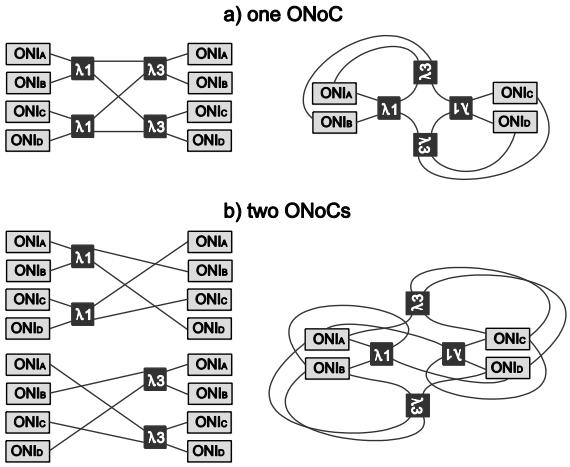

Figure 4 Schematic view and layout for a) one ONoC and b) two ONoCs scenarios

Experimental results for 1, 2, 4 and 8 ONoCs scenarios interconnecting 8 IPs are given in TABLE I. Basically, when the number of ONoCs is increased, the nOSC decreases and the number of waveguides increases. The following section details the proposed methodology used to define the number of ONoCs satisfying the design constraints, while minimizing the layout complexity drawback.

TABLE I. COMPARISON BETWEEN PERFORMANCE METRICS FOR VARIOUS NUMBER OF ONOCS

Number of ONoCs	**1**	**2**	**3**	**4**	**8**
Number of waveguides	8	16	24	32	56
nOSC	8	4	3	2	1

IV. METHOD AND EXPERIMENTAL RESULTS

A. *Method*

The Multi-ONoC generation method is given in Algorithm 1. As an initial configuration, the number of ONoCs is set to one since it maximizes WDM benefits. The inputs of the method are a connectivity matrix for N IPs and the maximum tolerated nOSC (which is given by technological constraints). In step 3, the used set of wavelengths WL is equitably distributed to the ONoCs. From this distribution, in step 4, the connectivity of each ONoC is obtained and the reduction method is called in order to suppress the useless optical switches, as discussed in section II. The maximum nOSC of the resulting ONoCs is compared to the tolerated nOSC. In case the constraint is satisfied, the Multi-ONoC configuration is validated and the process terminates. Otherwise, the number of ONoCs increases and the process is repeated. Two sets of experiments are conducted to evaluate the benefits of the method.

Algorithm 1: Multi-ONoC generation

1. Set the number of ONoC to 1.
2. Get the tolerated nOSC and the connectivity matrix from user.
3. Equitably distribute wavelength $wl_i \in WL$ to the ONoCs.
4. For each ONoC, generate the connectivity matrix and call the reduction method.
5. Set nOSC as the maximum nOSC of all the resulting ONoCs.
6. If nOSC satisfies the design constraint, validate the Multi-ONoC and exit; else, increment the number of ONoC and go to step 3.

B. *Experimental Results*

In the first experiment, we evaluate how the method contributes to realistically interconnect large scale MPSoC with today optical interconnect on-chip integration technologies. For this purpose, the connectivity matrix is filled so that 128, 256 and 512 IPs are fully interconnected and the maximum tolerated nOSC is set to 48. Results are illustrated in Figure 5. Obviously, the number of required ONoCs increases with the number of interconnected IPs: interconnecting 128, 256 and 512 IPs respectively requires 3, 6 and 11 ONoCs to satisfy the design constraint. The number of required waveguides linearly increases with the number of required ONoCs.

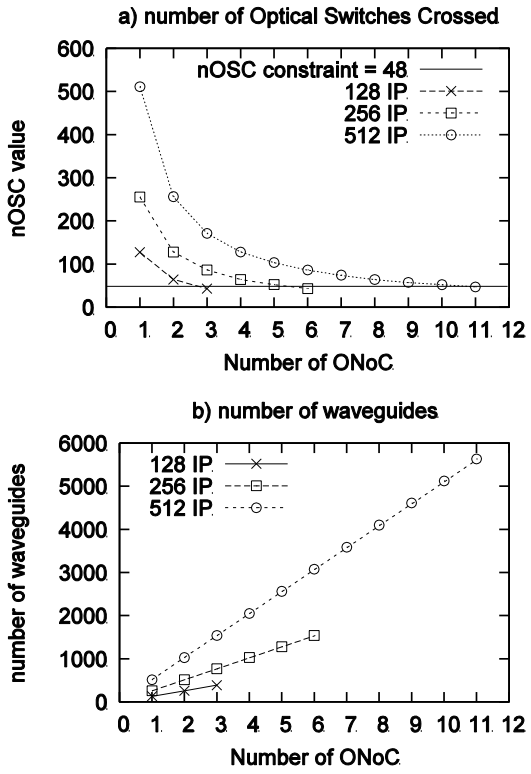

Figure 5 Sscalability of the method: a) nOSC and b) number of waveguides

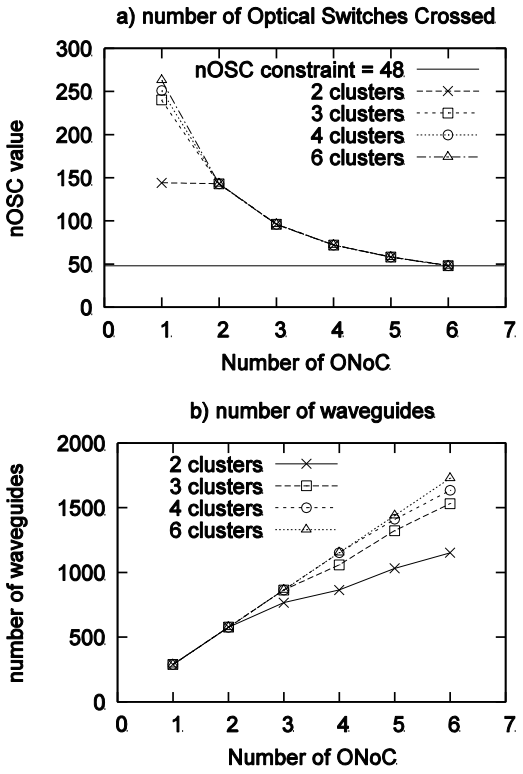

Figure 6 Efficiency of the method for interconnecting 288 clustered IPs: a) nOSC and b) number of waveguides

In the second experiment, various connectivity matrixes are evaluated. They represent realistic scenarios where sets of IPs are clustered so that they do not need to communicate each other through the ONoC. Such scenarios occur, for instance, interconnecting a cluster of processors to a cluster of memories: only the communications between processors and memories are necessary. Depending on the number of clusters, the number of connections in the connectivity matrix will vary. To evaluate our method for such architectures, 288 IPs are equitably distributed to 2, 3, 4 and 6 clusters. According to Figure 6, 6 ONoCs are necessary to satisfy the design constraint. As a main result, our method effectively reduces the nOSC for all the considered number of clusters (the only exception comes from the 2 clusters architecture which is already strongly optimized for one ONoC). The number of waveguides required to implement the Multi-ONoC depends on the number of clusters. Therefore, 6 ONoCs are required for all the considered architecture configurations, the complexity (given by the number of waveguides) is reduced with the number clusters.

V. CONCLUSIONS

The proposed methodology enables overcoming an important challenge faced by designers of ONoC-based MPSoCs: interconnecting a large number of IPs using optical networks is infeasible because of the current technological constraints. At the acceptable price of extra waveguides and electrical routing, the proposed method reduces the number of Optical Switches Crossed (nOSC) responsible for propagation losses, until satisfying technological constraints.

REFERENCES

[1] A. Kazmierczak *et al.*, "Design, simulation, and characterization of a passive optical add-drop filter in silicon-on-insulator technology," *IEEE Photon. Technol. Lett.*, vol. 17, no. 7, pp. 1447-9, July 2005.

[2] ITRS. International Technology Roadmap for Semiconductors. [Online]. Available: http://public.itrs.net/

[3] S. Pasricha and N. Dutt. ORB: An On-Chip Optical Ring Bus Communication Architecture for Multi-Processor Systems-on-Chip. In proceedings of ASP-DAC, 2008. pp. 789-794.

[4] A. Shacham et al.. Photonic Networks-on-Chip for Future Generations of Chip Multiprocessors. IEEE Transactions on Computers, Vol. 57, number 9, 2008. pp. 1246-1260.

[5] H. Gu, W. Zhang and J. Xu. A Low-power Fat Tree-based Optical Network-on-Chip for Multiprocessor System-on-Chip. In proceedings of DATE, 2009.

[6] H. Gu, J. Xu and Z. Wang. A Novel Optical Mesh Network-on-Chip for Gigascale Systems-on-Chip. In proceedings of APCCAS, 2008.

[7] I. O Connor, F. Mieyeville, F. Gaffiot and G. Nicolescu. Reduction Methods for Adapting Optical Network on Chip Topologies to Specific Routing Applications. In proceedings of Design of Circuits and Integrated Systems, Grenoble, 2008.

[8] Thijs Spuesens et al.. Improved Design of an InP-Based Microdisk Laser Heterogeneously Integrated with SOI. In 6th IEEE International Conference on Group IV Photonics (GFP), San Francisco, Sep. 2009.

[9] G. Rouskas. Routing and Wavelength Assignment in Optical WDM Networks. Wiley Encyclopedia of Telecommunications, 2001.

[10] T. Fukazawa et al.. Low loss intersection of Si photonic wire waveguides, Jap. J. Appl. Phys. 43(3), pp. 646-647, 2004.