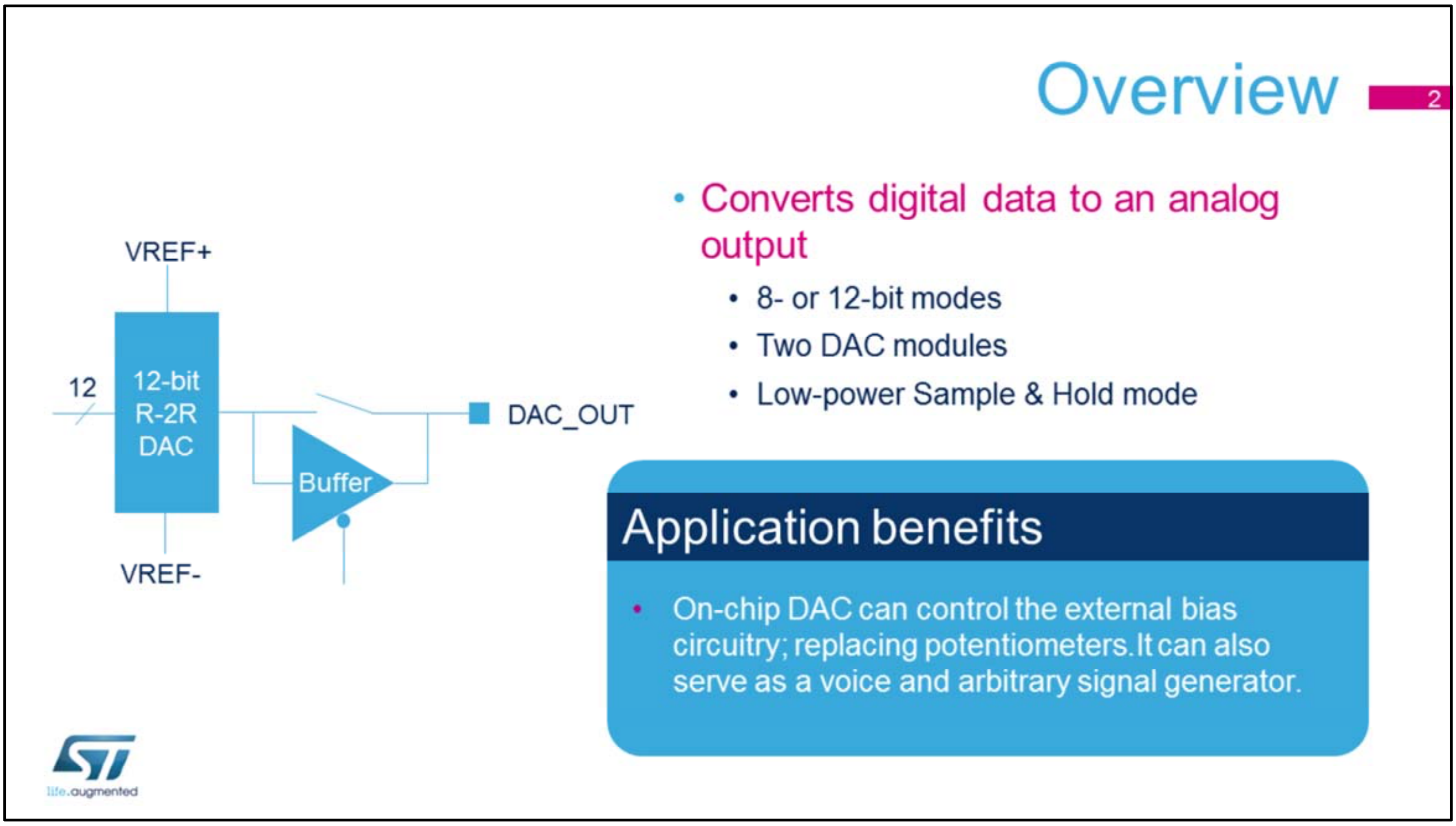
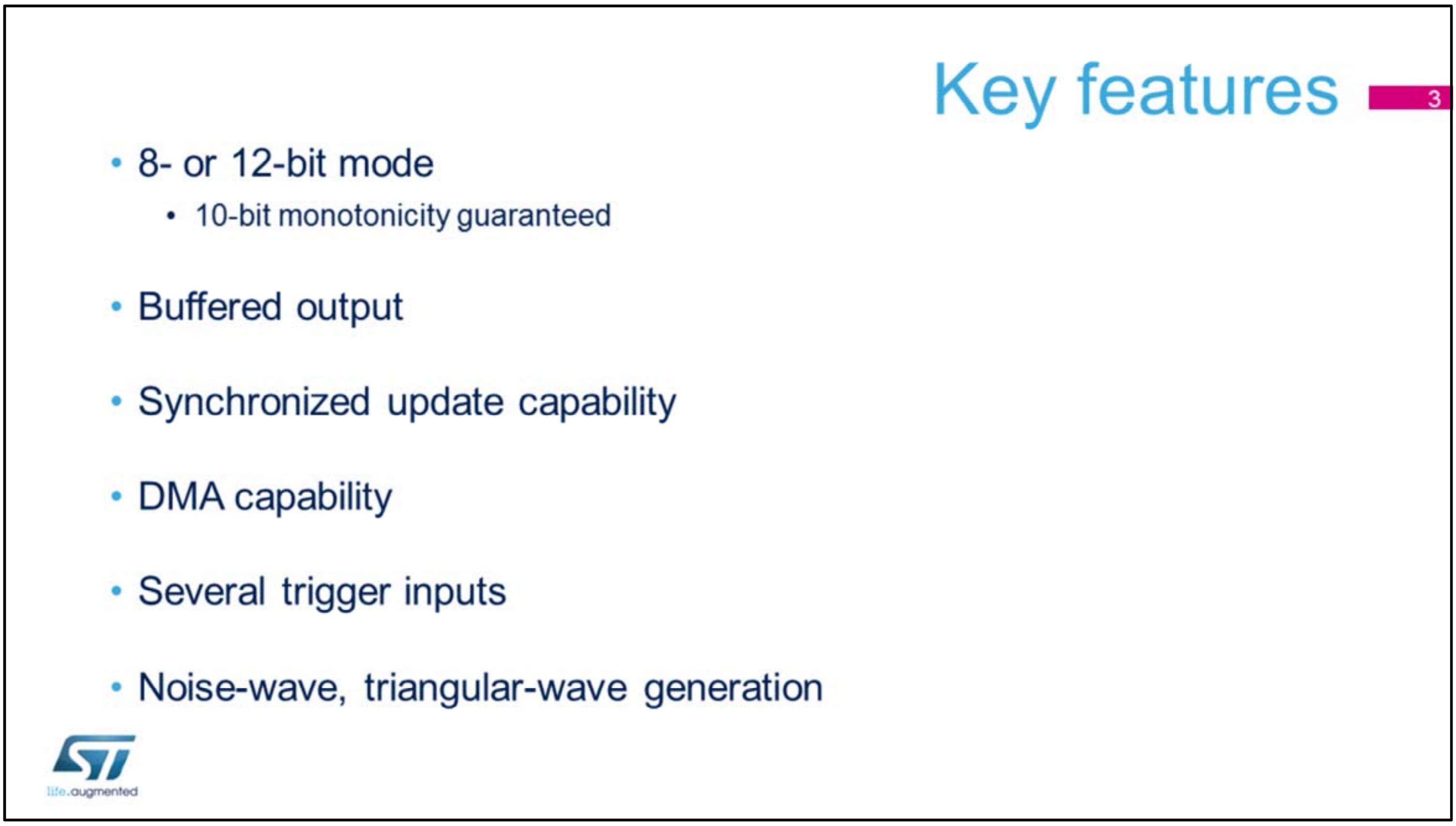
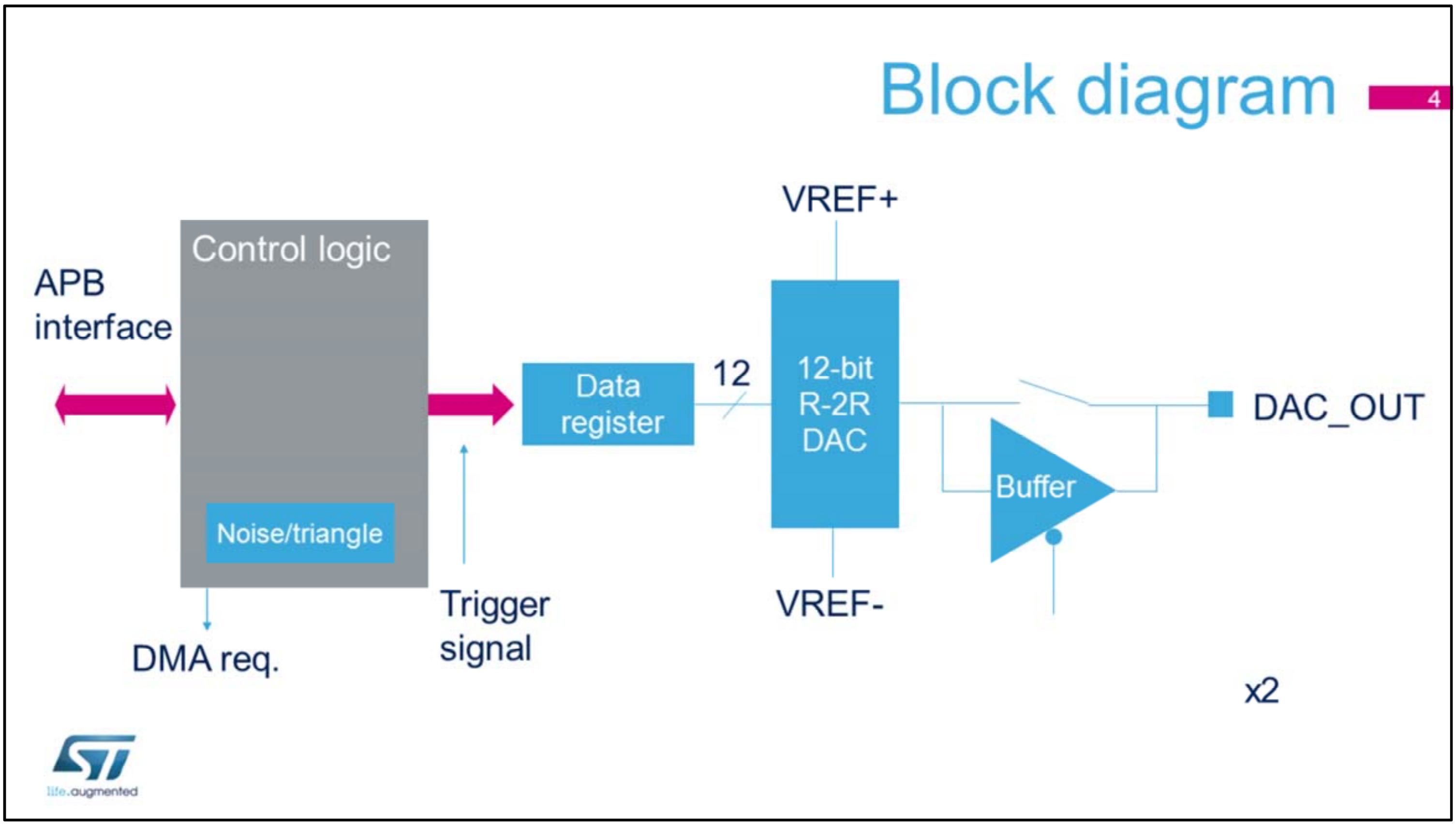
Hello, and welcome to this presentation of the STM32F7 digital-to-analog converter. This block is used to convert digital signals to analog voltages which can interface with the external world.



The STM32F7 digital-to-analog converter converts 8- or 12-bit digital data to an analog voltage. Two DAC modules are embedded in the STM32F7.
The DAC can interface with external pots or bias circuitry. It can also create voice and arbitrary signals.



The digital-to-analog converter inside STM32F7 products offers simple digital-to-analog conversion in an 8- or 12-bit mode; 10-bit monotonicity is guaranteed. The DAC output can have a low impedance buffer to drive external loads. Two DACs can be synchronized with each other. The input data can be transferred by DMA which offloads the CPU. The DAC output data can be updated by a timer or an external trigger as well as a software trigger. It also integrates small logic to generate noise waves as well as triangle waves.

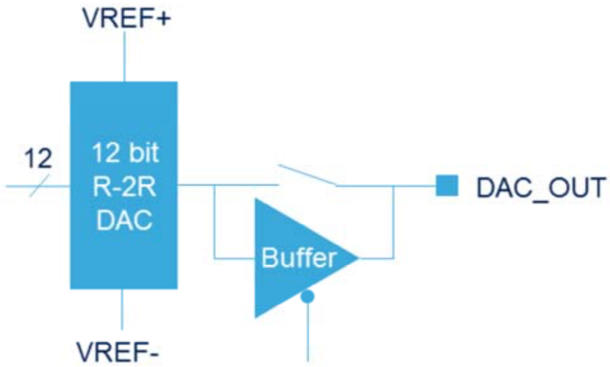


Here you can see the simplified block diagram of the digital-to-analog converter. The STM32F7 integrates 2 of them.

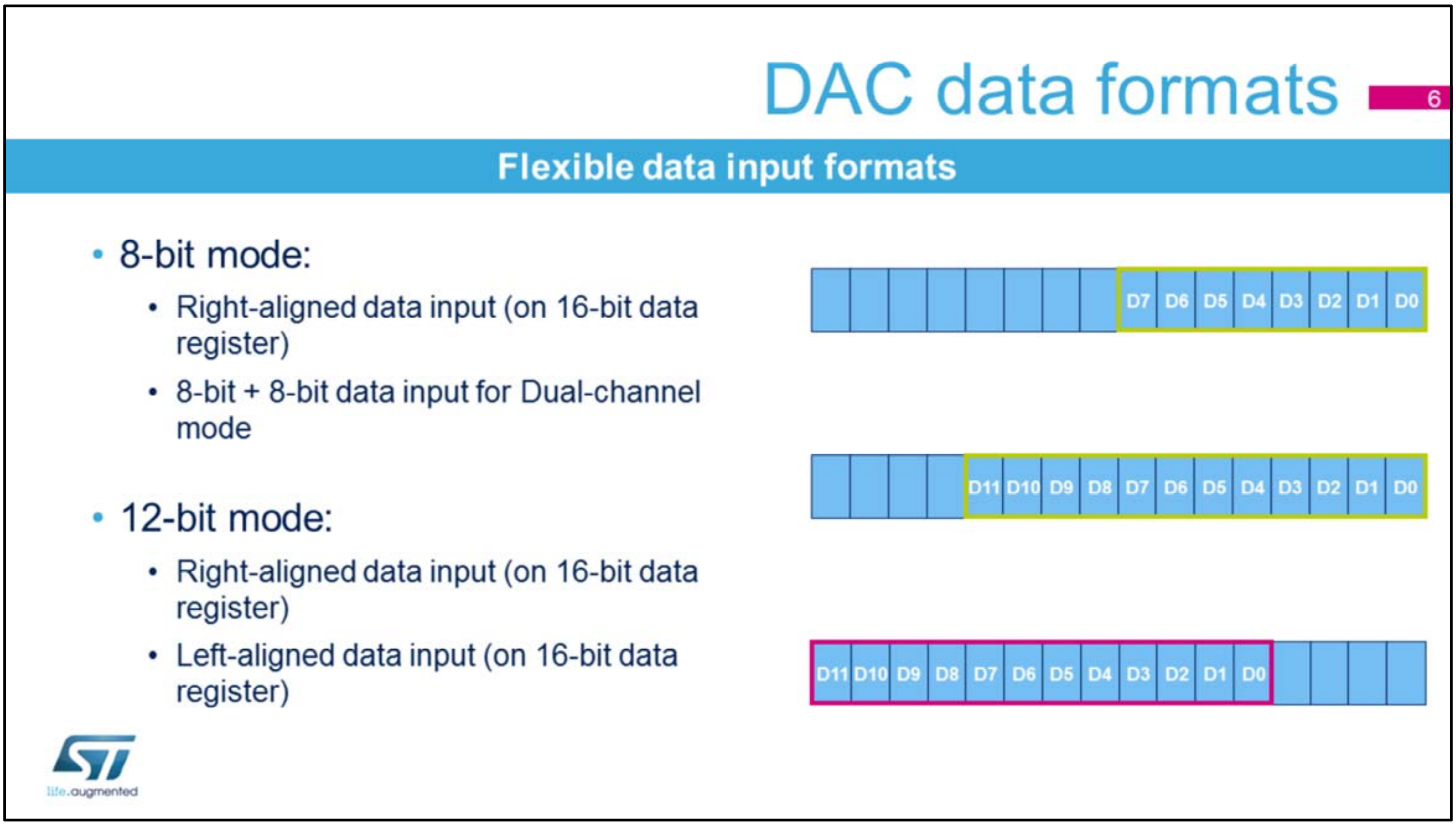
DAC with output buffer

Easy to interface with different configurations

- Output
  - Low impedance output using buffered mode
  - Raw output from the R-2R type resistor ladder DAC
    - Output impedance is <15 kΩ



The DAC output can be buffered for low impedance loads. When unbuffered, the output is directly connected to the R-2R resistor ladder network type of DAC.



The DAC can support different input formats. In 8-bit mode, it’s a right-aligned 8-bit data format. In Dual channel mode , it’s an 8-bit plus 8-bit data format, in order to provide input data for two DAC simultaneously. In 12-bit mode, either a right- or left-aligned mode can be used for input data.

DAC conversion triggers

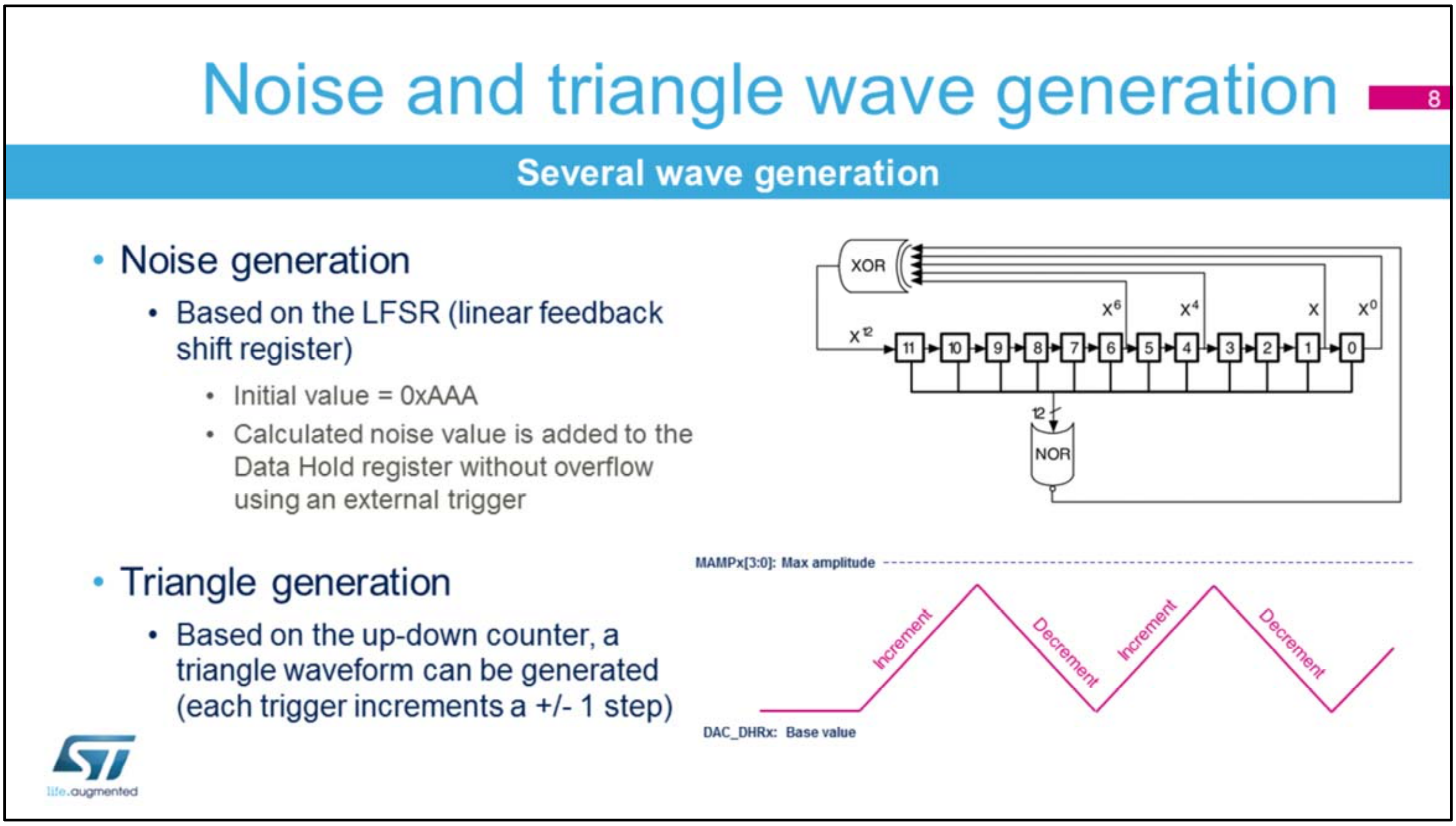
7

Several triggers for starting the DAC

- Conversions can be started
- Automatically by writing to the Data Hold register
- By a triggered conversion:
  - 6 different timer outputs
  - External I/O trigger
  - Setting the software trigger bit

life.augmented

DAC output conversion is started by writing to the Data Hold register using software. 6 different timer outputs, an external I/O or software can trigger a DAC conversion.

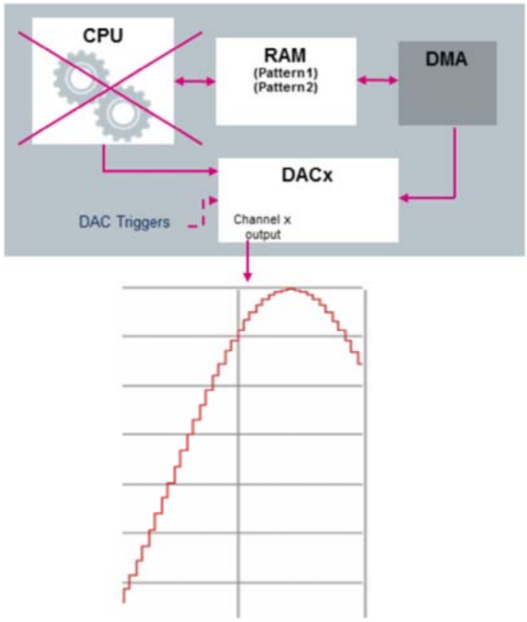


The DAC digital interface integrates two special signal generators. The Linear Feedback Shift register can create the noise signal for the DAC input. Each trigger updates the DAC output data by an LFSR block.
The up-down counter with a programmable count value can create triangle wave data which can update the DAC output data. The data can also be updated by a trigger signal.

DAC with DMA

Offloads the CPU

- The DAC DMA request is generated when an external trigger occurs:
  - The Data Hold register value is then transferred to the Data Output register.
  - DMA underrun with interrupt capability
  - Can generate a stable sampling time based output (timer controlled)



life.augmented

The DAC can also create DMA requests from the trigger signal. Once a trigger is detected, the Data Hold register value is then transferred to the Data Output register. Then the DMA request is generated to obtain the new data for the Data Hold register. As the update of the Output Data register is initiated directly by the trigger signal, the DAC output signal will not have jitter, so that it can create a stable sampling time signal output, making it easy to filter out the sampling frequency.

Interrupts and DMA

Interrupt event	Description
DMA underrun	When a DMA request is not processed by the next external trigger

DMA event	Description
DMA request	External trigger when the DMAENx bits are set

The DAC can generate a DMA underrun interrupt. To transfer data from memory, a DMA request can be generated.

Low-power modes

Mode	Description
Run	Active.
Sleep	Active.
Stop	Active.
Standby	Powered-down. The peripheral must be reinitialized after exiting Standby mode.

The digital-to-analog converter is active in the following power modes: Run, Sleep and Stop.
In Standby modes, the DAC is powered-down and it must be reinitialized afterwards.

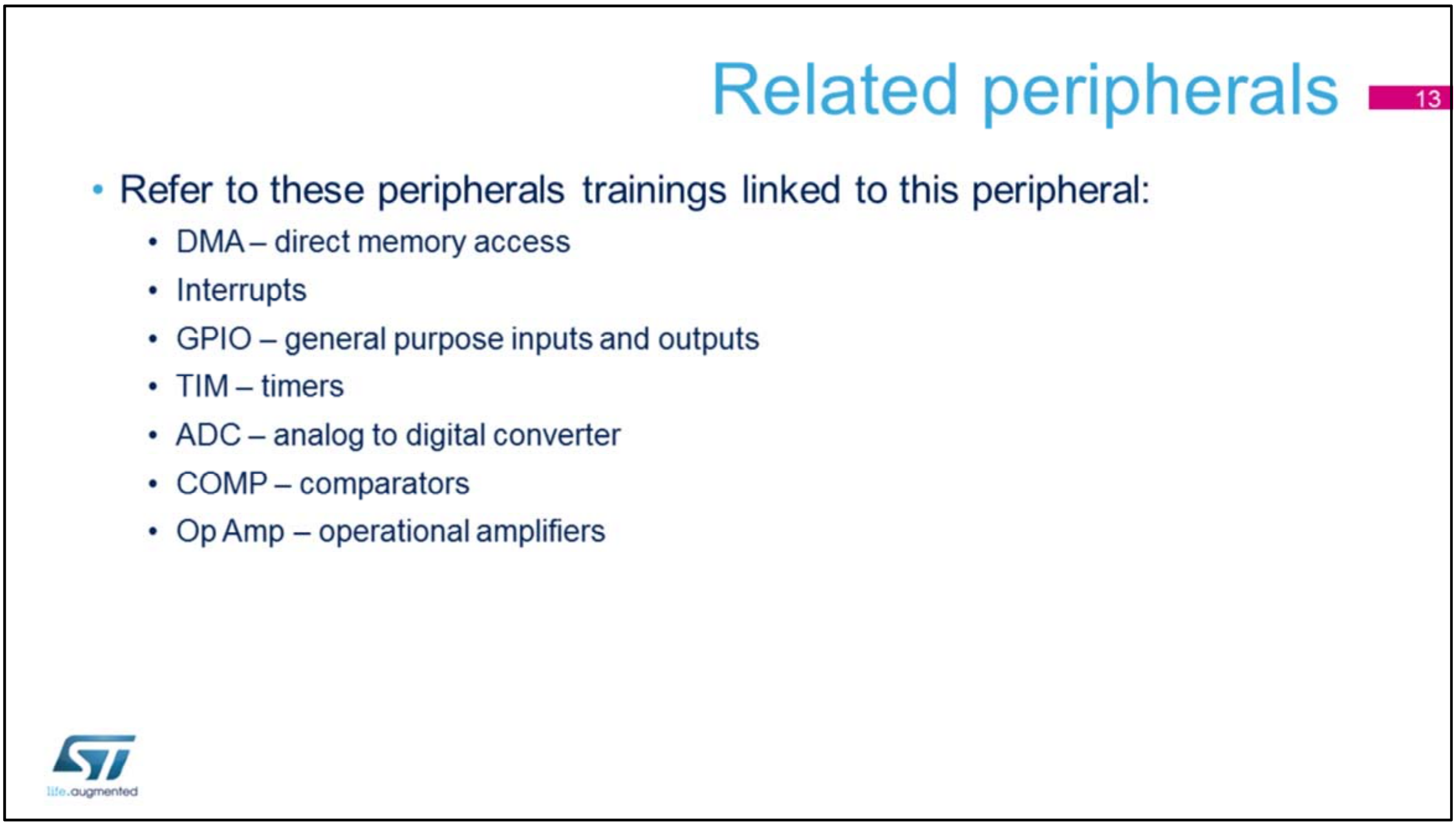
Performance

12

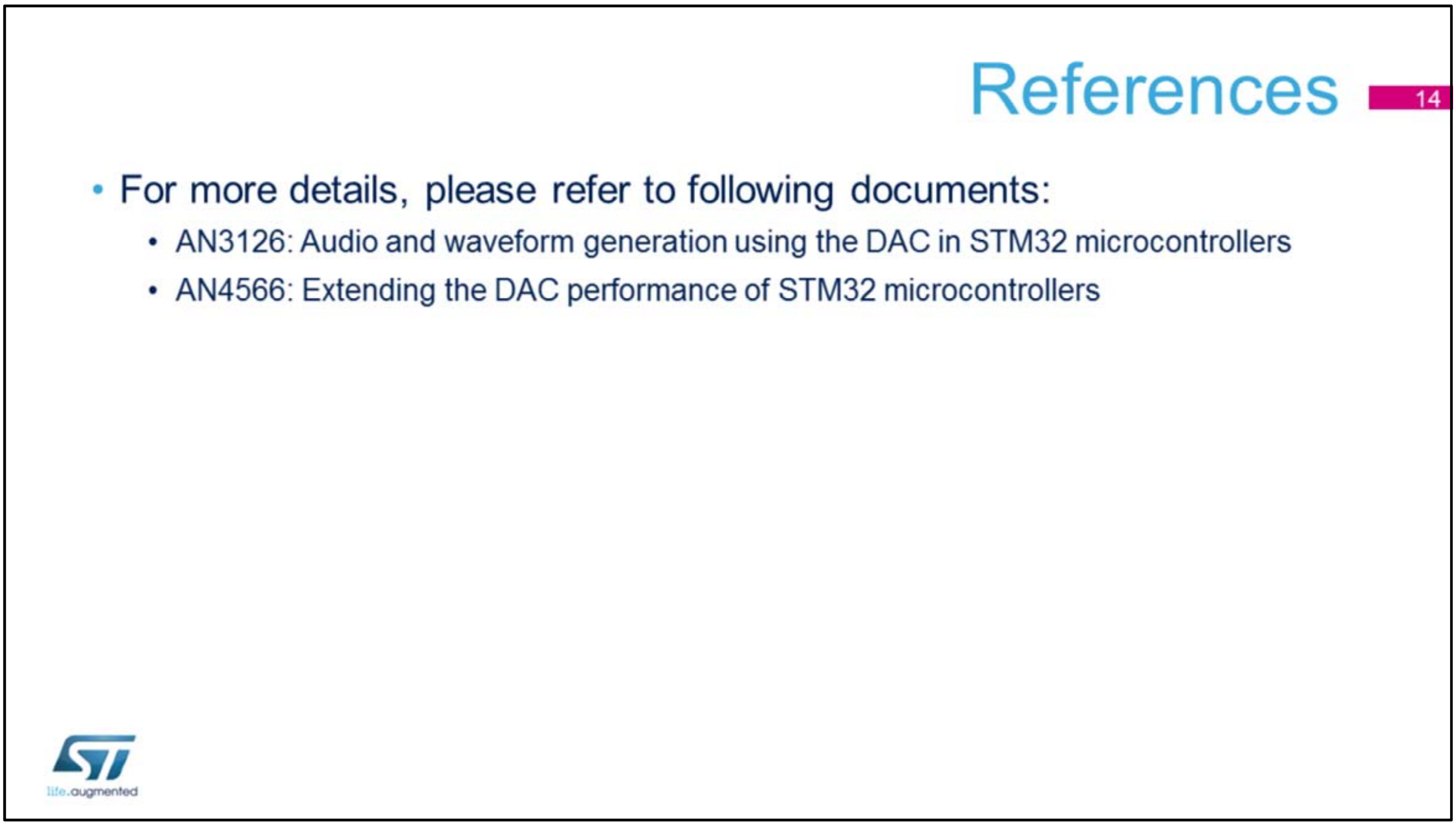
	Condition	Value (typical)	Unit
VDDA		1.8 ~ 3.6	V
Monotonicity		10	bits
DNL		+/- 2	LSB
INL		+/- 4	LSB
Consumption	Buffer on Buffer off	450 170	µA µA
Settling time	+/-4 LSB (Buffer on) R = 5 kohm, C = 50 pF	3	µs
Sampling rate		1.0	Msample/s

life.augmented

The following table shows some performance parameters for the digital-to-analog converter. The DAC can work between 1.8 and 3.6 volts. 10-bit monotonicity is guaranteed. Power consumption is 450 µA when the buffer is enabled and 170 µA when the buffer is disabled. The DAC buffered output has a settling time of 3 µsec with 5 kohms and 50 pF load. The DAC can handle a sampling rate of 1 mega sample per second; when using external components, it can support up to 10 mega samples per second. This is described in detail in application note AN4566.



This is a list of peripherals related to the DAC. Please refer to these peripheral trainings for more information if needed.



Application notes dedicated to DAC topics are also available.