
Hello, and welcome to this presentation of the SPDIF-RX block.
SPDIF stands for Sony/Philips Digital InterFace.

## Overview

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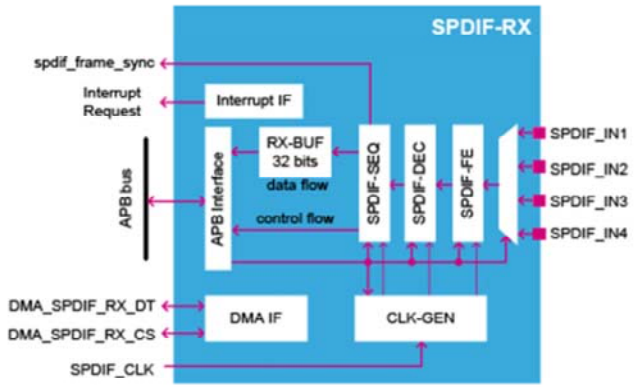
- The SPDIF-RX interface (Sony/Philips Digital InterFace) is able to receive an SPDIF flow compliant with standards IEC 60958 and IEC61937.




### Application benefits

- Data stream separated from control stream
- Interrupt and DMA services

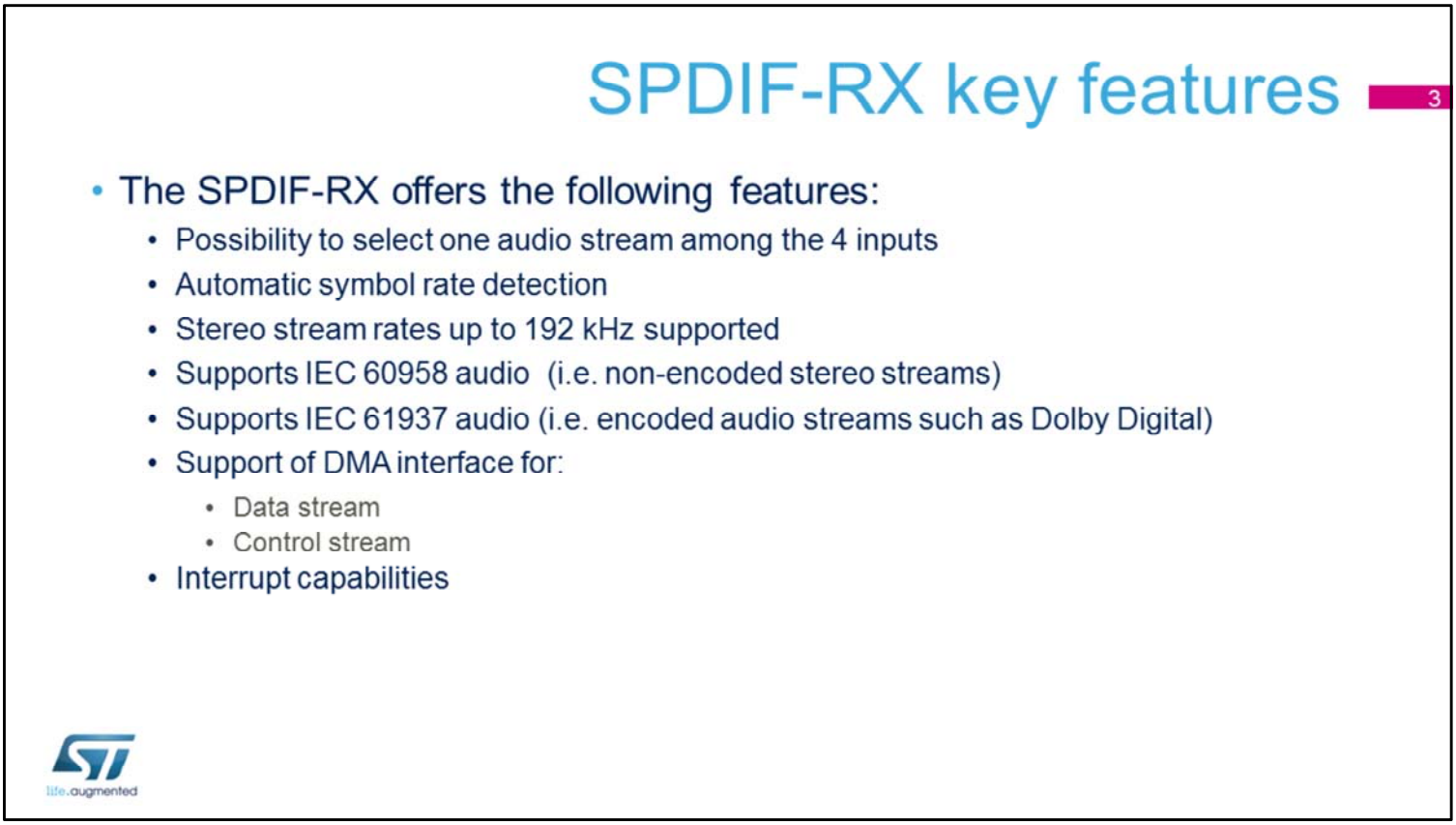
The SPDIF-RX block is able to receive digital audio streams compliant with the IEC-60958 and IEC-61937 standards.

The SPDIF-RX embeds an Advanced Peripheral Bus (or “A” “P” “B”) interface, allowing the control of the block and the reception of audio and control flows.
The SPDIF-RX also provides status registers so the application can check the quality of the reception.

The SPDIF-RX needs two peripheral clocks:
- An APB clock for the register interface accesses.
- A kernel clock named SPDIF_CLK used for the re-sampling and processing of the incoming stream.

The receiver part is mainly composed of:
- the SPDIF-FE which performs the sampling, the

filtering and the edge detection of the incoming stream
- the SPDIF_DEC which decodes the received symbols
- the SPDIF_SEQ which checks the frame format integrity, and separates the payload from the control /user information.




The SPDIF-RX provides the following features:

- Possibility to select one audio stream among the 4 inputs. Note that only one stream can be decoded at a single time.
- Automatic symbol rate detection. If the SPDIF_CLK frequency is high enough, the SPDIF-RX will be able to decode the incoming stream, and provide to the application information about its estimated sampling rate. Stereo stream rates up to 192 kHz are supported.
- The SPDIF-RX decodes audio frames compliant with IEC-60958. This specification describes non-encoded stereo streams. The SPDIF-RX also supports encoded audio streams such as Dolby Digital as described in IEC-61937.
- In addition, the SPDIF-RX provides two DMA channels: one dedicated to the audio samples data

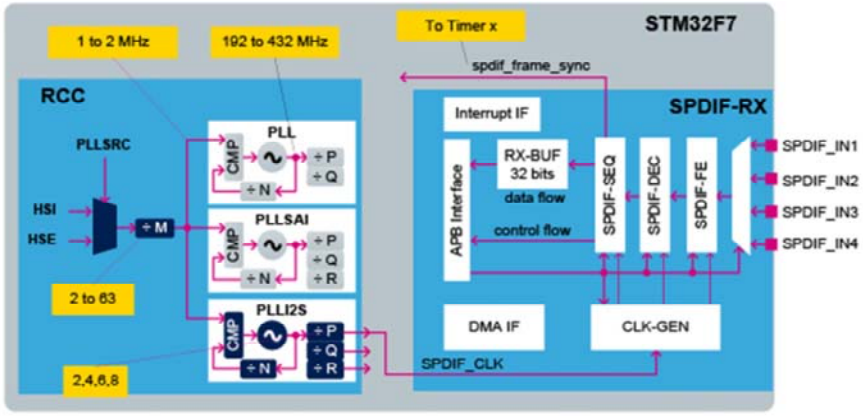
(encoded or not), and one dedicated to the control, status and user information.

- Interrupt capabilities are also available for various signaling.

# SPDIF-RX in the circuit



- The P output of the PLLI2S provides a kernel clock to the SPDIF-RX.
- The SPDIF_CLK does not need to be a multiple of the audio frequency




The RCC (Reset and Clock Control) block of the STM32F7 provides both the APB clock and the SPDIF_CLK kernel clock to the SPDIF-RX.
The SPDIF_CLK is generated by the post-divider P of the PLLI2S, allowing the application to adjust the SPDIF_CLK frequency.

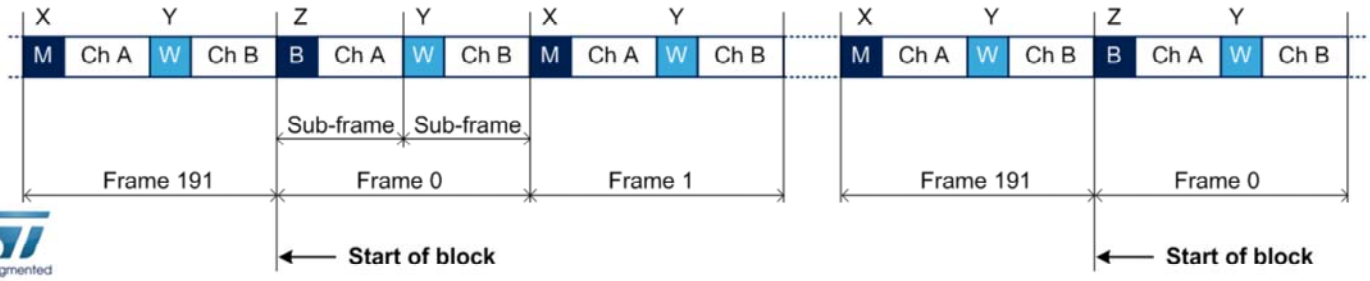
The signal spdif_frame_sync provided by the SPDIF-RX is connected to a timer, the application can use it to perform a clock drift estimation in between the two audio streams.

Refer to the training slides of the RCC for more details.

# SPDIF protocol overview (1/5)



- The block structure is used to organize the Channel Status (CS) and User (U) information.
  - Each block contains 192 frames
  - Each frame contains 2 sub-frames
  - A preamble allows the detection of the block and sub-frame boundaries
    - Preamble B detects the start of new block, and the start of a Channel A
    - Preamble M detects the start of a Channel A (when it is not a block boundary)
    - Preamble W detects the start of a Channel B




The next 5 slides give a short overview of the SPDIF standard.
They mainly describe the physical and logical structure of the digital audio stream.

In IEC60958, the digital audio stream is organized in block structure in order to decode the Channel Status (CS), and User (U) information .

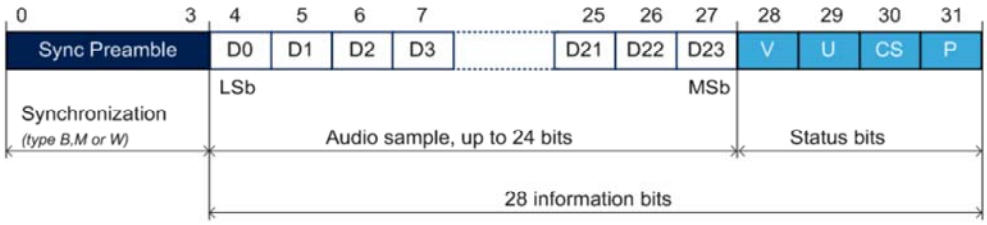
- Each block contains 192 frames
- Each frame contains 2 sub-frames

The SPDIF-RX is able to recognize the start of block, the preambles and the frame boundaries.

# SPDIF protocol overview (2/5)



- Sub-frame format
  - The preamble
  - Up to 24 bits of data
  - 4 Status bits
    - V is the validity bit, it means that the current sample can be directly converted into an analog signal.
    - P is the parity bit of the received sub-frame, it is used to check the received sub-frame
    - U is the User data channel, each message is composed of 192 bits
    - CS is the Channel Status, each message is composed of 192 bits (i.e. sampling rate, sample length….)



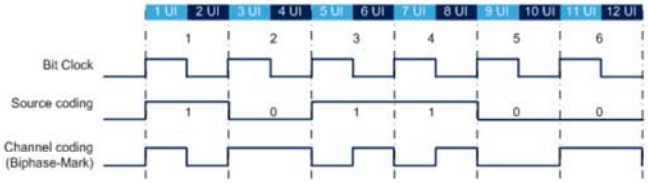

An SPDIF frame contains 2 sub-frames. Each sub-frame contains 32 bits, divided into 3 fields:

- A synchronization preamble allowing the detection of the block and sub-frame boundaries
- A payload of 24 bits
- Status bits: V, U, CS and P

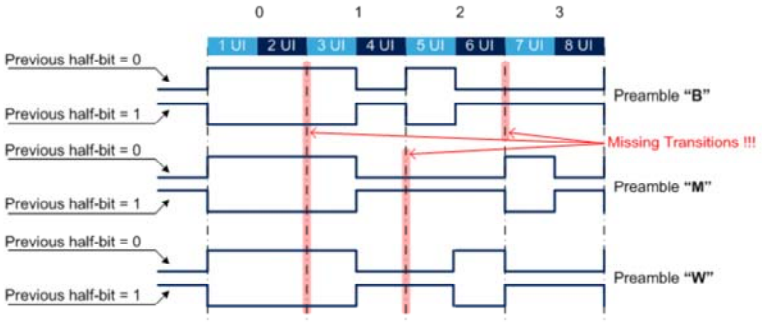
# SPDIF protocol (3/5)



- Biphase-mark data encoding:




- Preambles:
  - The preambles 'violate' the biphase-mark code rules

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The digital audio data are coded using biphase-mark encoding as shown in the upper figure.
Note that with biphase-mark encoding, there is a transition at the boundary of each bit.

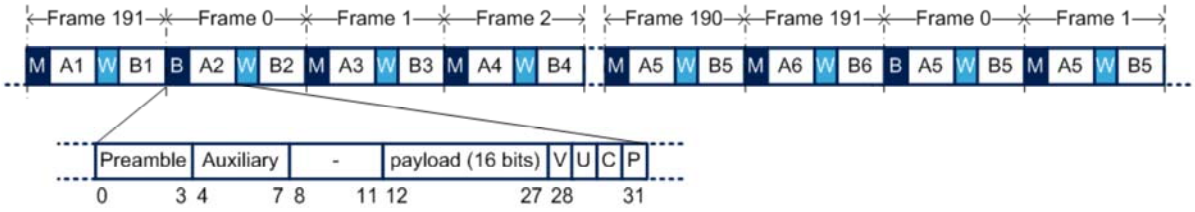
The preamble length is 4 bits, and some transitions on the preamble do not respect biphase-mark encoding. This will be used by the SPDIF receivers to easily detect the block and sub-frame boundaries.

UI means Unit Interval, it represents the shortest nominal time interval in the coding scheme.

# SPDIF protocol overview (4/5)



- The IEC 61937 standard allows the transfer of non-linear encoded PCM audio streams into sub-frames as described in IEC 60958.
  - The encoded audio streams are transported over this interface as a sequence of data-bursts.
  - Each data-burst consists of a 64-bit burst-preamble, followed by the burst-payload.
  - The data-bursts are transported by blocks of 16 bits, placed at position [12-27] of each IEC 60958 sub-frame.




Bits 4 to 27 of each sub-frame can also be used to transfer encoded audio signals.
This is described in specification IEC61937.

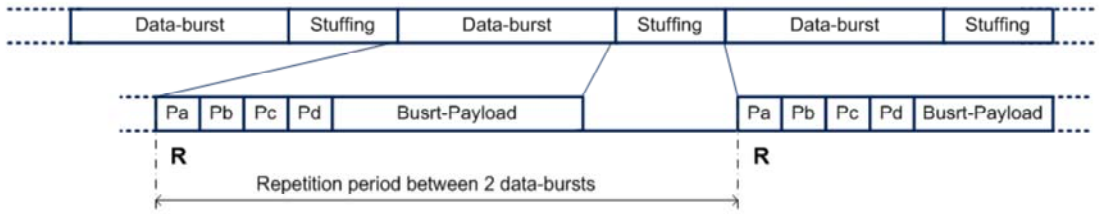
The encoded data packet uses bits 12 to 27 of each sub-frame.
The 64-bit burst-preamble is a specific pattern also located on bits 12 to 27 of 4 consecutive sub-frames.
It is used to detect the start of a data-burst.

Note that the burst-preamble (64 bits) shall not be confused with the sub-frame preamble (4-bits) used to detect the sub-frame and block boundaries.

# SPDIF protocol overview (5/5)



- The burst-preamble:
  - The Pa, Pb preamble are the synchronization patterns (Pa = 0xF872, Pb = 0x4E1F)
  - The Pc, Pd preamble contain information on data packet and payload size
- The burst-payload contains the encoded data (Dolby Digital, DTS…).
- Stuffing:
  - Between two repetition periods, the payloads of un-used sub-frames are forced to zeroes. These sub-frames are called “stuffing”.




The first 32 bits of the burst-preamble are a fixed pattern: Pa and Pb.
The last 32 bits of the burst-preamble contain information on data packet and payload size.

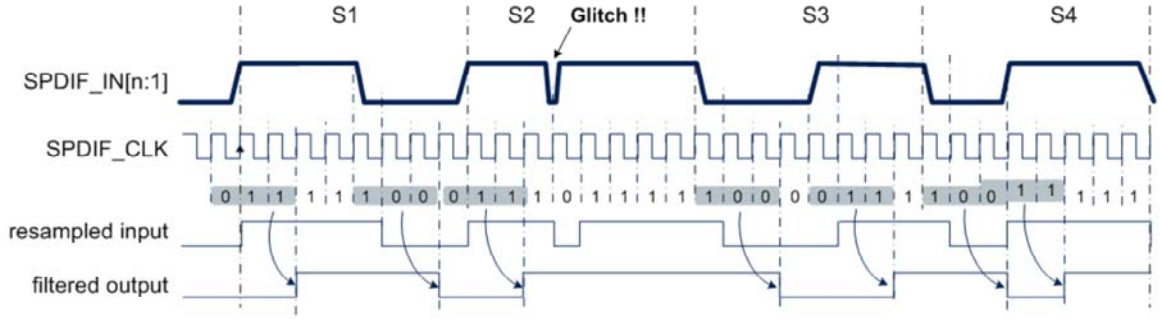
Stuffing is used to adjust the repetition rate of the data-bursts.

# SPDIF-RX noise filtering



- **Reduces sensitivity to input signal noise!**

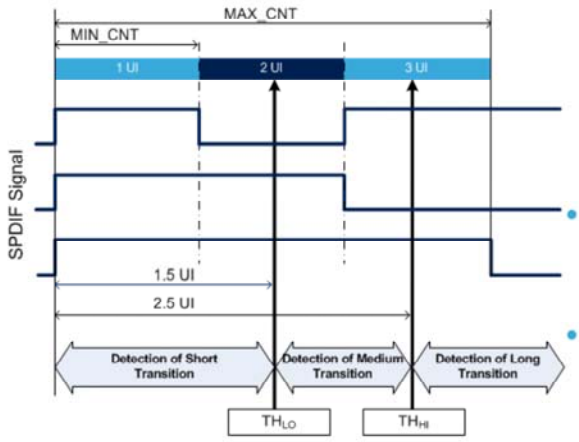
- The SPDIF-RX provides a filtering of the incoming stream, working as follow:
  - A rising edge is detected when a 0-1-1 sequence is sampled.
  - A falling edge is detected when a 1-0-0 sequence is sampled.
  - After a rising edge, a falling edge sequence is expected.
  - After a falling edge, a rising edge sequence is expected.




The SPDIF-RX is able to suppress glitches, increasing reception reliability.

# SPDIF-RX synchronization (1/3)






- The receiver must be able to estimate the time interval between two transitions and defines if it is:
  - A part of a '1' symbol
  - A '0' symbol
  - A long pulse (preamble)
- The receiver estimates two thresholds: THLO and THHI in order to distinguish the transition type.
- If the time interval between two transition is:
  - Lower than THLO → Short transition detected
  - Higher than THHI → Long transition detected
  - Between THLO and THHI → Medium transition detected

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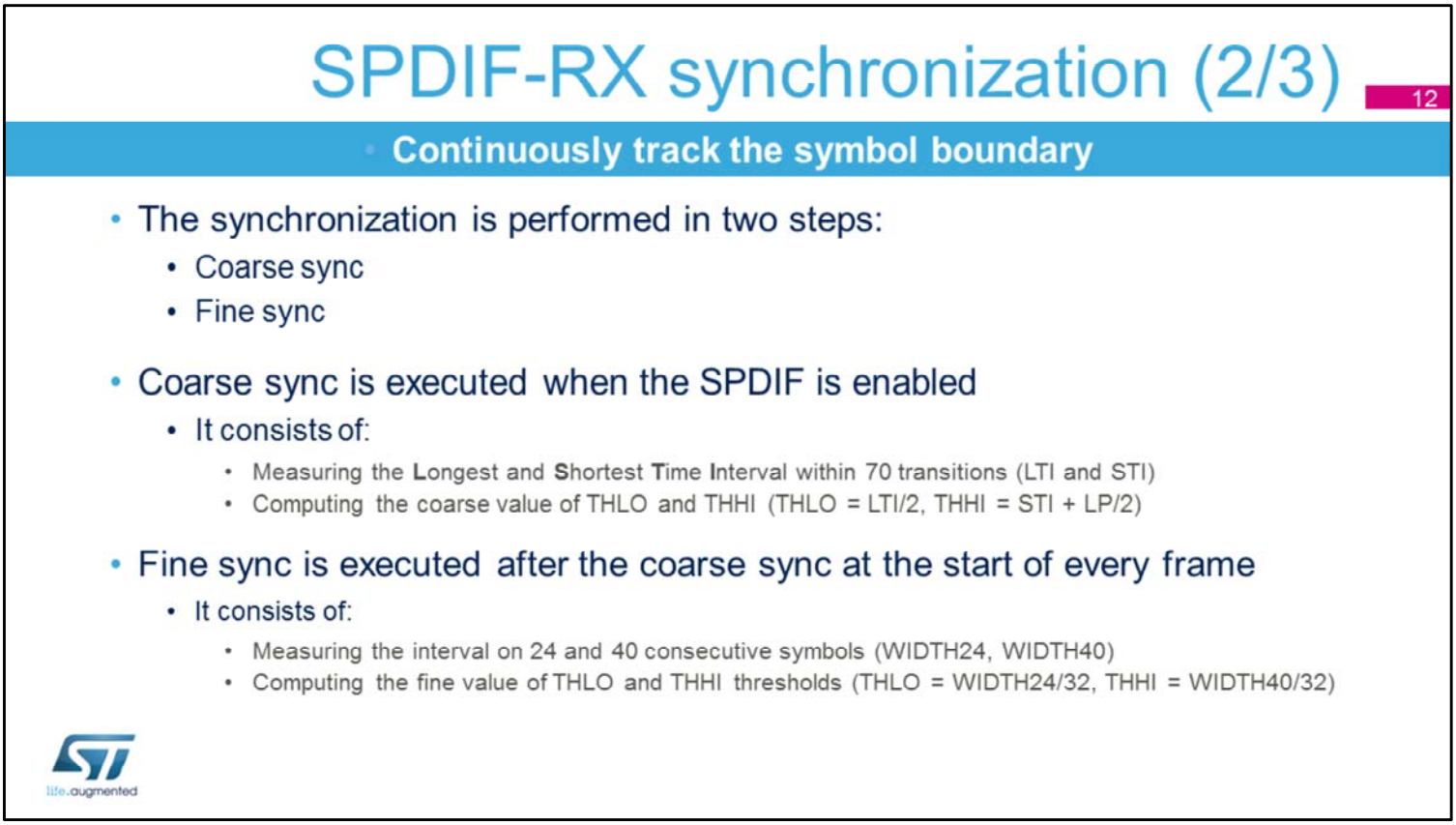
In order to decode the incoming stream, the SPDIF-RX estimates the duration of one UI and defines two thresholds:

- The low threshold: THLO fixed to 1.5 UI
- The high threshold: THHI fixed to 2.5 UI

When both thresholds have been computed, the SPDIF-RX compares the time interval between consecutive transitions of the incoming stream to those thresholds.
If the time interval is lower than THLO , a short transition is detected. Note that two consecutive short transitions correspond to the symbol '1', but can be also a part of the preamble pattern.
If the time interval is between THLO and THHI, a medium transition is detected. Note that a medium transition correspond to the symbol '0', but can be also a part of the preamble pattern.
If the time interval is higher than THLO, a long transition is detected. Note that a long transition is always a part of the

preamble pattern.




In order to decode the incoming stream with good reliability, the estimation of the thresholds THLO and THHI must be accurate.

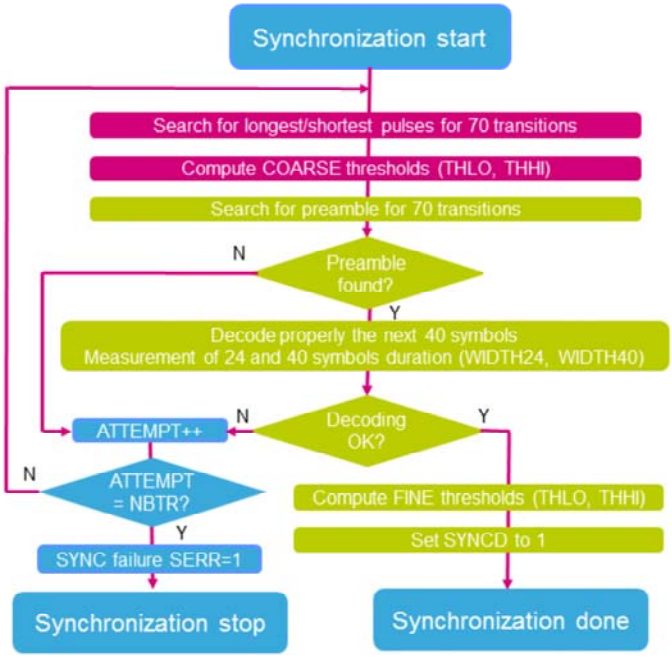
The THLO and THHI thresholds are estimated in 2 steps: The coarse synchronization measures consecutive time intervals within 70 transitions and then selects the longest and the shortest time intervals.
These two values are used to compute a first estimate of THLO and THHI thresholds.

Thanks to a coarse estimate of THLO and THHI thresholds, the SPDIF-RX is able to decode SPDIF frames and then further improve the estimation of THLO and THHI thresholds by measuring intervals over 24 and 40 consecutive symbols.

# SPDIF-RX synchronization (3/3)



- In noisy environments, the thresholds estimated by the coarse sync may be inaccurate.
  - Failures may appear until the fine sync is properly completed
- The user can choose the accepted amount of attempts (NBTR)




The figure shows the hardware process performed by the SPDIF_RX in order to estimate properly the THLO and THHI thresholds.

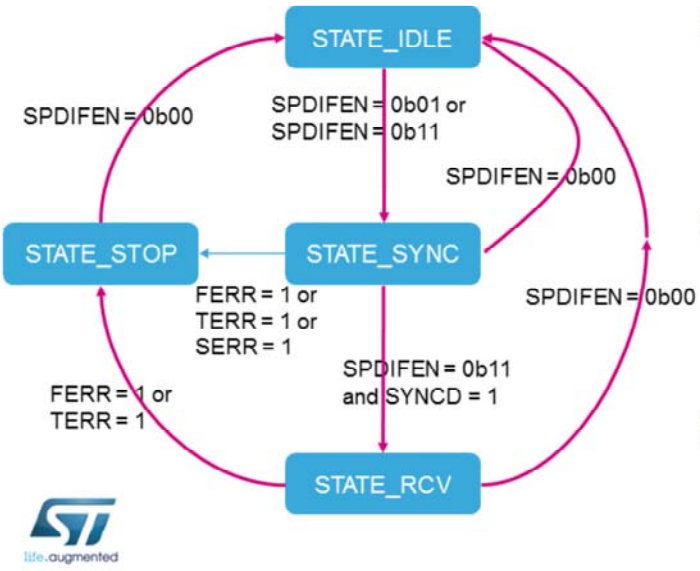
Note that the coarse synchronization may become inaccurate in a noisy environment and the fine synchronization may fail.
This can be considered as a normal situation, and the application can program an amount of retries (NBTR).

Note as well that the THLO and THHI thresholds are updated every frame.

# SPDIF-RX states



The SPDIF-RX can switch in between 4 states:




**STATE_IDLE**:

The SPDIF-RX is disabled

**STATE_SYNC**:

The SPDIF-RX is synchronized, thresholds are updated regularly.

The user and channel status can be read.

The audio samples are not provided to receive buffer.

**STATE_RCV**:

The SPDIF-RX is synchronized, thresholds are updated regularly.

The user and channel status can be read.

Data are provided to the receive buffer.

**STATE_STOP**:

Error(s) occurred.

The user, channel status and data reception is stopped.

The user must switch the peripheral to STATE_IDLE.

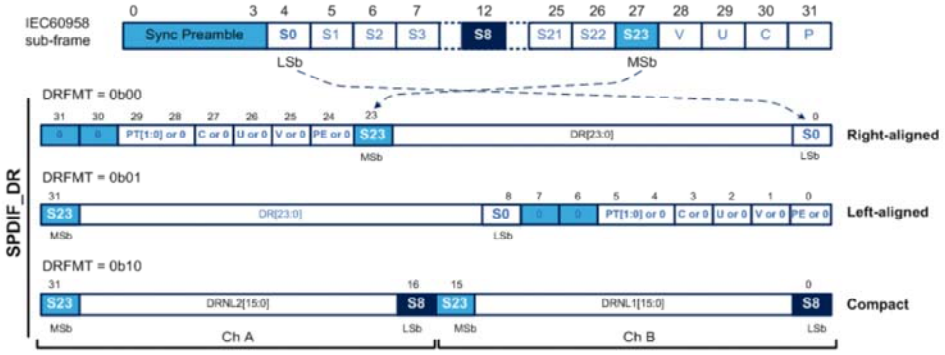
The figure shows the different states of the SPDIF-RX. The state of the SPDIF-RX can be changed by the application, via the field SPDIFEN or by the SPDIF-RX hardware mainly if errors are detected.

When an error is detected, the SPDIF-RX directly moves to STATE_STOP. It is up to the application to set the SPDIF-RX to STATE_IDLE and then set it again to STATE_SYNC or STATE_RCV.

# SPDIF-RX data flow



- The SPDIF-RX offers a 32-bit double buffer for data reception
- Possibility to read data via DMA or Interrupt
- Flexible data format: right-aligned, left-aligned, or compact format
  - The bits PTMSK, CUMSK, VMSK, and PMSK can be used to insert a preamble type, C & U bits, Validity bit and Parity error bit to each data sample.




The SPDIF-RX offers a 32-bit double buffer for data reception.

The application can read the received data using DMA or Interrupts.

Various data formats are available:

- right-aligned,
- left-aligned, or
- compact format

The compact format can be interesting when the SPDIF-RX is receiving encoded audio frame.

In addition, the SPDIF-RX can insert a preamble type, C & U bits, Validity bit and Parity error bit with each audio sample.

Using the mask bits, the user can select which information will be provided.

# SPDIF-RX control flow

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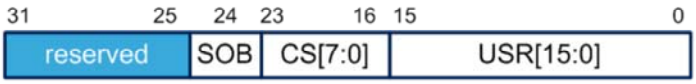
- The SPDIF-RX offers a 32-bit buffer for CS and U channel reception
  - The user can choose to read CS from Channel A or Channel B (exclusive).
  - Possibility to read CS and U via DMA or Interrupt.
  - The acquisition of CS and U bits is triggered at the start of a new block, once the fine synC is completed.
  - Every time 8 frames, the collected CS and U bits are copied into the SPDIF_CSR register.
  - The SOB bit indicates if the CS and U bits correspond to the first 8 frames of a block.

**SPDIF_CSR format**




CS0 is the oldest value
USR0 is the oldest value from the channel A
USR1 is the oldest value from the channel B

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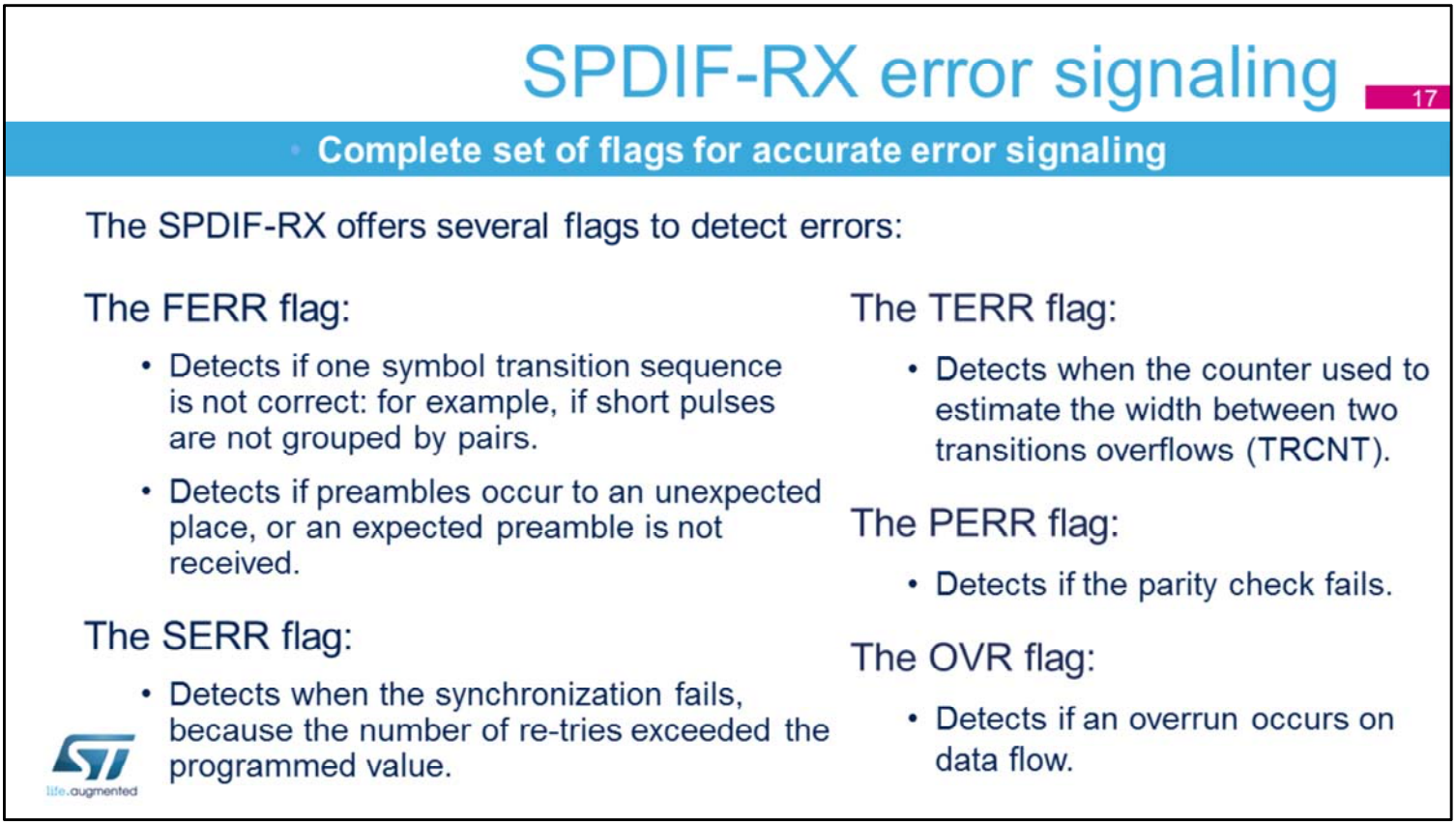
The SPDIF-RX offers a 32-bit buffer for the reception of the CS and U channels.

The application can read the received control information in the SPDIF_CSR register, using DMA or Interrupts.

The SPDIF_CSR register contains:
- 8 bits of CS coming from the selected channel (could be channel A or B)
- 16 bits of U (the U bit of channel A and U bits from channel B).
- 1 bit indicating if a start of block has been detected.




A complete error signaling is provided to the application in order to define the root cause of any failures.

The FERR flag detects errors linked to the frame structure.

The SERR flag detects synchronization failures.

The TERR flag detects when the counter used to estimate the width between two transitions overflows. This generally means that no signal is detected on the selected SPDIF input.

The PERR flag detects if the parity check fails.

The OVR flag detects if an overrun occurs on the data flow.

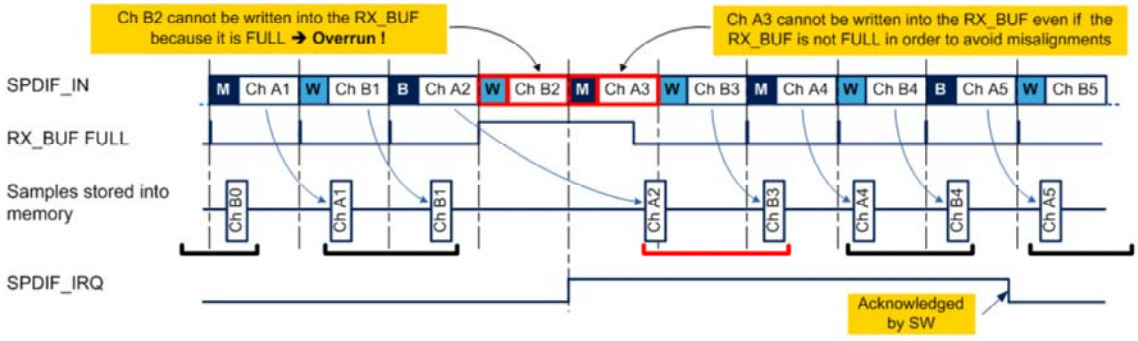
# SPDIF-RX overrun handling



**• SPDIF-RX recovers from overrun without misalignments**

The SPDIF-RX can recover from an overrun situation without misalignment.

- The RXSTEO bit is used to indicate how the SPDIF reacts to an overrun situation:
  - If RXSTEO = 0, the SPDIF-RX minimizes the amount of data lost. To be used for PCM MONO mode, or reception of encoded audio signals
  - If RXSTEO = 1, the SPDIF-RX avoids the misalignment of stereo samples. Must be used for PCM STEREO streams (see figure below)

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The RXSTEO bit indicates how the SPDIF reacts to an overrun situation:

- If RXSTEO = 0, the SPDIF-RX can minimize the amount of data lost. To be used for PCM MONO mode, or the reception of encoded audio signals.
- If RXSTEO = 1, the SPDIF-RX can avoid the misalignment of stereo samples. Must be used for PCM STEREO streams.

# SPDIF-RX interrupts



- The SPDIF-RX offers a single interrupt line, handling the following events:

| Interrupt Event | Description | How to clear interrupt |
|---|---|---|
| **RXNE** | Reception Buffer Not Empty for data flow | Read SPDIF_DR |
| **CSRNE** | Reception Buffer Not Empty for control flow | Read SPDIF_CSR |
| **PERR** | Data corruption detection | Set PERRCF to 1 |
| **FSERR** | Frame structure and synchronization error (Includes SERR, TERR and FERR) | Set SPDIFEN to 0 |
| **OVR** | Overflow detection | Set OVRCF to 1 |
| **SDB** | Start of new block detection | Set SBDCF to 1 |
| **SYNCD** | Synchronization done | Set SYNCDCF to 1 |

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The SPDIF-RX offer a single interrupt line shared by several events:

- Error events
- Data and Control flow reception events
- Synchronization ready event
- Block detection event

# SPDIF-RX clocking



- The SPDIF_CLK is used to sample the incoming S/PDIF stream
- The SPDIF_CLK frequency must be at least 11 times higher than the symbol rate of the incoming audio stream
- The symbol rate is 64 times higher than the audio sampling rate (IEC 60958).

| Sample Rate (Symbol rate) | Minimum SPDIF_CLK Frequency |
|---|---|
| 48 kHz (3.072 MHz) | 33.8 MHz |
| 96 kHz (6.144 MHz) | 67.6 MHz |
| 192 kHz (12.288 MHz) | 135.2 MHz |

The higher the SPDIF_CLK frequency is, the more reliable the reception will be.

In order to have a reliable decoding of the SPDIF stream, the SPDIF_CLK frequency must be at least 11 times higher than the symbol rate.
The table gives the minimum requested frequency for the SPDIF_CLK clock according the sample rate of the SPDIF stream.

# SPDIF-RX misc functions



- The SPDIF-RX provides a means to estimate the symbol rate:
  - The WIDTH5 field provides the duration of 5 symbols counted with SPDIF_CLK clock.
  - Example: If $f_{SPDIF\_CLK}$ = 84 MHz, and WIDTH5 = 144d, then the audio sampling rate coarse estimate (fs) is:

    $fs = 5 \times f_{SPDIF\_CLK} / (WIDTH5 \times 64) \sim 45.6$ kHz

    the closer audio standard frequency is 44.1 kHz, so the received stream is probably 44.1 kHz.
- It is possible to check the estimated THLO and THHI values via the SPDIF_DIR register.
- The SPDIF-RX provides the spdif_frame_sync signal to be connected to a timer in order to estimate the clock drift.

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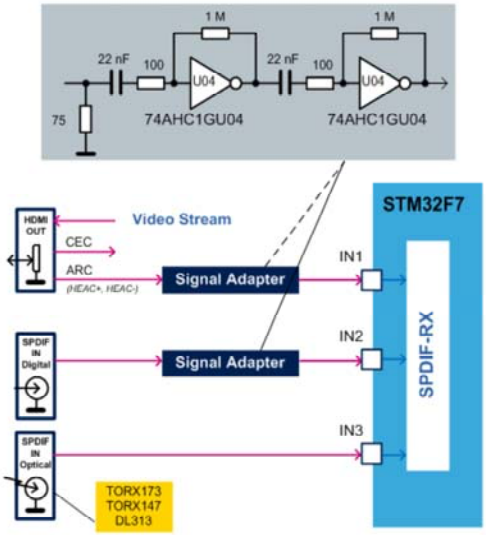
The SPDIF-RX provides information allowing the application to estimate the sampling rate of the decoded stream without having to decode the CS channel.
The accuracy of the sampling rate estimation is partly limited by the frequency of the SPDIF_CLK.

The application can also check the estimated THLO and THHI thresholds for debugging purposes.

The SPDIF-RX also provides a signal named spdif_frame_sync which can be connected to a timer in order to estimate the clock drift.
This feature can be useful if the circuit receives audio samples via SPDIF-RX, performs audio processing and provides audio samples to an external audio device.
In this case a sample rate converter may be needed to perform the rate adaptation, which may require the clock drift estimation.

# SPDIF-RX misc functions






- The SPDIF-RX can receive signals coming from:
  - An SPDIF digital input
  - An SPDIF optical input
  - Audio Return Channel from an HDMI connector
- A simple signal adapter may be needed in order to amplify the signal received from the SPDIF interface 200 millivolts peak-to-peak (200 mVpp).

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The SPDIF-RX can receive signals coming from:

- An SPDIF input
- An SPDIF optical input
- Audio Return Channel from an HDMI connector

A signal adapter may be needed in order to amplify the signal received from the SPDIF interface (200 mVpp) .

Using 1 or 2 unbuffered inverters can be sufficient in most cases.

Note that for SPDIF decoding, the signal polarity can be inverted without affecting the decoding; only the transitions are used by the receiver.

# Low-power modes



| Mode | Description |
|---|---|
| **Run** | Active. |
| **Sleep** | Active. Peripheral interrupts cause the device to exit Sleep mode. |
| **Stop** | Frozen. Peripheral registers content is kept. |
| **Standby** | Powered-down. The peripheral must be reinitialized after exiting Standby mode. |

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Here is an overview of the status of the SPDIF-RX in each of the low-power modes.
SPDIF-RX operations are not possible when the device is in Stop and Standby modes.

# Related peripherals



- Refer to these trainings related to this peripheral for more information:
  - Reset and clock control (RCC)
  - Direct memory access controller (DMA)

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This is a list of peripherals related to the SPDIF-RX. Please refer to Reset and Clock Control and Direct Memory Access Controller trainings for more details on possible configuration.