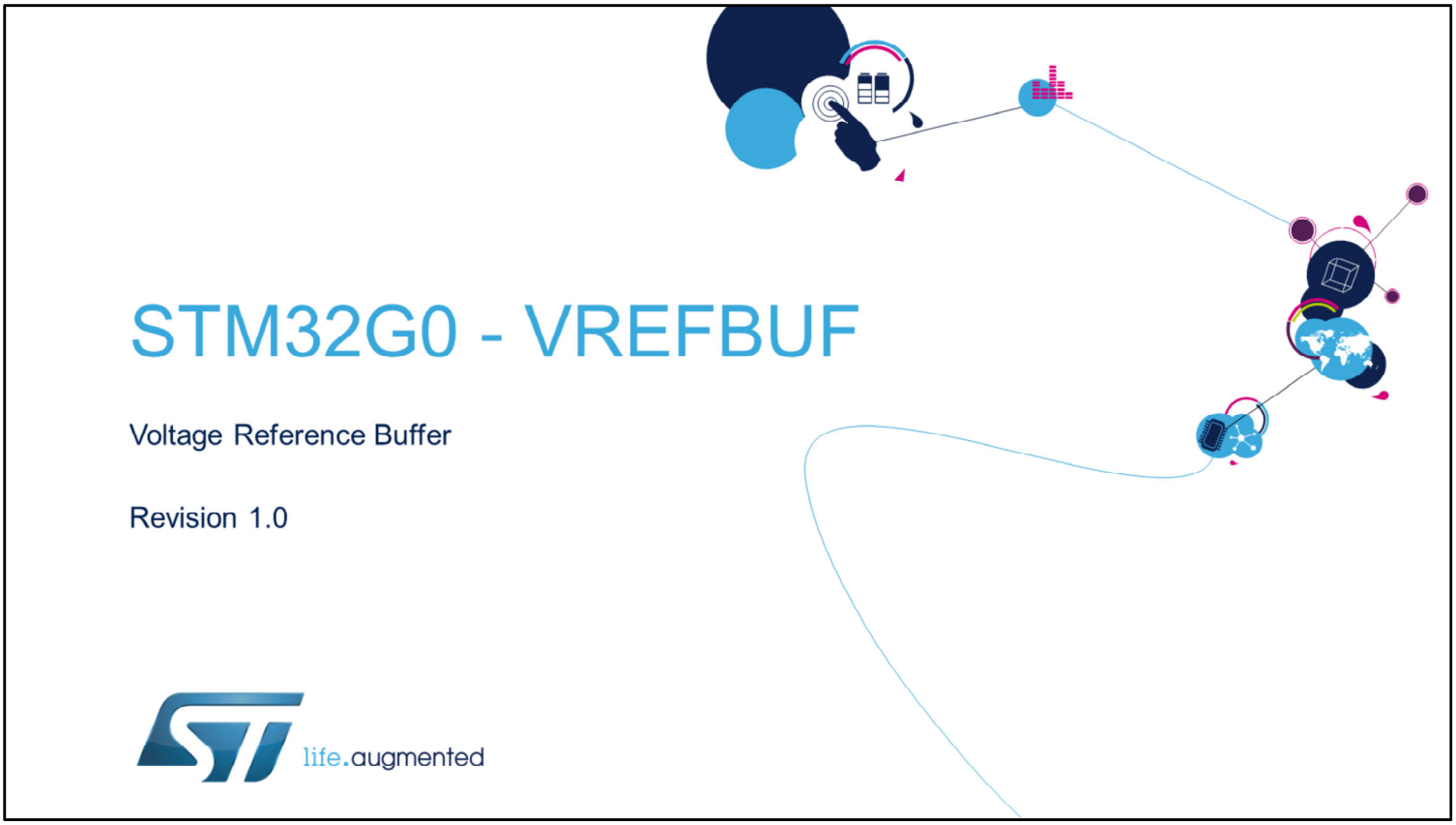
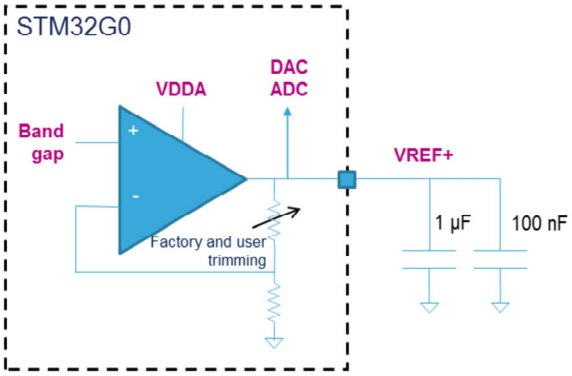


Hello, and welcome to this presentation of the STM32G0 Voltage Reference buffer. It covers the main features of this block, which creates an on-chip reference voltage.

Overview



- Provides an analog reference voltage
  - 2.5 / 2.048 V reference voltage for ADC/DAC
  - Can provide reference voltage and support external loads up to 4 mA with low quiescent current.

Application benefits

- Not necessary to have external reference voltage IC.
- On-chip VREF generator provides VDDA-independent reference voltage.

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The VREF buffer embedded in STM32G0 microcontrollers provides a stable voltage based on an internal bandgap reference for use by both the analog-to-digital and digital-to-analog converters. Its output voltage is programmable to 2.5 or 2.048 V. This output voltage can also support external loads up to 4 mA. External bulk and bypass capacitors are required when the internal VREF buffer is used.

Applications can benefit from this on-chip voltage reference as it eliminates the need for an expensive, external standalone reference voltage IC. For space-constrained systems, it is common to use the analog supply as the reference voltage. By using this VREF buffer instead, it can create a stable voltage even if the analog supply is changing, for example when the VDDA supply comes from a battery output.

Features (1/2)

- Supports 2 voltages controlled with **VRS** bit in VREF_CSR register:
  - VREFBUF_OUT1 ~= **2 .048 V**. This requires VDDA ≥ 2.4V
  - VREFBUF_OUT1 ~= **2 .5 V**. This requires VDDA ≥ 2.8V
- Internal reference output on VREF+ pin
  - Current load up to 4 mA (consumption < 50 µA)
- Requires external capacitance on VREF+ pin
- Not available on all packages (VREF+ double-bonded with VDDA)
- Factory and user calibrated

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Two reference voltage values can be chosen. The 2.5V value requires a VDDA ≥ 2.8 V.
The VREF+ pin can deliver 4 mA (maximum). In this case, the VREFBUF consumption from VDDA is 50 µA. The voltage is held with the external capacitor.
When the VREF+ pin is double-bonded with the VDDA pin in a package, the voltage reference buffer is not available and must be kept disabled (refer to datasheet for the full pinout description for each package).

Features (2/2)

- Configuration with ENVR and HIZ bits in the VREF_CSR

ENVR	HIZ	Configuration
0	0	VREF buffer OFF VREF+ pin pulled-down to VSSA
0	**1**	**External voltage reference mode (default):** • **VREF buffer OFF** • **VREF+ pin floating**
1	0	Internal voltage reference mode: • VREF buffer ON • VREF+ pin connected to the VREF buffer output
1	1	Hold mode: • VREF buffer ON • VREF+ pin floating. The voltage is held with an external capacitor

- VRR bit is set when the output reaches the defined value

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The internal voltage reference can be configured in four different modes depending on ENVR and HIZ bits configuration.
After enabling the VREFBUF buffer by setting ENVR bit and clearing HIZ bit in the VREFBUF_CSR register, the user must wait until the VRR bit is set, meaning that the voltage reference output has reached its expected value.

Low-power modes

Mode	Description
Run	Active.
Sleep	Active
Low-power run	Active.
Low-power sleep	Active.
Stop 0/Stop 1	Active.
Standby	Powered-down. The peripheral must be reinitialized after exiting Standby mode.

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The VREF Buffer is active in the following power modes: Run, Sleep, Low-power run, Low-power sleep, Stop 0 and Stop 1 modes.
In Standby and Shutdown modes, the VREF buffer is powered-down and it must be reinitialized after waking up from these modes.

Performance

Symbol	Condition	Typical	Unit
V_{DDA}	V_{REF} = 2.048	2.4~3.6	V
	V_{REF} = 2.5	2.8~3.6	V
$V_{REF\_OUT\_ERROR}$	V_{REF} = 2.048	-2 / +1	mV
	V_{REF} = 2.5	-2 / +2	mV
I_{LOAD}	Max. load current	4	mA
I_{VDDA}	I_{LOAD} = 0 µA	16	µA
	I_{LOAD} = 500 µA	18	µA
	I_{LOAD} = 4 mA	35	µA
PSRR	DC	60	dB
t_{START}	C_{LOAD} = 1.1 µF	500	µs

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This table shows certain performance parameters for the VREF buffer. The VREF buffer can work from 2.4 to 3.6 V for a 2.048 V output, and 2.8 to 3.6 V for a 2.5 V output. The quiescent current is very small even with a 4 mA output current. It is possible to disable the VREF buffer when it is not being used. It can be available again 500 microseconds after it is re-enabled.
The Power supply rejection is 60 dB.

Related peripherals

- Refer to these trainings linked to this peripheral for more information:
  - Analog-to-digital converter (ADC)
  - Digital-to-analog converter (DAC)

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The STM32G0's analog-to-digital and digital-to-analog converters use this VREF Buffer output. Please refer to the training modules for these peripheral for additional information.