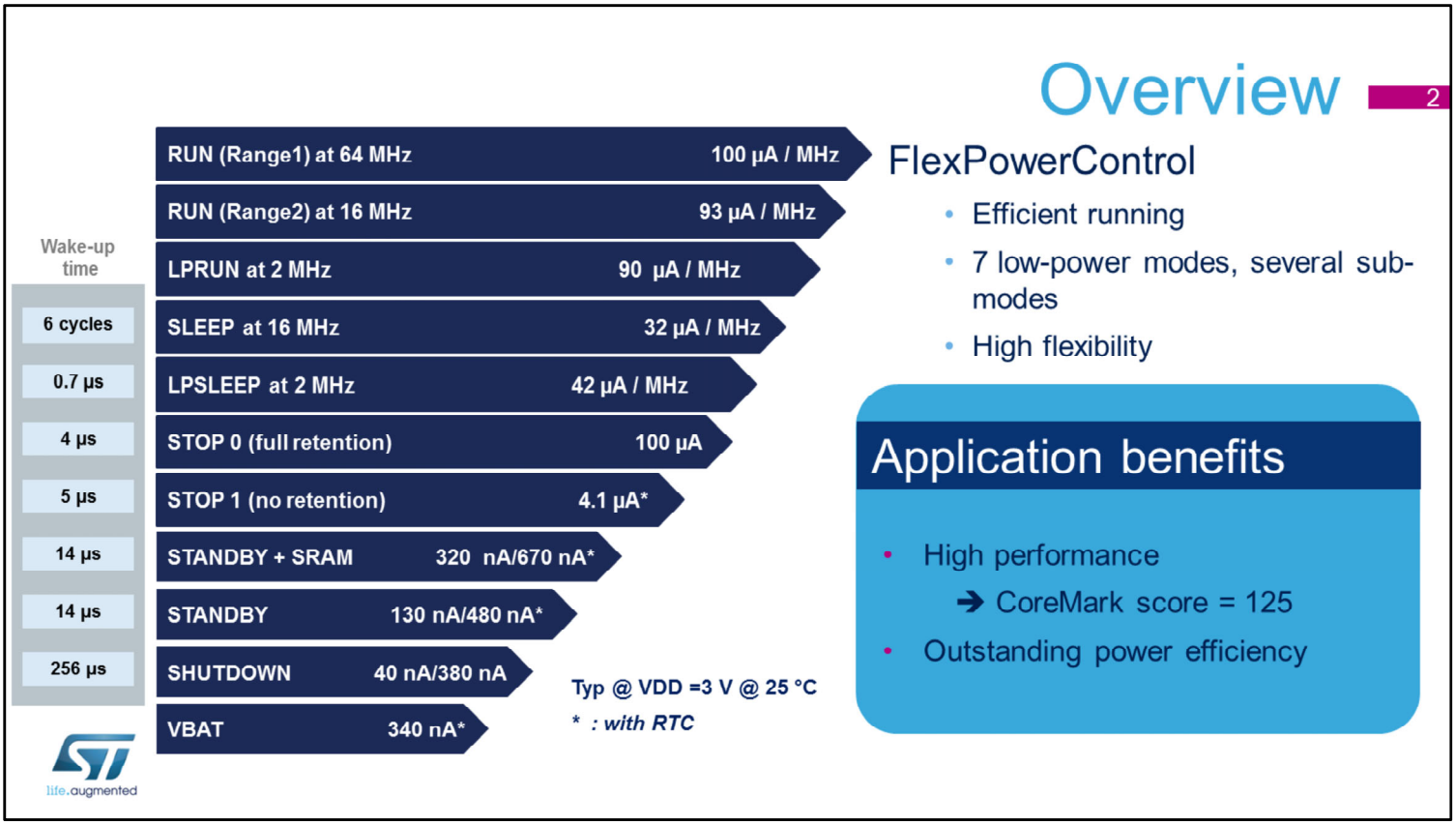
Hello, and welcome to this presentation of the STM32G0 power controller. The STM32G0's power management functions and all low power modes will also be covered in this presentation.



STM32G0 devices feature FlexPowerControl, which increases flexibility in power mode management and further reduces the overall application consumption. Run mode can support a system clock running at up to 64 MHz, with only 100 µA/MHz.
At 16 MHz, the consumption is even lower: 93 µA/MHz.
STM32G0 devices support 7 main low-power modes: Low-power run, Sleep, Low-power sleep, Stop 0, Stop 1, Standby and Shutdown modes.
Each mode can be configured in many ways, providing several additional sub-modes.
In addition, STM32G0 devices support a battery backup domain, called VBAT.
The high flexibility in power management provides both high performance with a CoreMark score equal to 125, together with an outstanding power efficiency.

Key features

- 7 low-power modes with fast wakeup
  - Down to 40 nA with I/O wake-up
  - Down to 320 nA with 36 KB RAM retained at 3.0V, 25 °C, RTC OFF
  - Wake-up from high number of peripherals
- 100 µA / MHz in Run mode at Maximum Frequency
- Battery backup mode with RTC and backup registers

Application benefits

- High flexibility to lower power consumption depending on active peripherals, required performance and needed wakeup sources
- Increase battery life
- BOM cost saving by removing external shifters

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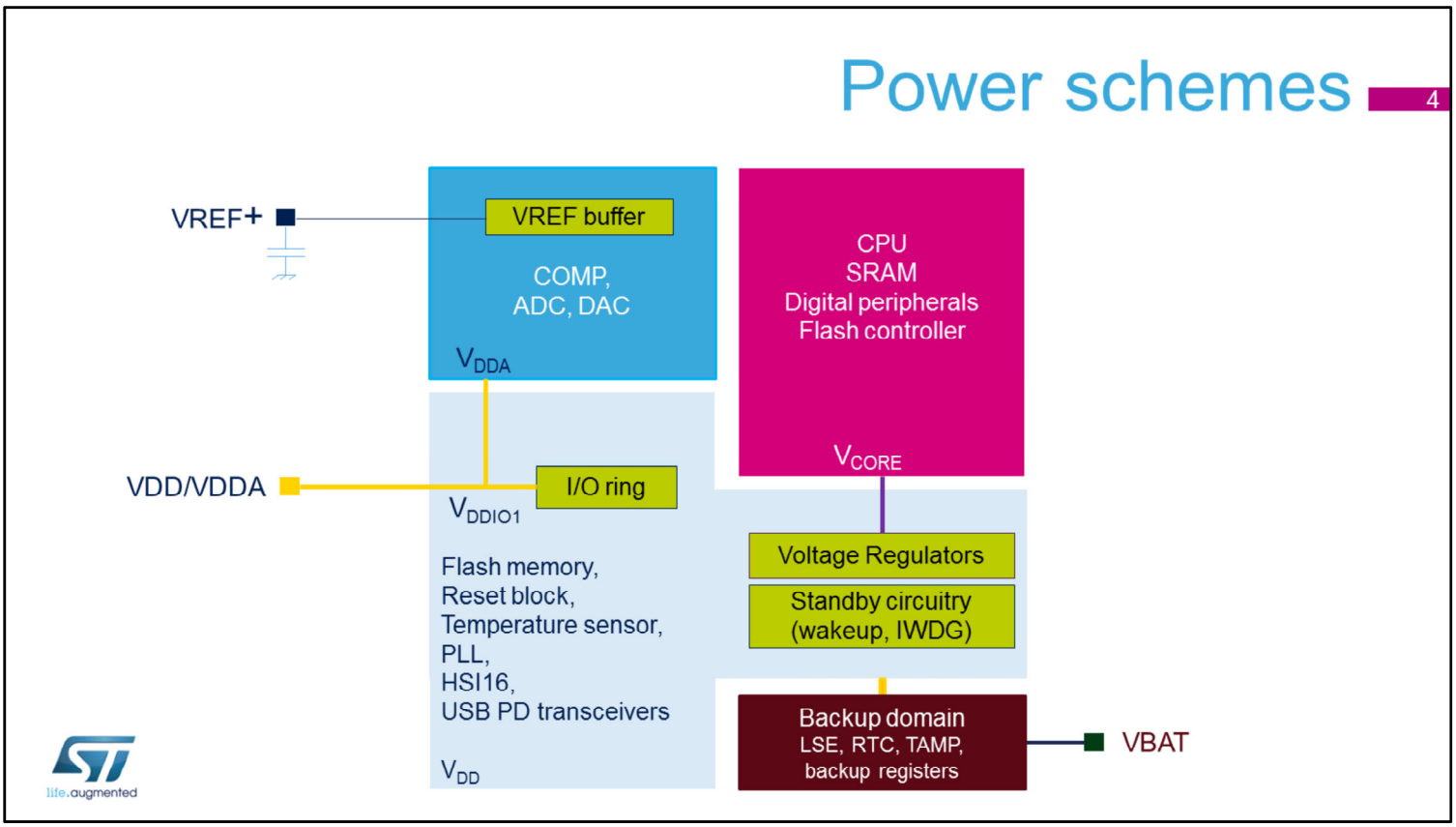
The STM32G0 has several key features related to power management:
Several low-power modes, down to 30 nA while it is still possible to wake up the MCU with an event on an I/O.
For only 320 nA, 36 kilobytes of SRAM can be retained assuming a 3.0V VDD power supply.
A large number of peripherals can wake up from the various low-power modes.
Dynamic consumption is down to 100 µA/MHz, executing from Flash memory.
A battery backup domain, called VBAT, including the RTC and certain backup registers.
Several power supplies are independent, allowing to reduce MCU power consumption while some peripherals are supplied at higher voltages.
Thanks to the large number of power modes, STM32G0 devices offer high flexibility to minimize the power

consumption and adjust it depending on active peripherals, required performance and needed wake-up sources.



STM32G0 devices have several independent power supplies, which can be set at different voltages or tied together. The main power supply is VDD, supplying almost all I/Os except those part of the VBAT domain . VDD also supplies the flash memory, the reset block, temperature sensor and all internal clock sources. In addition, it supplies the Standby circuitry which includes the wakeup logic and independent watchdog.
VDD supplies voltage regulators which provide the VCORE supply.
VCORE supplies most of the digital peripherals, SRAMs and Flash controller.
VDDA voltage is the same as the VDD one and supplies the analog peripherals.
The VREF+ pin provides the reference voltage to the analog-to-digital and to digital-to-analog converters and can be used as an external buffer reference for the

application.
A backup battery can be connected to VBAT pin to supply the backup domain.

Power schemes

- **Optimized power and performance thanks to independent power supplies**
  - V_{DD} from 1.71 to 3.6 V (down to 1.6 V at power-down)
    - VDD must be set if any other independent supply is provided
  - V_{DDA} from 1.71 to 3.6 V (down to 1.6 V at power-down)
    - 1.62 V min. when ADC or COMPs are used
    - 1.8 V min. when DAC is used
    - 2.4 V min. when VREFBUF is used
  - $V_{REF+} = V_{DDA}$ when $V_{DDA} < 2$ V and from 2V to V_{DDA} when $V_{DDA} > 2$ V
  - V_{BAT} from 1.55 to 3.6V for power domain including the RTC block and TAMP block, which contain the 20-byte backup registers

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The main power supply VDD ensures full feature operation in all power modes from 1.71 up to 3.6 V, allowing to be supplied by an external 1.8 V regulator. Device functionality is guaranteed down to 1.6 V, the minimum voltage after which a power-down reset is generated. Other independent supplies are provided to allow peripherals to operate at a different voltage.
The analog power supply VDDA is always connected to VDD. When the analog-to-digital converters or comparators are used, the VDDA voltage must be greater than 1.62 V. When the digital-to-analog converters is used, VDDA must be greater than 1.8 V. When the voltage reference buffer is used, VDDA must be greater than 2.4 V.
A backup domain is supplied by VBAT, which must be greater than 1.55 V. The backup domain contains the RTC, the 32.768-kHz LSE external oscillator and the

Tamp block containing the 20-byte backup registers.

Power schemes

Independent voltage reference supplies for analog performance

- VREF+: reference voltage for ADC and DAC
  - It can be provided either by an external reference voltage or by the internal voltage reference buffer (VREFBUF)
  - VREF+ pin, and thus the internal voltage reference, is not available on low pin count packages
    - On those packages, this pin is double-bonded with VDD
    - The internal voltage reference buffer is thus not available and must be kept disabled

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The ADC and DAC voltage references can be provided either by an external supply voltage or by the internal reference buffer.
This allows to improve converters performance by providing an isolated and independent reference voltage.
The VREF+ pin and thus the internal voltage reference, is not available on low pin count packages.
In those packages, the VREF+ pin is double-bonded with VDD/VDDA and the internal voltage buffer must be kept disabled. The voltage reference can be provided through the VDDA pin in those packages.

Power supply supervisor

7

- **Safe and ultra-low-power reset management**

- POR & PDR are always enabled in all modes except Shutdown mode
  - In Stop 0/1 and Standby mode, it can be activated periodically to decrease power consumption, this option is enabled by ULPEN bit
- Brown-out reset can be enabled in all modes except Shutdown mode when BOR_EN option bit is set
  - Ensure reset as soon as MCU power supply drops below selected threshold, regardless of the VDD slope
  - 5 thresholds selected by option byte **BORR_LEV[1:0]** and **BORF_LEV[1:0],** independently configurable for rising and falling edge.
- Power voltage detector active in all modes except Standby and Shutdown
  - 7 thresholds + external pin, independently configurable for rising and falling edges

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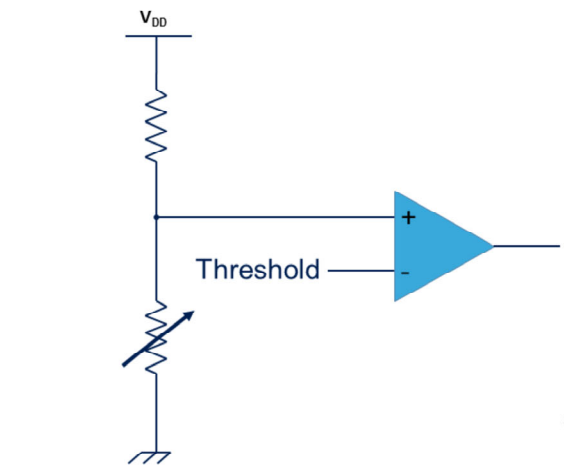
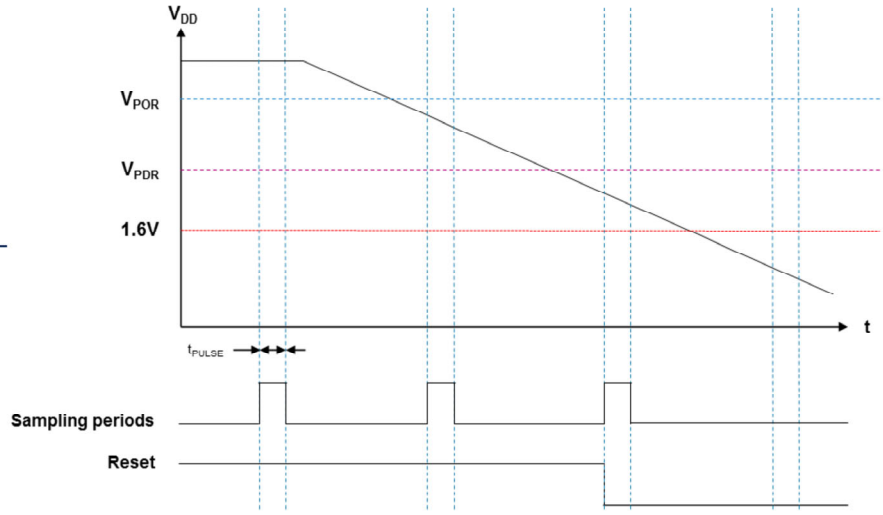
The power supply supervisor guarantees a safe and ultra-low power reset management.
STM32G0 devices embed a Power-On Reset (POR) and a Power-Down Reset (PDR) which are always enabled in all power modes except Shutdown mode.
STM32G0 devices embed an ultra-low-power Brown-Out Reset (BOR), which is active periodically instead of continuously monitoring the power voltage.
The BOR ensures reset generation as soon as the MCU power supply drops below the selected threshold, regardless of the VDD slope. Four thresholds from 2.0 to 2.95 V can be selected by option byte programmed in Flash memory independently for rising and falling edge. It can also be disabled to save power consumption.
A Power Voltage Detector (PVD) can generate an interrupt when VDD crosses the selected threshold. The PVD can be enabled in all modes except Standby and

Shutdown modes. Seven thresholds, independently configurable for rising and falling edges, can be selected by software. In addition, comparisons can be done between VREFINT and the PVD_IN external pin.

ULPEN feature

- The divider bridge necessary for PDR and BOR is only periodically connected





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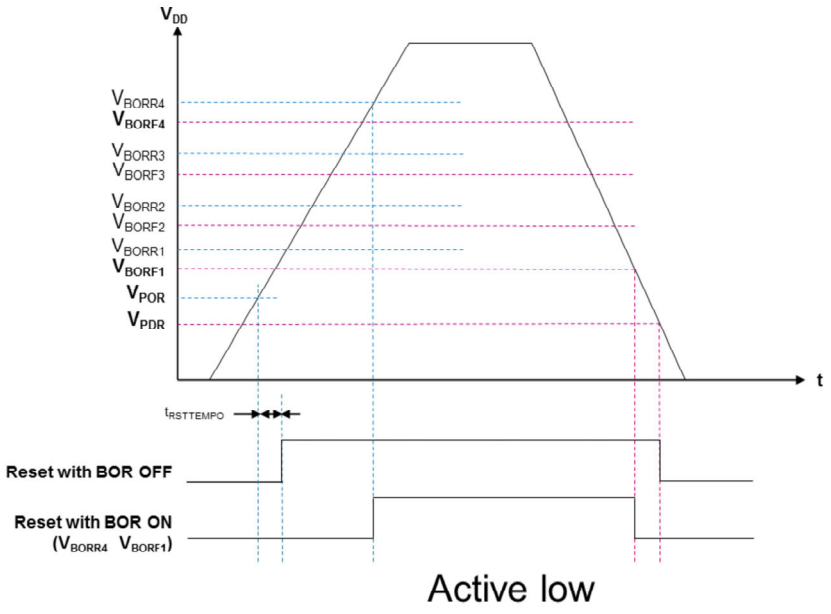
In the STM32G0 Devices, the Reset monitoring circuitry, BOR and POR/PDR can be enabled in a periodic sampling mode. This mode is activated by setting the ULPEN bit to one.
The resistor bridge necessary for their functionality is powered only during a short time periodically.
It reduces consequently the power consumption.

Brown Out and Power On/Down Reset

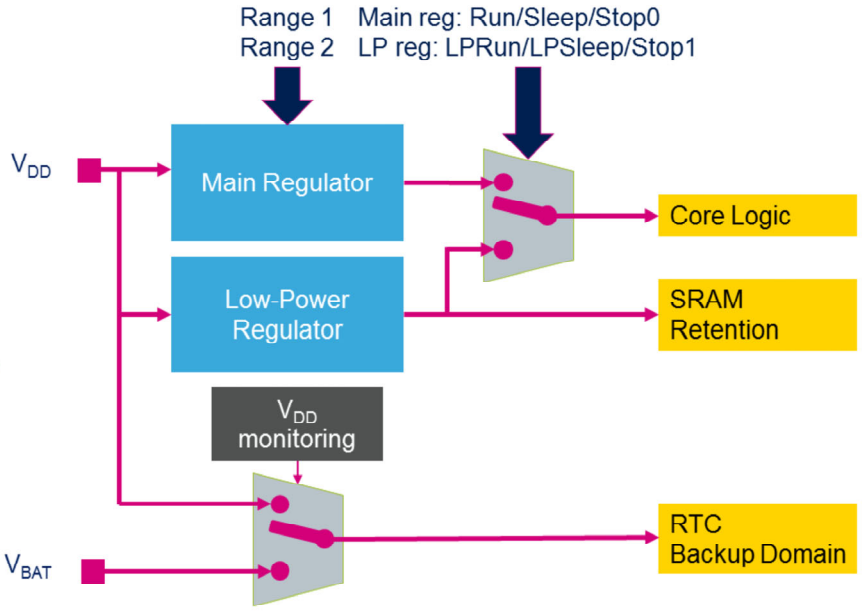
- The Brown-out reset can have rising and falling threshold selected independently
- POR/PDR always On, except in shutdown mode
- BOR is enabled or disabled by option bytes



The Power reset (BOR and POR) resets all registers except those in the Backup domain powered by VBAT which contains the RTC and TAMP blocks and the external low-speed oscillator LSE.
When exiting Standby mode, all registers powered by the Main regulator are reset.
When exiting Shutdown mode, a Power reset is generated.
When the BOR is enabled, four BOR levels can be selected through option bytes with independent configuration for rising and falling thresholds.
The Backup domain reset occurs when the BDRST bit is set in the RCC Backup Domain control register.
It also occurs when VDD and VBAT are powered on if both supplies have previously been powered off. It resets the RTC and TAMP registers, the Backup registers, and the RCC Backup Domain Control Register.

Voltage regulators

- Two Voltage Regulators
- One Main regulator with two voltage ranges for Dynamic Voltage Scaling; used in Run, Sleep and Stop 0 modes
- One Low-power regulator for Low-power run, Low-power sleep and Stop modes as well as for RAM retention in Standby



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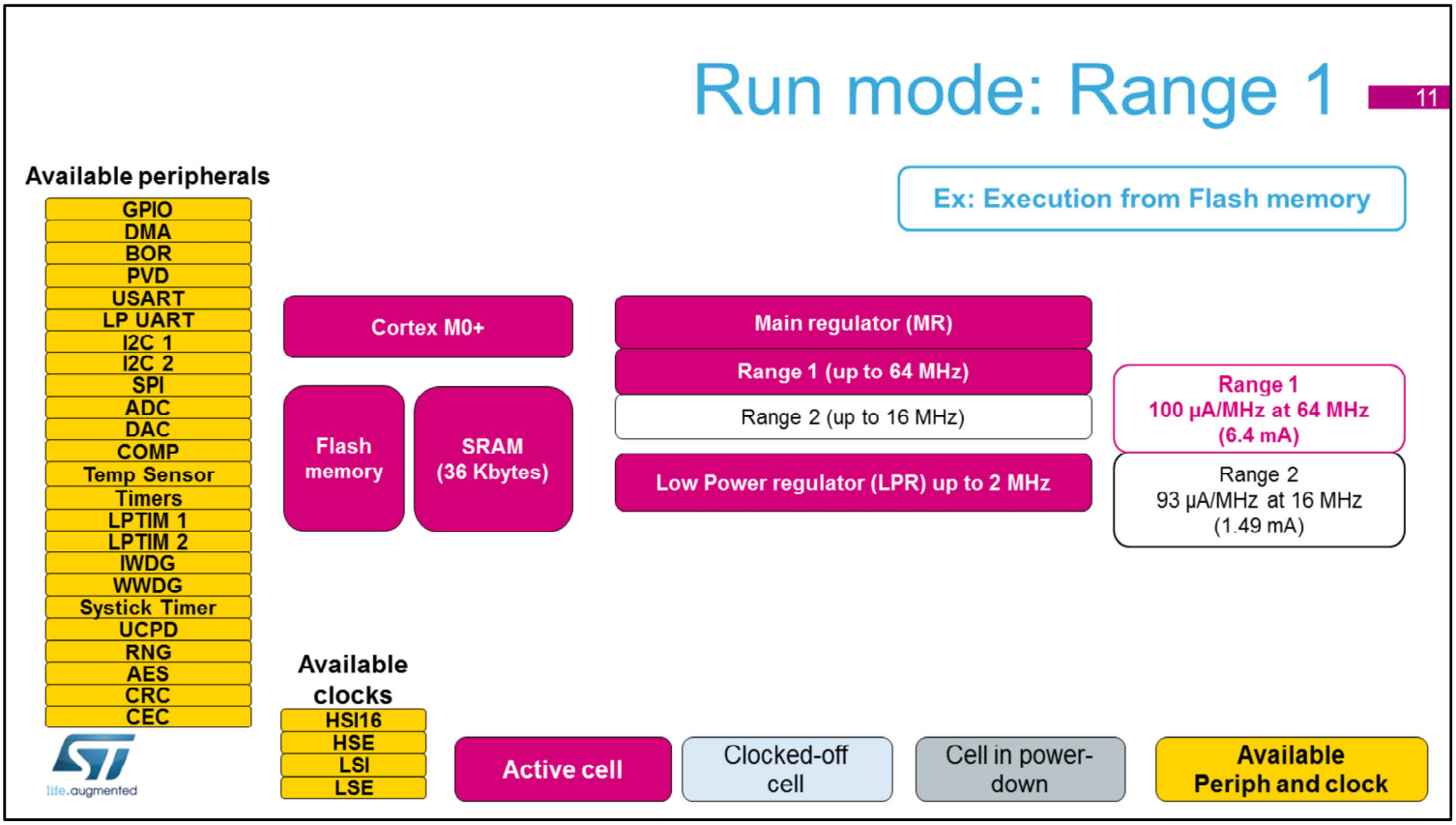
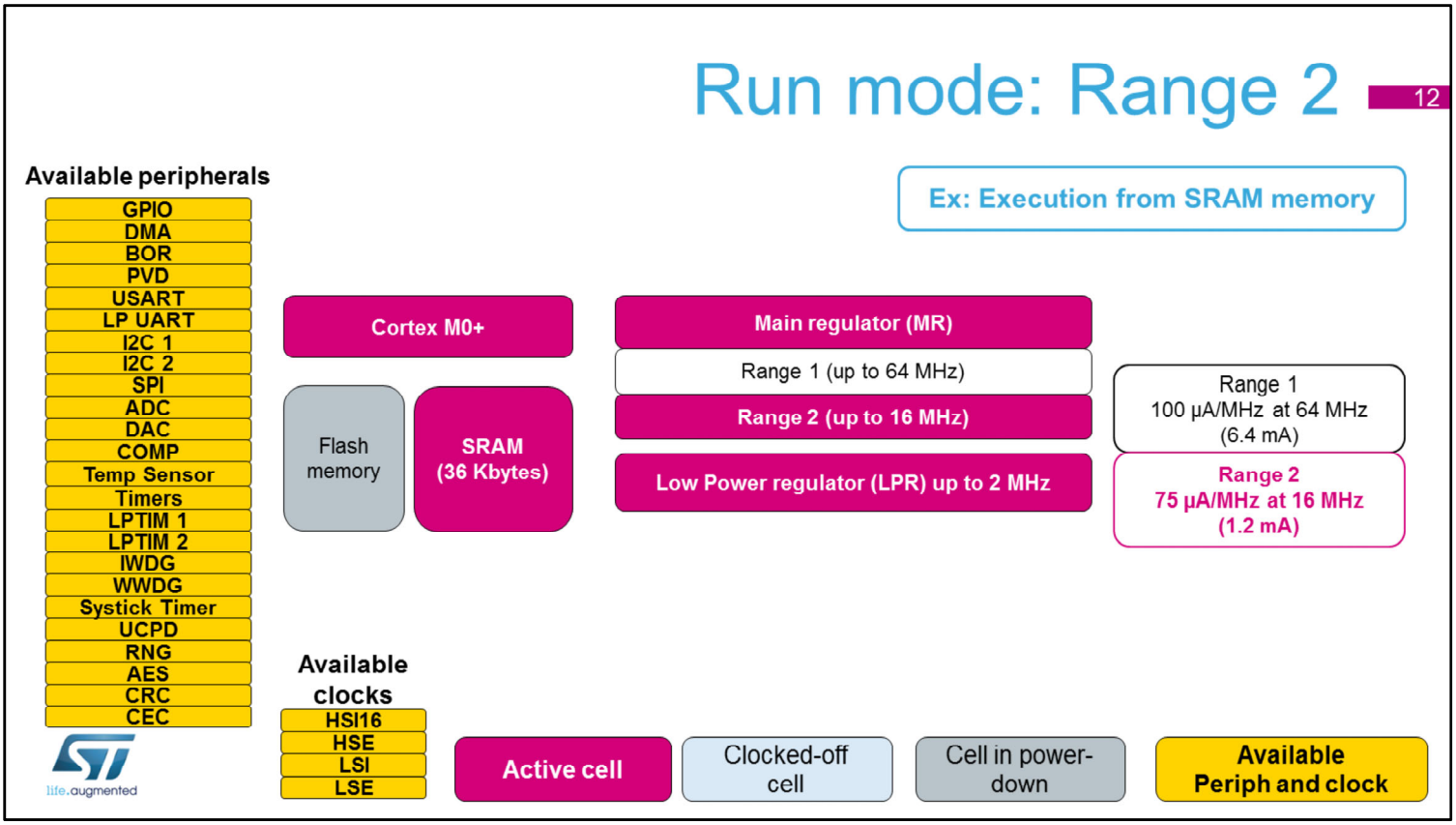
Two embedded linear voltage regulators supply all the digital circuitries except for the Standby circuitry and the Backup domain. The regulator output voltage (V_{CORE}) can be programmed by software to two different values depending on the performance and the power consumption requirements. This is called Dynamic Voltage Scaling.

Depending on the application mode, V_{CORE} is provided either by the Main voltage regulator for Run, Sleep and Stop0 modes, or by the Low-power regulator for Low-power run, Low-power sleep, Stop 1 modes.

The regulators are OFF in Standby and Shutdown mode. When SRAM content is preserved in Standby mode, the Low-power regulator remains ON and provides the SRAM supply.

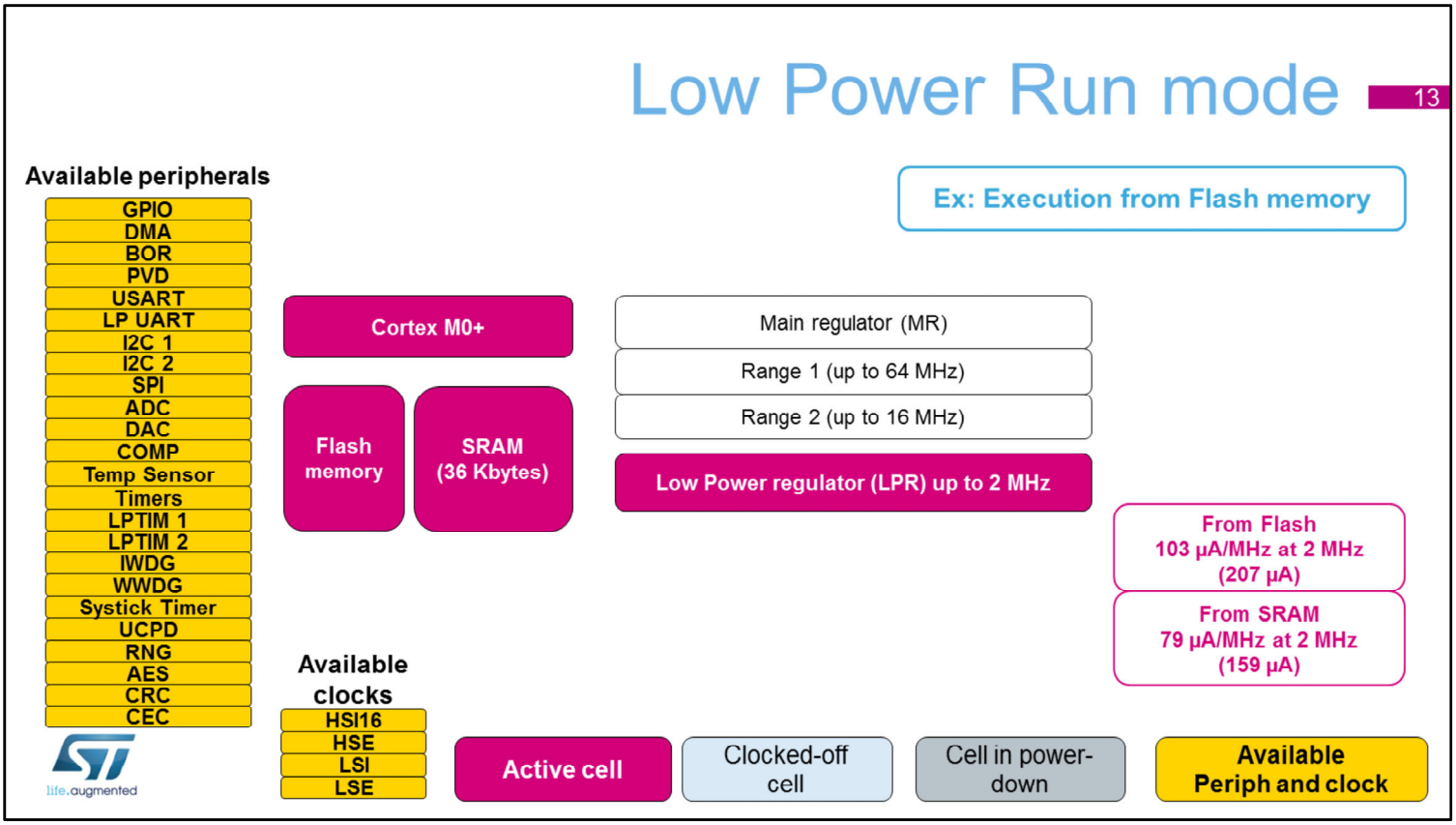


In Run mode, the CPU is clocked and program can be executed from FLASH or SRAM Memory.
In Range 1, the system clock is up to 64 MHz, in Range 2 it is up to 16 MHz.
By default, the SRAM clock is enabled. It can be gated off during Sleep mode by software.
All peripherals can be activated in Range 1.
The Run mode consumption is 100 µA/MHz in Range 1 at 64 MHz with the Flash memory ON at 25°C.



In Range 2, all peripherals can be active but the FLASH Memory cannot be programmed or erased.
The Run mode consumption is 75 µA/MHz in Range 2 at 16 MHz with the Flash memory OFF.

Low Power Run mode



In Low Power Run mode, the CPU is clocked and program can be executed from FLASH or SRAM, additionally the FLASH can be completely unpowered to save power.
The system clock is limited to 2 MHz. The Main Regulator is switched off and supply to digital blocks is provided by the Low Power Regulator.
In Low Power mode, all peripherals can be active.

Run and Low-power run modes

Flexibility between required performance and consumption

Voltage range	SYSCLK	HSI16	HSE	PLL
Range 1	64 MHz max	16 MHz	48 MHz	128 MHz VCO max = 344 MHz
Range 2	16 MHz max	16 MHz	16 MHz	40 MHz VCO max = 128 MHz
Low-power run	2 MHz max	Allowed with divider	Allowed with divider	Not allowed

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The Run mode, thanks to voltage scaling, and the Low-power run modes offer flexibility between required performance and consumption.
In Run mode range 1, the system clock is limited to 64 MHz and the internal and external oscillators and the PLL can be used.
In Run mode range 2, the system clock is limited to 16 MHz and the internal and external oscillators as well as the PLL can be used, but must be limited to 16 MHz.
In Low-power run mode, the system clock must be limited to 2 MHz.

Run and Low-power run modes

- Each peripheral clock can be configured to be ON or OFF
  - After reset, all peripheral clocks are OFF, except Flash interface clock
  - SRAM clock is always ON in Run mode
- When running from SRAM (in Run or Low-power run):
  - Flash memory can be put in Power-down mode (only in Low-Power run)
  - Flash interface clock can be switched off
  - Interrupt vectors must then be re-mapped to SRAM

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Each peripheral clock can be configured to be ON or OFF in Run and Low-power run modes.
By default all peripherals clocks are OFF, except the Flash interface clock.
The SRAM clock is always ON in Run mode.
When running from SRAM (in Run or Low-power run modes), the Flash memory can be put in Power-down mode thanks to software, and the Flash clock can be switched off.
The Flash memory must not be accessed when it is switched off, consequently interrupt vectors must be mapped in SRAM, using the Cortex-M0+ Vector Table Offset Register.

Run and Low-power run modes

- Current consumption in Run mode depends on several parameters:
  - Executed binary code (program itself + compiler impact)
  - Program location in memory (depending on address of executed code)
  - Device configuration (depending on application)
  - I/O pin loading and switching rate
  - Temperature
  - Execution from Flash memory or SRAM
    - When execution from Flash memory: Accelerator configuration (Cache, Prefetch)
    - ➢ Energy efficiency better with Prefetch + Cache ON
    - When execution from SRAM:
    - ➢ Energy efficiency better versus Flash

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The current consumption in Run or Low-power run modes depends on several parameters: first the executed binary code, that means the program itself plus the compiler impact. Then it depends on the program location in the memory, the device software configuration, the I/O pin loading and switching rate and the temperature.
The consumption also depends on whether the code is executed from Flash memory or from SRAM. Energy efficiency is better when the Flash prefetch and the instruction cache are enabled . Executing from flash consumes more than executing from SRAM because the flash memory belongs to the VDD power domain while the SRAM belongs to the Vcore power domain.

Sleep and Low-power sleep modes

All peripherals available and fastest wakeup time

- Core is stopped, each peripheral clock can be gated ON or OFF
- Entered by executing **WFI** (Wait For Interrupt) or **WFE** (Wait For Event)
- Two mechanisms to enter this mode:
  - **Sleep Now**: MCU enters Sleep mode as soon as WFI/WFE instruction are executed
  - **Sleep on Exit**: MCU enters Sleep mode as soon as it exits the lowest priority Interrupt Service Routine
    - The stack is not popped before entering Sleep mode, it will not be pushed when the next interrupt occurs, saving running time
  - Controlled by Cortex-M0+ **System Control Register [SLEEPONEXIT]**

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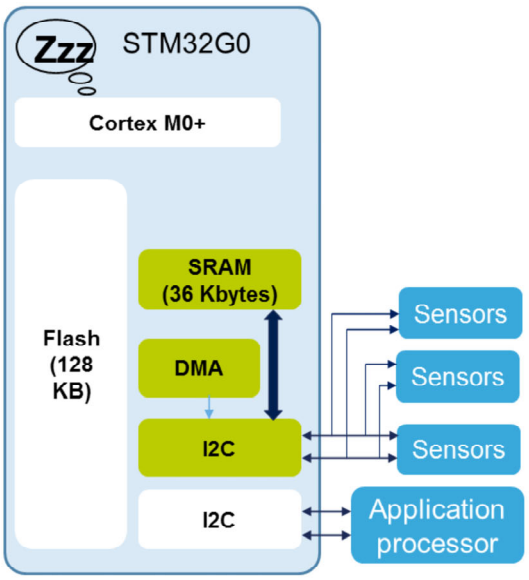
Sleep and Low-power sleep modes allow all peripherals to be used and features the fastest wakeup time.
In these modes, the CPU is stopped and each peripheral clock can be configured by software to be gated ON or OFF during the Sleep and Low-power sleep modes.
These modes are entered by executing the assembler instruction Wait for Interrupt (WFI) or Wait for Event (WFE). When executed in Low-power run mode, the device enters Low-power sleep mode.
Depending on the SLEEPONEXIT bit configuration in the Cortex®-M0+ System Control Register, the MCU enters Sleep mode as soon as the instruction is executed, or as soon as it exits the lowest priority Interrupt Sub Routine.
This last configuration allows to save time and consumption by saving the need to pop and push the stack when exiting the low power mode. However all computations must be done in Cortex®-M0+ handler

mode, because the thread mode is no longer used .

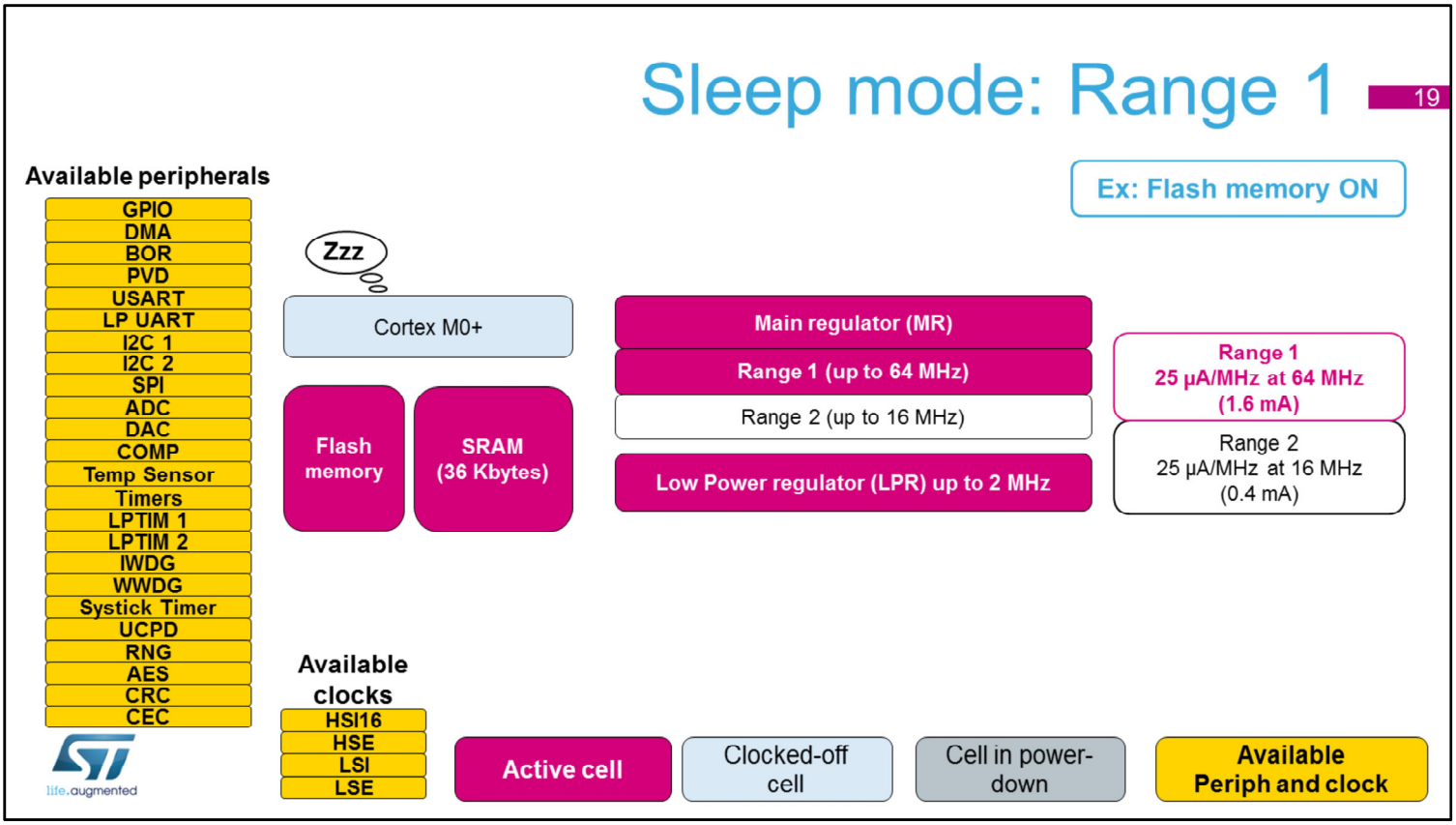
Batch Acquisition mode (BAM)

Optimized mode for transferring data with communication peripherals, while the rest of the device is in low power.

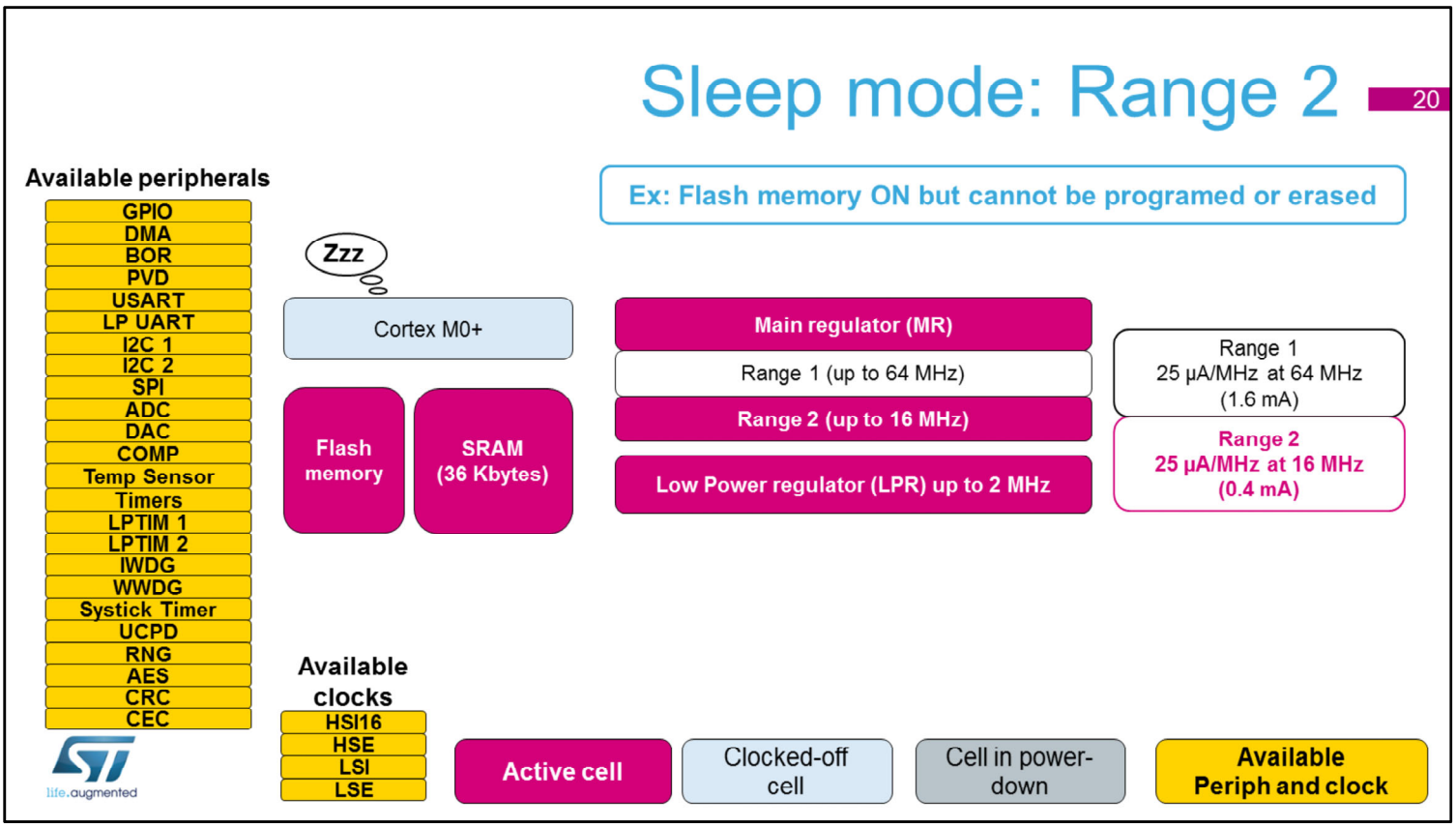
1. Only the needed communication peripheral + DMA + SRAM are configured with clock enabled in Sleep mode
2. Flash memory is put in Power-down mode and Flash clock is gated off during Sleep mode
3. Enter either Sleep or Low-power sleep mode
   - Note that the I2C clock can be at 16 MHz even in Low-power sleep mode, allowing 1 MHz Fast-mode Plus support. U(S)ART/LPUART clock can also be HSI16.



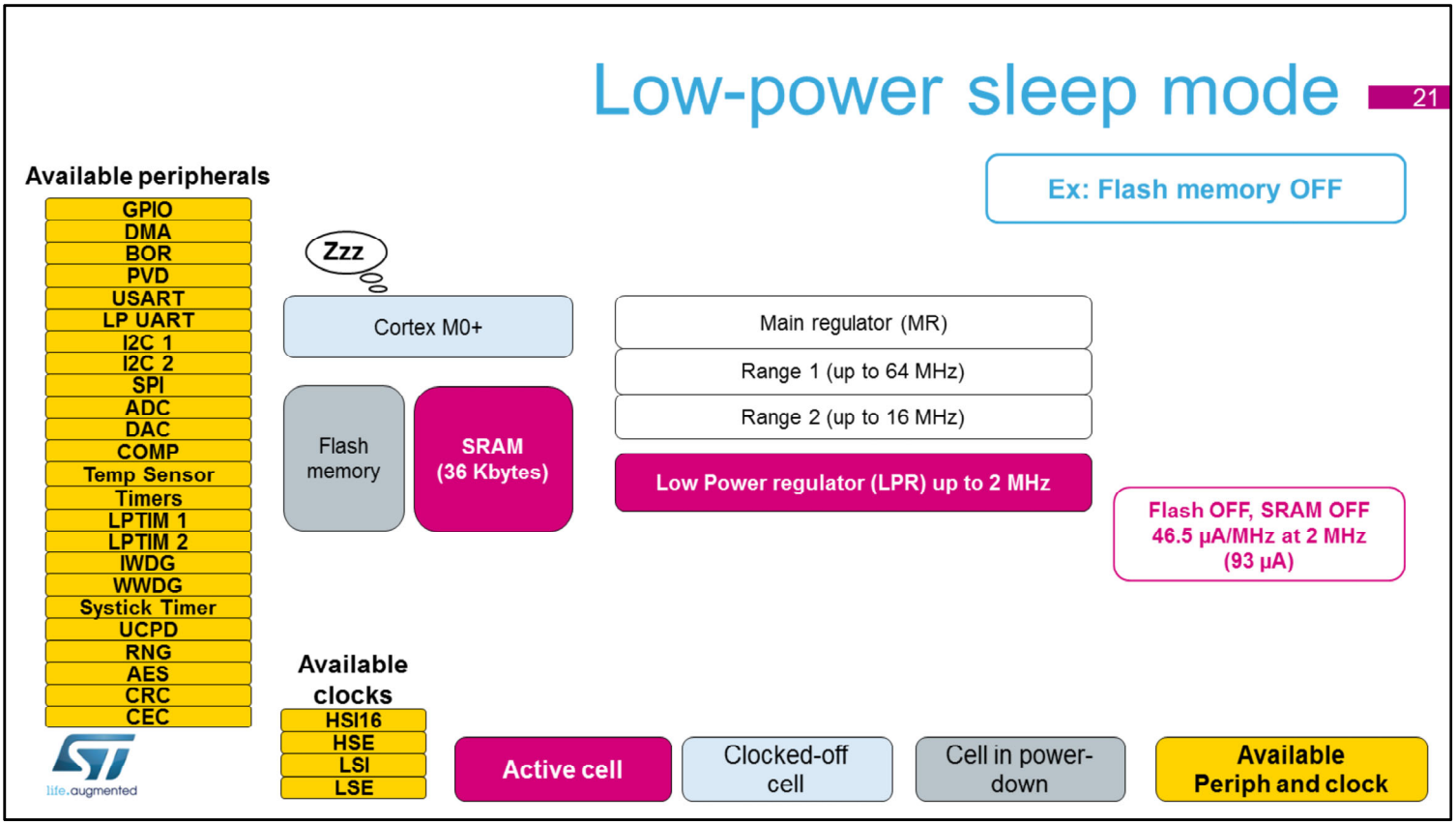
Batch Acquisition Mode is an optimized mode for transferring data.
Only the needed communication peripheral + DMA + SRAM configured with clock enabled in Sleep mode.
Flash memory is put in Power-down mode and the Flash memory clock is gated off during Sleep mode.
Then it can enter either Sleep or Low-power sleep mode.
Note that the I2C clock can be at 16 MHz even in Low-power sleep mode, allowing support for 1-MHz Fast-mode Plus. The USART and LPUART clocks can also be based on the high-speed internal oscillator. Typical applications are sensor hubs.



In Sleep mode, the CPU clocks are OFF.
In Range 1, the system clock is up to 64 MHz, in Range 2 it is up to 16 MHz.
By default, the SRAM clock is enabled. It can be gated off during Sleep mode by software.
All peripherals can be activated in Range 1. The Sleep mode consumption is 25 µA/MHz in Range 1 at 64 MHz with the Flash memory ON.



In Range 2, all peripherals can be activated but the Flash Memory cannot be programmed or erased.
The Sleep mode consumption is 25 µA/MHz in Range 2 at 16 MHz with the Flash memory ON.



In Low-power sleep mode, the CPU clock is OFF and the logic is supplied by the low-power regulator. The system clock is up to 2 MHz.
Flash memory can be configured in Power down and can be gated off; SRAM can be gated off.
All peripherals can be active.
The Low-power sleep mode consumption is 46.5 µA/MHz at 2 MHz with Flash memory disabled.

Stop modes

Lowest power modes with full retention, 5 µs wakeup time to 16 MHz

- SRAM and all peripheral registers retention
  - All high-speed clocks are stopped
  - Flash can be switched OFF
- LSE (32.768 kHz external oscillator) and LSI (32 kHz internal oscillator) can be enabled
- Several peripherals can be active and wake up from Stop modes
- System clock at wakeup is HSI16 (2 µs wakeup time on RAM, 5.5µs on FLASH not powered)
- Stop 1 is equivalent to Stop 0 with Main Regulator off, resulting in a smaller current consumption but longer wake up time

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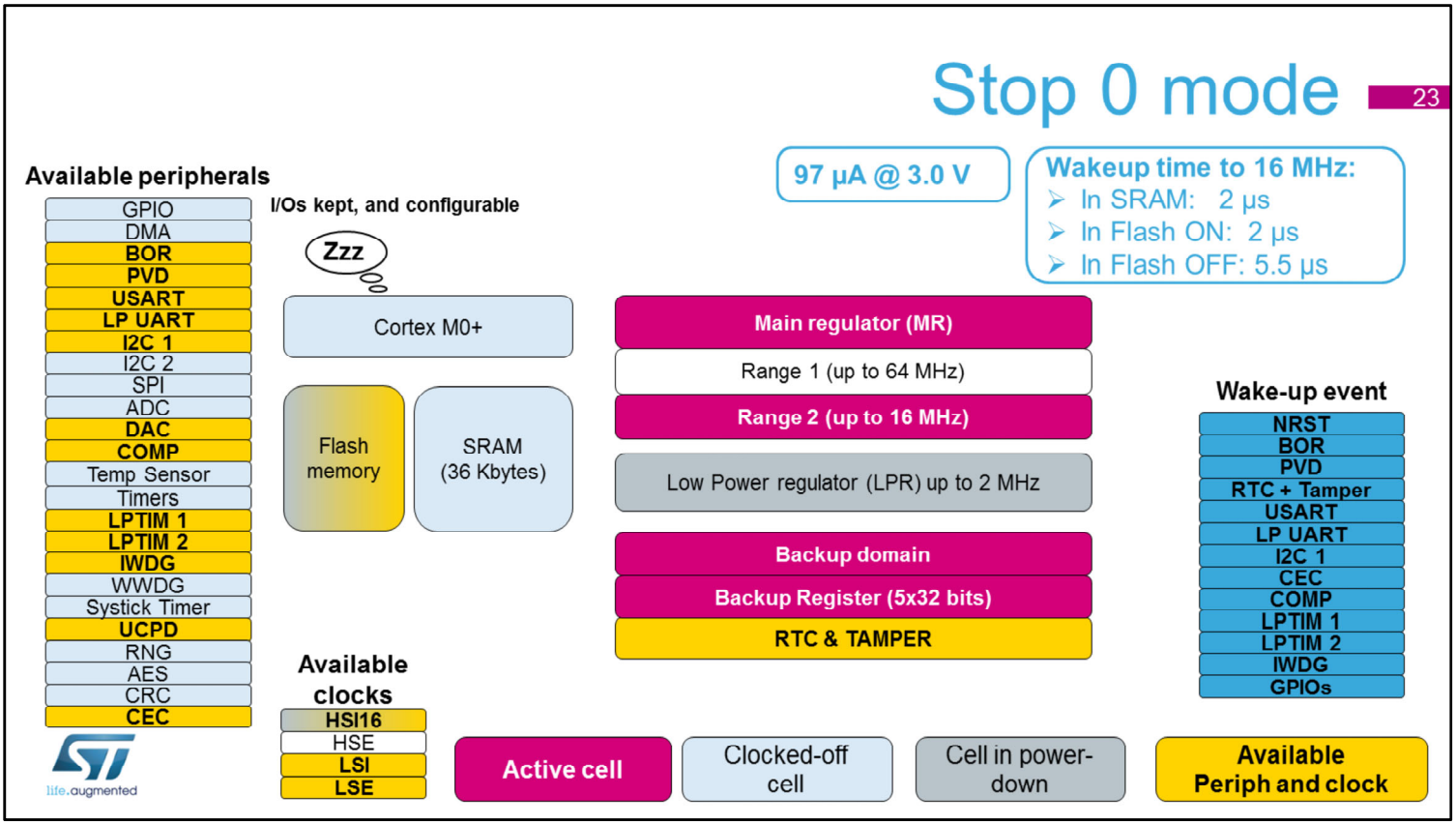
STM32G0 devices features two Stop modes: Stop 0, and 1, which are the lowest power modes with full retention and only a 2-µs wakeup time to Run mode at 16 MHz.
The contents of SRAM and all peripherals registers are preserved in Stop modes.
All high speed clocks are stopped.
The 32.768 kHz external oscillator and 32 kHz internal oscillator can be enabled.
Several peripherals can be active and wake up from Stop mode.
System clock on wake-up is the internal high-speed oscillator at 16 MHz with only a 2-µs wakeup time from RAM or 5µs from FLASH, the divider configuration to SYSCLK is kept upon wake-up.
Stop 1 is similar to Stop 0 with the Main regulator switched OFF.



The voltage regulator is configured in main regulator mode

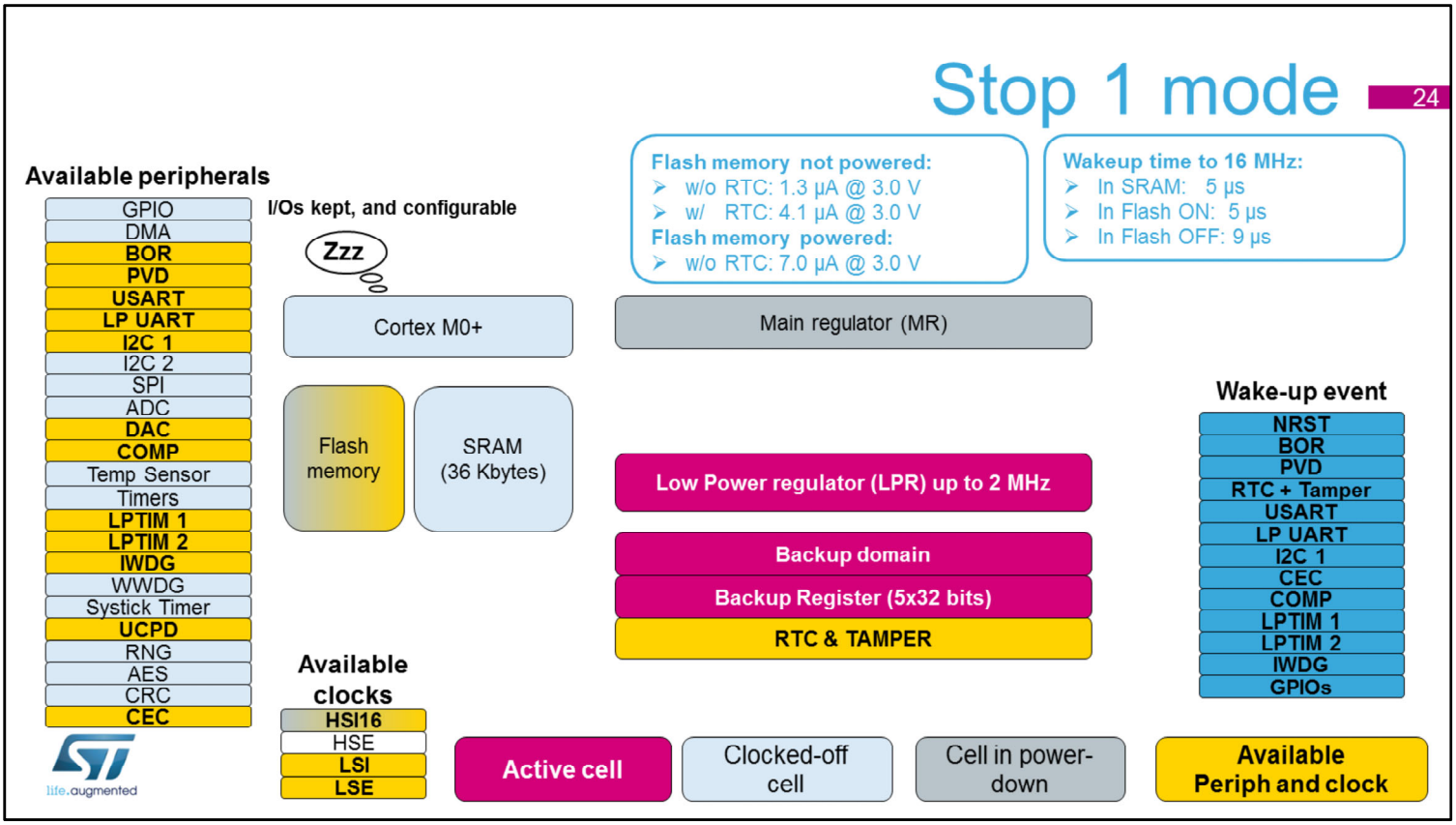
All clocks in the VCORE domain are stopped; the PLL, the HSI16 and the HSE oscillators are disabled.

The RTC, clocked by the internal or external low-speed oscillator, can remain active.

The brown-out reset is always enabled. Most of the peripheral clocks are gated off. Several peripherals can be functional in Stop 0 mode: Power voltage detector, digital to analog converters, comparators, independent watchdog, low power timers, I2C, UART and low-power UART.

The events from all I/Os can wake up from Stop 0 mode, as well as the interrupt generated by the active peripherals. The I2C and UART, HDMI CEC or LPUART can switch the HSI16 ON during the Stop mode in order to recognize their wakeup condition and switch off the

HSI16 after receiving the frame if it is not a wakeup frame. In this case, the HSI16 clock is propagated only to the peripheral requesting it.
The Stop 0 mode consumption typical at 3V is 97 µA when HSI is disabled, 276 µA when HSI is enabled.
The wakeup time is 2 µs and the system clock at wakeup is HSI at 16 MHz assuming execution in SRAM or in powered Flash memory.
It is 5.5 µs when execution is from the initially non-powered flash.
Flash memory as well as HSI16 are configurable: they can be stopped or kept enabled.



Stop 1 mode is very similar to Stop 0 except that the power figures are much lower as the main regulator is stopped and replaced by the low Power Regulator.
The Stop 1 mode consumption without RTC is 1.3 µA typical at 3V when flash is not powered and RTC is disabled.
The wakeup time is 5 µs with the HSI 16MHz as system clock at wakeup, regulator in range 1 or 2.
Flash memory as well as HSI16 are configurable: they can be stopped or kept enabled.

Stop modes comparison

	STOP0	STOP1
Consumption	25 °C, 3 V	
	97 µA	1.3 µA when RTC is disabled
Wakeup time to 16 MHz	5.5 µs in Flash memory initially powered down 2 µs in RAM	9 µs in Flash memory initially powered down 5 µs in RAM
Wakeup clock	**HSI16** at **16 MHz**	
Regulator	Main regulator	Low power regulator
Peripherals	RTC, I/Os, BOR, PVD, COMPs, IWDG	
	2 LP TIMERs 1 LP UART (Start, address match or byte reception) 2 U(S)ARTx (Start, address match or byte reception) 1 I2C (address match)	

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When comparing Stop modes:
Stop 0 mode consumption is higher than Stop 1 mode consumption, but the wakeup time is shorter and the number of active peripherals is higher.
Stop 0 mode keep the Main regulator enabled, allowing a very short wake-up time of 2µs when restarting from the RAM to the expense of a higher consumption than Stop 1.
The I2C address recognition is functional in both Stop modes, and can generate a wakeup event in case of an address match.
The UART and LPUART byte reception is functional in both Stop modes and can generate a wakeup event in case of Start detection or Byte reception or Address match event.
When clocked by the internal or external low-speed oscillator, or when clocked by an external pin, the low-

power timer can wake up the MCU with all its events.

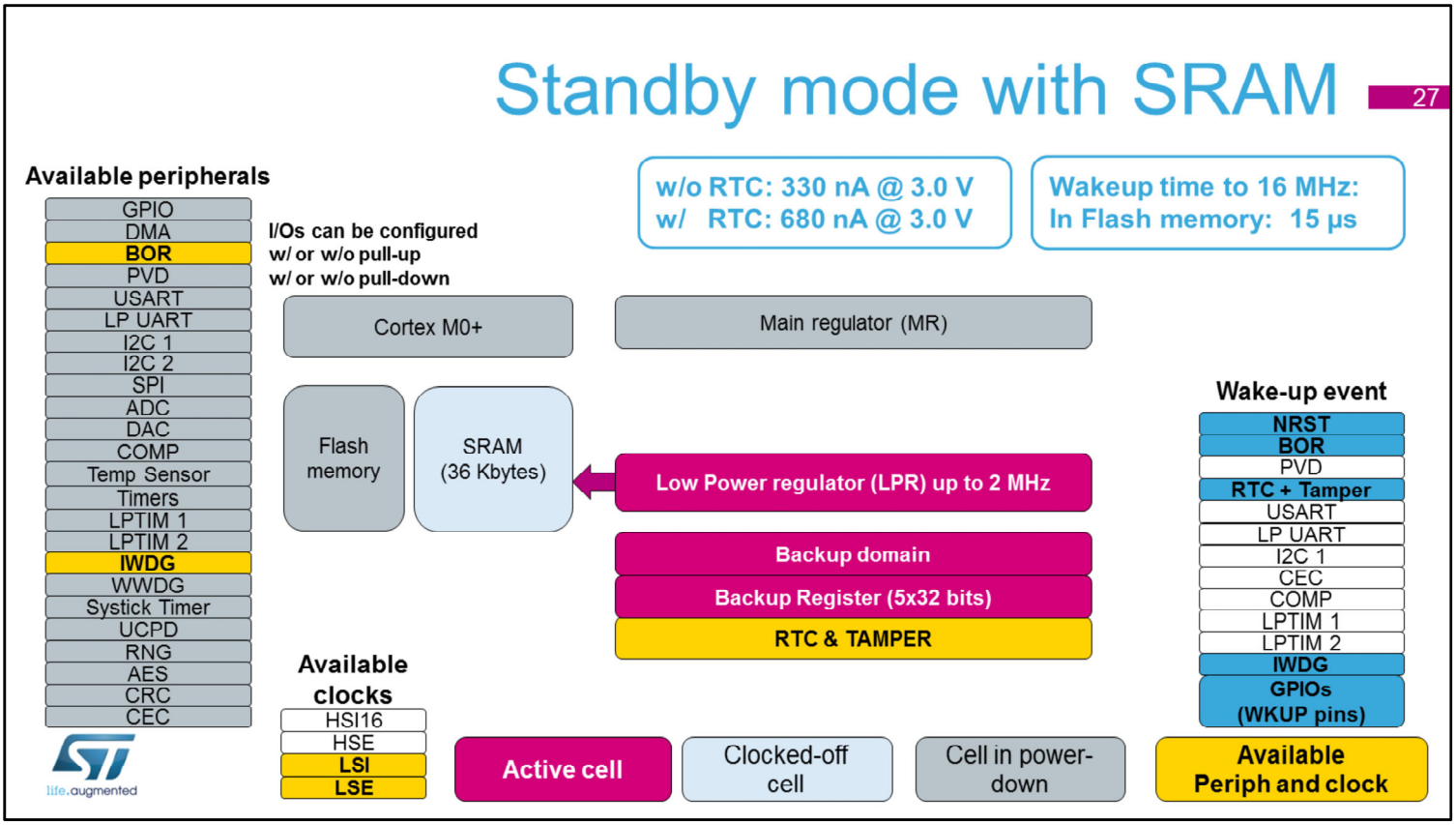
Standby mode

Lowest power mode with SRAM retention, switch to VBAT and I/O control

- By default: neither SRAM nor registers retention (voltage regulators in power down)
  - 20-byte backup registers always retained
- **Possibility to retain the entire SRAM (36 Kbytes)**
- **Ultra Low Power BOR configurable**: safe reset regardless of VDD slope, with a ULP mode to reduce consumption for glitch free applications
- Configurable **pull-up** or **pull-down** for each I/O
  - PWR_PUCRx / PWR_PDCRx registers (x = A,B,…F), applied when **APC** is set in PWR_CR3 register
  - **Allows to control external component inputs state**
- **5 wakeup pins**: the polarity of each wakeup pins is configurable
- Wakeup clock is **HSI16 at 16 MHz**

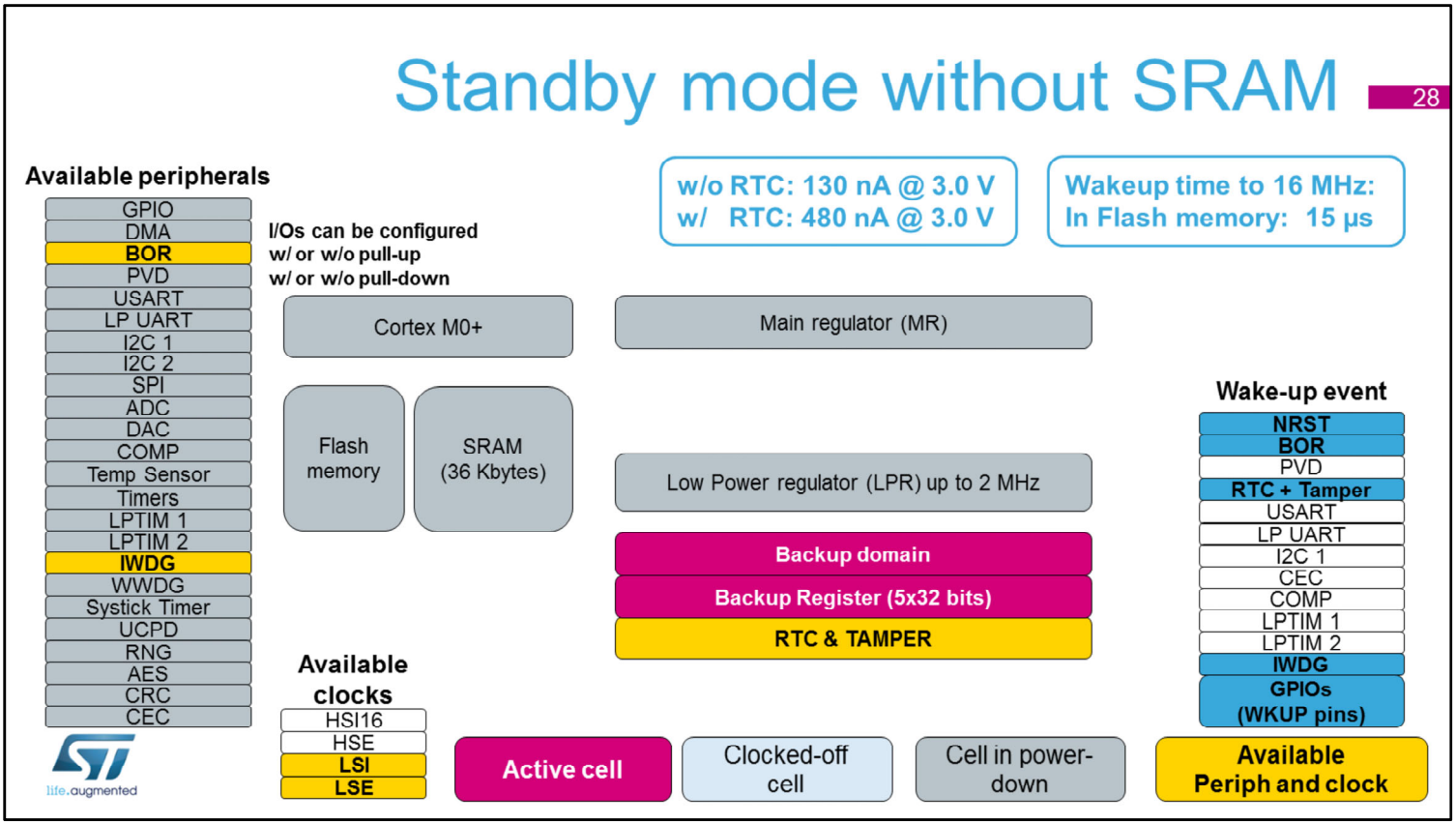
The Standby mode is the lowest power mode in which 36 Kbytes of SRAM can be retained, the automatic switch from VDD to VBAT is supported and the I/Os level can be configured by independent pull-up and pull-down circuitry.
By default, the voltage regulators are in Power down mode and the SRAM contents and peripherals registers are lost. The 20-byte backup registers are always retained.
The ultra low power Brown-Out Reset (BOR) is available in Standby mode. The Power Down Reset is always ON to ensure a safe reset regardless of the VDD slope..
Each I/O can be configured with or without a pull-up or pull-down, which is applied and released thanks to the APC control bit. This allows to control the inputs state of external components even during Standby mode.
5 wakeup pins are available to wake up the device from

Standby mode. The polarity of each of the 5 wakeup pins is configurable.
The wakeup clock is HSI with a frequency of 16 MHz.

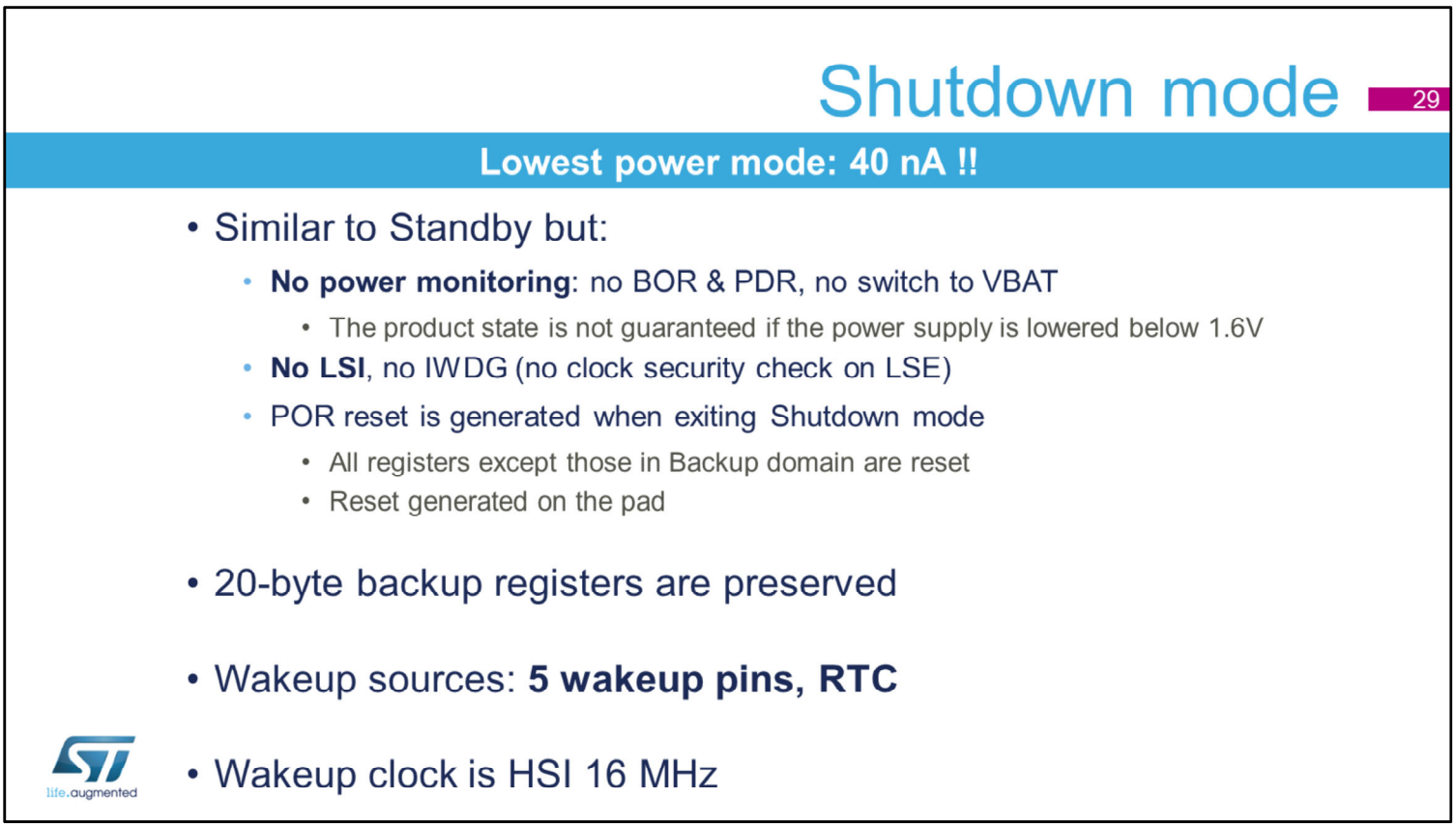


In Standby mode with SRAM, the main regulator is powered down and the low power regulator supplies the SRAM to preserve its content.
The RTC, clocked by the internal or external low-speed oscillator, may remain active .
The brown-out reset can be enabled. The independent watchdog can also be enabled in Standby mode.
Reset, brown-out or Power down reset, RTC and tamper detection, independent watchdog and any event on the 5 wakeup pins can exit the MCU from Standby mode.
The Standby mode with SRAM consumption without the RTC is around 330nA typical at 3 V. The wakeup time is approximately 15 µs.

Standby mode without SRAM

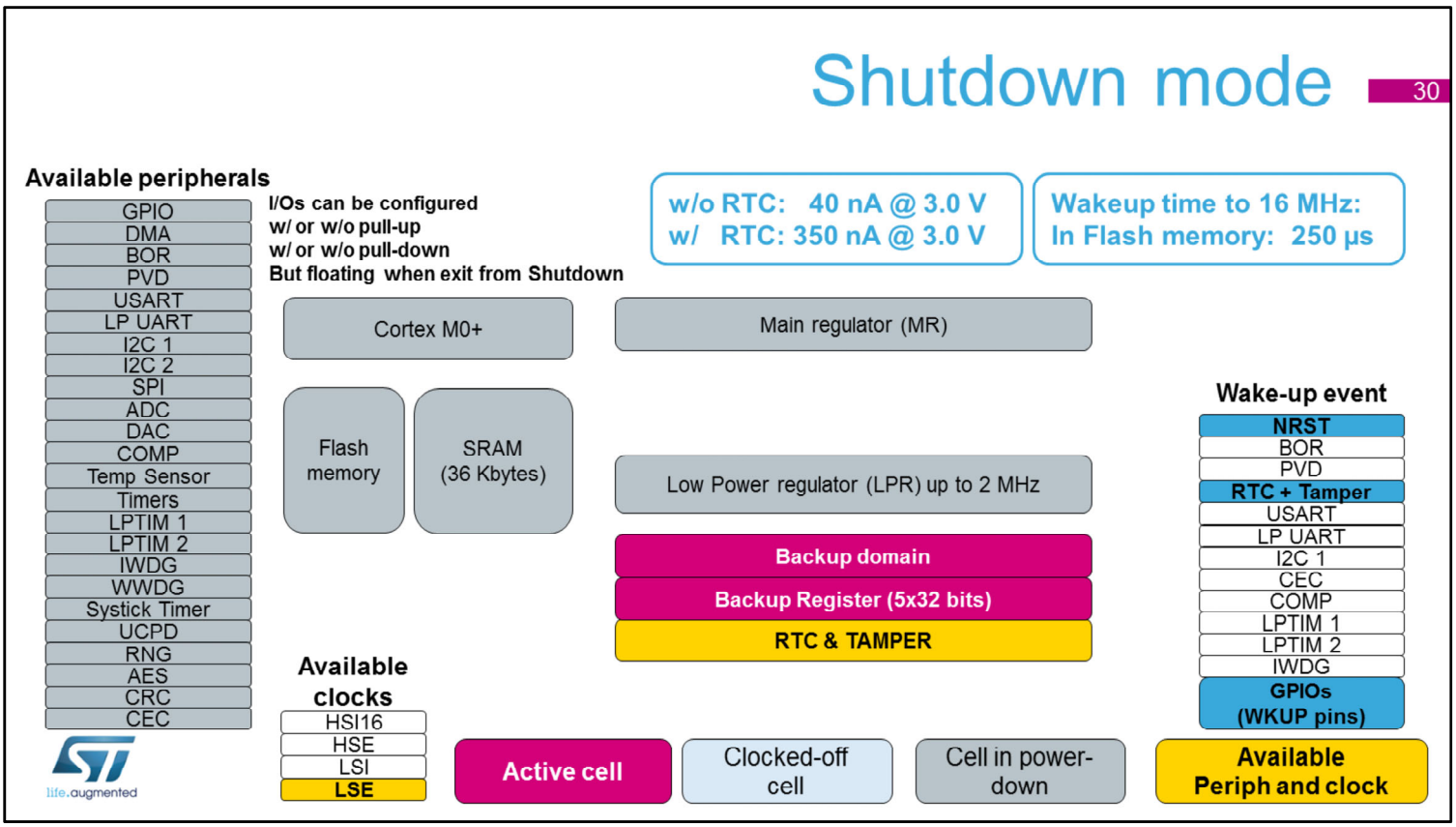


In Standby mode without SRAM retention, both main and low power regulators are powered down.
Wake-up events and available peripherals as well wake-up sources are the same as in Standby mode with SRAM.



The shutdown mode is the lowest power mode of the STM32G0, with only 40 nA at 3.0 V.
This mode is similar to Standby mode but without any power monitoring: the power down reset is disabled and the switch to VBAT is not supported in Shutdown mode. Hence the product state is not guaranteed in case the power supply is lowered below 1.6V.
The LSI is not available, and consequently the independent watchdog is also not available.
A power reset is generated when the device exits Shutdown mode: all registers are reset except those in the backup domain, and a reset signal is generated on the pad.
The 20-byte backup registers are retained in Shutdown mode.
The wakeup sources are the 5 wakeup pins and the RTC events including tampers.

When exiting Shutdown mode, the wakeup clock is HSI at 16 MHz.



In Shutdown mode, the main regulator and the low-power regulator are powered down.
The RTC, clocked by the external low-speed oscillator, can remain active.
The brown-out reset is deactivated. Only the external low-speed clock can be enabled.
The wakeup events are the RTC and tamper events, the reset and the 5 wakeup pins.
The Shutdown consumption without RTC is around 40 nA typical at 3 V. The wakeup time is typically 250 µs.

Low-power modes summary

Mode	Regulator	CPU	Flash	SRAM	Clocks	Peripherals	Wakeup time
Run	MR Range 1	**Yes**	**ON**(1)	**ON**	Any	All	N/A
	MR Range 2					All	
LPRun	LPR	**Yes**	**ON**(1)	**ON**	Any except PLL	All	
Sleep	MR Range 1	No	**ON**(1)	**ON**(2)	Any	All Any interrupt or event	11 cycles
	MR Range 2						
LPSleep	LPR	No	**ON**(1)	**ON**(2)	Any except PLL	All Any interrupt or event	11 cycles
Stop 0	MR	No	OFF	**ON**	LSE/LSI	Reset pin, all I/Os BOR, PVD, RTC, IWDG, COMP, DAC, USARTx, LPUART, I2C, LPTIMx, UCPD, CEC	2 µs RAM 5.5µs Flash memory
Stop 1	LPR						5 µs RAM 9 µs Flash memory
Standby	LPR	DOWN	OFF	**SRAM ON**	LSE/LSI	Reset pin, 5 WKUPx pins BOR, RTC, IWDG	14 µs
	OFF			DOWN			
Shutdown	OFF	DOWN	OFF	DOWN	LSE	Reset pin, 5 WKUPx pins RTC	258 µs

1. Can be put in power-down and clock can be gated off
2. SRAM can be gated off

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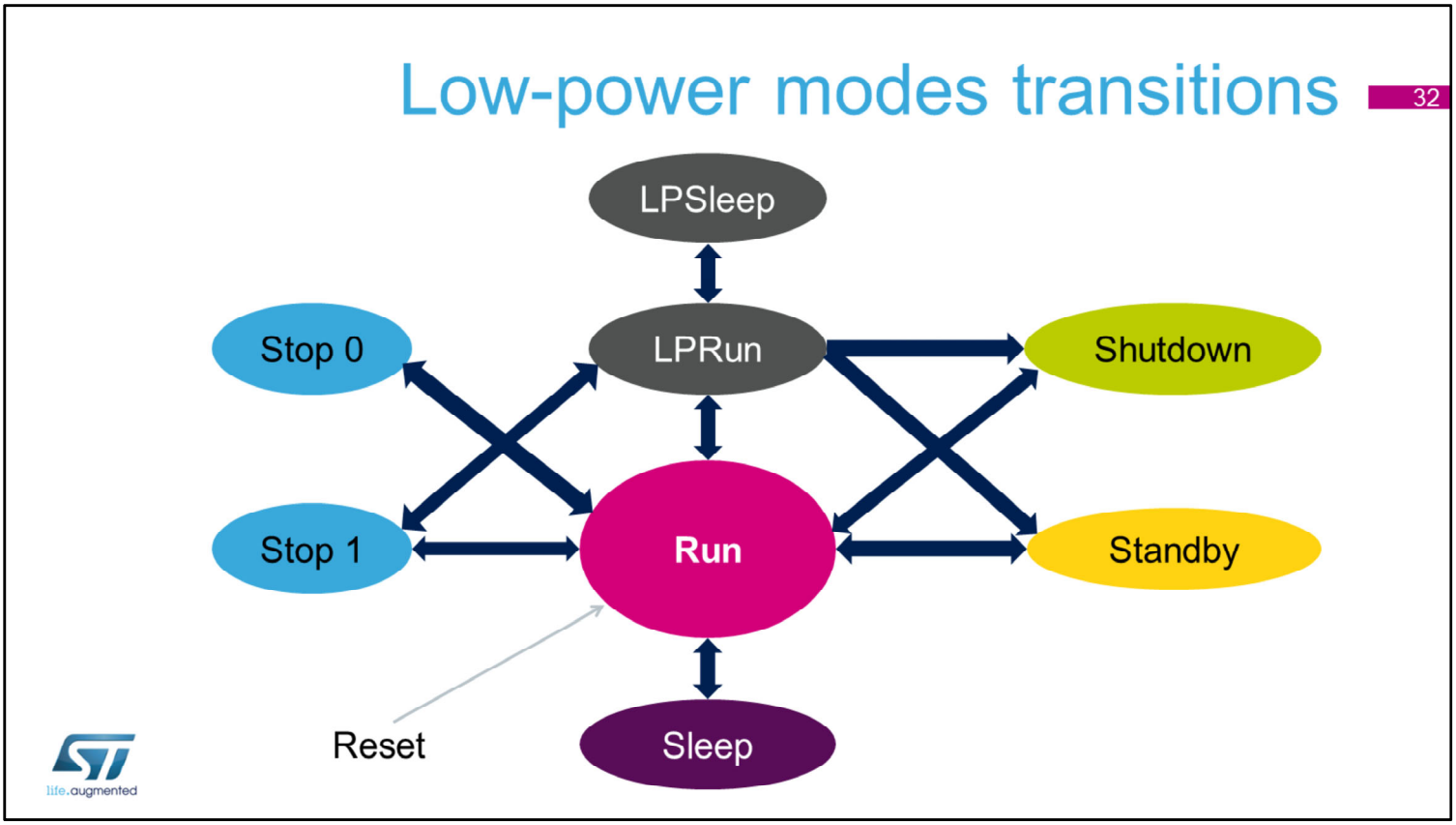
Here you can see the summary of all the STM32G0 power modes.
The minimum output of PLL is 3.09MHz, thus it cannot be used in LPRUN mode where the maximum frequency is 2MHz.



From Run mode, it is possible to access all low-power modes except Low-power sleep mode. In order to enter Low-power sleep mode, it is required to move first to Low-power run mode and execute a Wait for Interrupt or Wait for Event instruction while the regulator is the low-power regulator.
On the other hand, when exiting Low-power sleep mode, the STM32G0 is in Low-power run mode.
When the device is in Low-power run mode, it is possible to transition to all low-power modes except Sleep and Stop 0 modes. Stop 0 mode can only be entered from Run mode.
If the device enters Stop 1 mode from Low-power run mode, it will exit in Low-power run mode.
If the device enters Standby or Shutdown, it will exit in Run mode.

VBAT backup domain

RTC still running and backup registers preserved in case of V_{DD} loss

- Backup domain contains:
  - RTC clocked by 32.768 kHz LSE oscillator, including **2 tamper pins**
  - **20 bytes backup registers**
  - Reset through the RCC_BDCR
- Automatic internal switch between V_{BAT} and V_{DD} when V_{DD} is powered down and powered on
- Internal connection to ADC for voltage monitoring ($V_{BAT}/3$)
- VBAT battery charging

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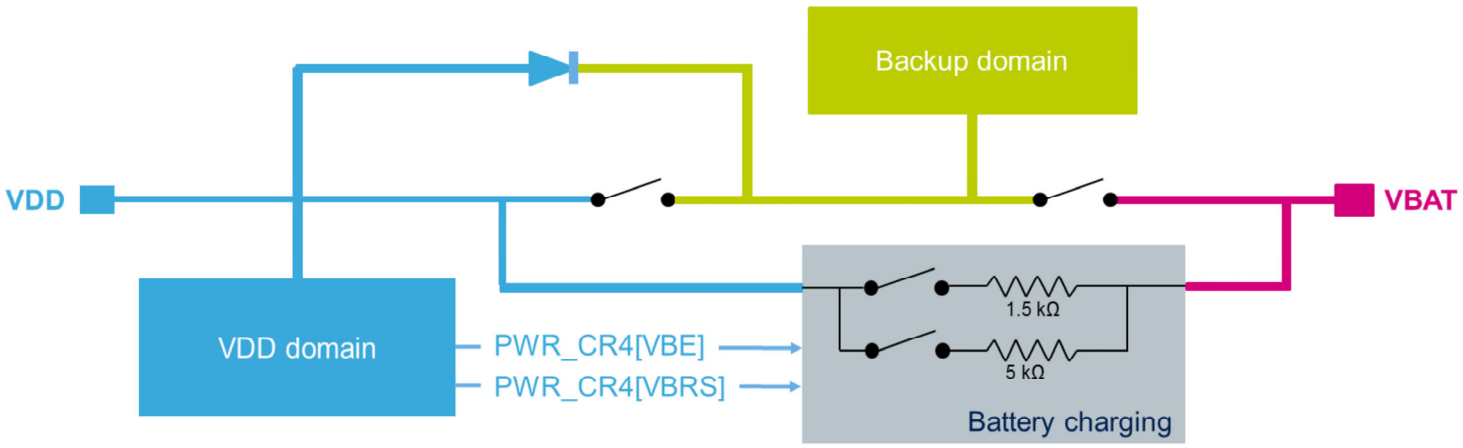
The backup domain allows to keep the RTC functional and to preserve the backup registers in case the VDD supply is down, thanks to a backup battery connected to the VBAT pin.
The backup domain contains the RTC clocked by the low-speed external oscillator at 32.768 kHz.
Two tamper pins are functional in VBAT mode, and will erase the 20-byte backup registers also included in the VBAT domain, in case of intrusion detection.
The backup domain also contains the RTC clock control logic.
In case VDD drops below a certain threshold, the backup domain power supply automatically switches to VBAT.
When VDD is back to normal, the backup domain power supply automatically switches back to VDD.
The VBAT voltage is internally connected to an ADC input channel in order to monitor the backup battery

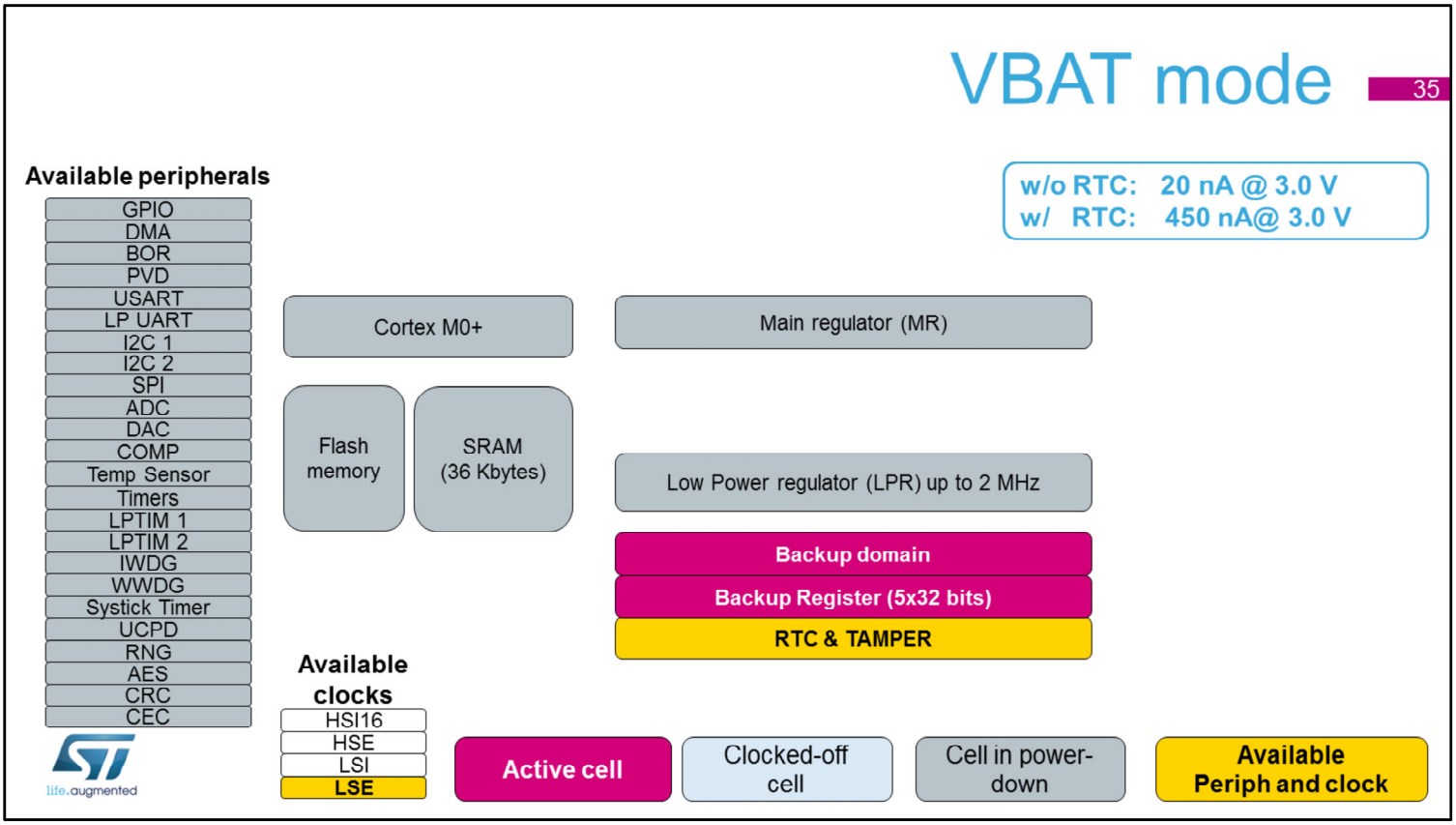
level.
When VDD is present, the battery connected to VBAT can be charged from the VDD supply.

VBAT backup domain

- VBAT battery charging: allows to charge a super-cap on VBAT through internal resistor when V_{DD} is present



The battery charging feature allows to charge a super-cap connected to VBAT pin through internal resistor when VDD supply is present.
The charging is enabled by software and is done either through a 5kΩ or 1.5kΩ resistor depending on software.
Battery charging is automatically disabled in VBAT mode.
PWR_CR4[VBE] enables battery charging.
PWR_CR4[VBRS] selects the resistance value.
During the startup phase, if VDD is established in less than tRSTTEMPO and VDD greater than VBAT + 0.6 V, a current may be injected into VBAT through an internal diode connected between VDD and the power switch (VBAT).
If the power supply/battery connected to the VBAT pin cannot support this current injection, it is strongly recommended to connect an external low-drop diode between this power supply and the VBAT pin



In VBAT mode, the main regulator and the low-power regulator are powered down.
The RTC and Tamper, clocked by the external low-speed oscillator, can remain active.
Only the external low-speed clock can be enabled.
The only powered block is the backup domain that includes RTC and Tampers, and the return to normal execution happens once VDD supply is provided.
The VBAT consumption with RTC is around 450 nA typical at 3 V.

Option bytes

- 3 option bits can be configured in Flash option bytes to prohibit a given low-power mode:
  - nRST_SHDWN: When cleared, a Reset is generated when entering Shutdown mode
  - nRST_STDBY: When cleared, a Reset is generated when entering Standby mode
  - nRST_STOP: When cleared, a Reset is generated when entering Stop modes

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Three bits are available in the Flash option bytes to prohibit a given low-power mode.
When cleared, a reset is generated instead of entering the related low-power modes.

Debug information

- Under Sleep mode, the DBG connection is not lost
- 2 bits in DBGMCU_CR register allows to debug in Stop, Standby and Shutdown modes:
  - DBG_STANDBY: When set, the digital part is not unpowered in Standby and Shutdown modes, and HCLK and FCLK remain ON, provided by internal RC
    - In addition, the MCU in under system reset during Standby/Shutdown
  - DBG_STOP: When set, HCLK and FCLK remain ON in Stop modes, provided by internal RC
- When those bits are set, the connection with debugger is kept during the low-power mode
  - After wakeup, debug is still possible

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The microcontroller integrates special means to allow the user to debug software in low-power modes.
Two bits are available in the Debug Control Register, in order to allow debugging in Stop, Standby and Shutdown modes.
When the related bit is set, the regulator is kept on in Standby and Shutdown modes, and the HCLK and FCLK clocks are provided by an internal RC oscillator.
This maintains the connection with the debugger during the low-power modes, and continues debugging after wakeup.
Remember to clear these bits when the microcontroller is not under debug, because the consumption is increased in low power modes.

Related peripherals

- Refer to the following list of peripherals training for more details of their dependencies with the power modes:
  - Reset and clock control (RCC)
  - Interrupts (NVIC, EXTI)
  - Digital-to-analog converter (DAC)
  - Comparator (COMP)
  - Low-power timer (LPTIM)
  - Independent watchdog (IWDG)
  - Real-time clock (RTC)
  - Inter-integrated circuit (I2C) interface
  - Universal synchronous asynchronous receiver transmitter (USART)
  - Low-power universal asynchronous receiver transmitter (LPUART)
  - USB PORT C Power Delivery (UCPD)
  - HDMI-CEC controller (HDMI-CEC)

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In addition to this training, you can refer to the Reset and Clock Control, Interrupts trainings as well as those for all the peripherals with wakeup from Stop capability.