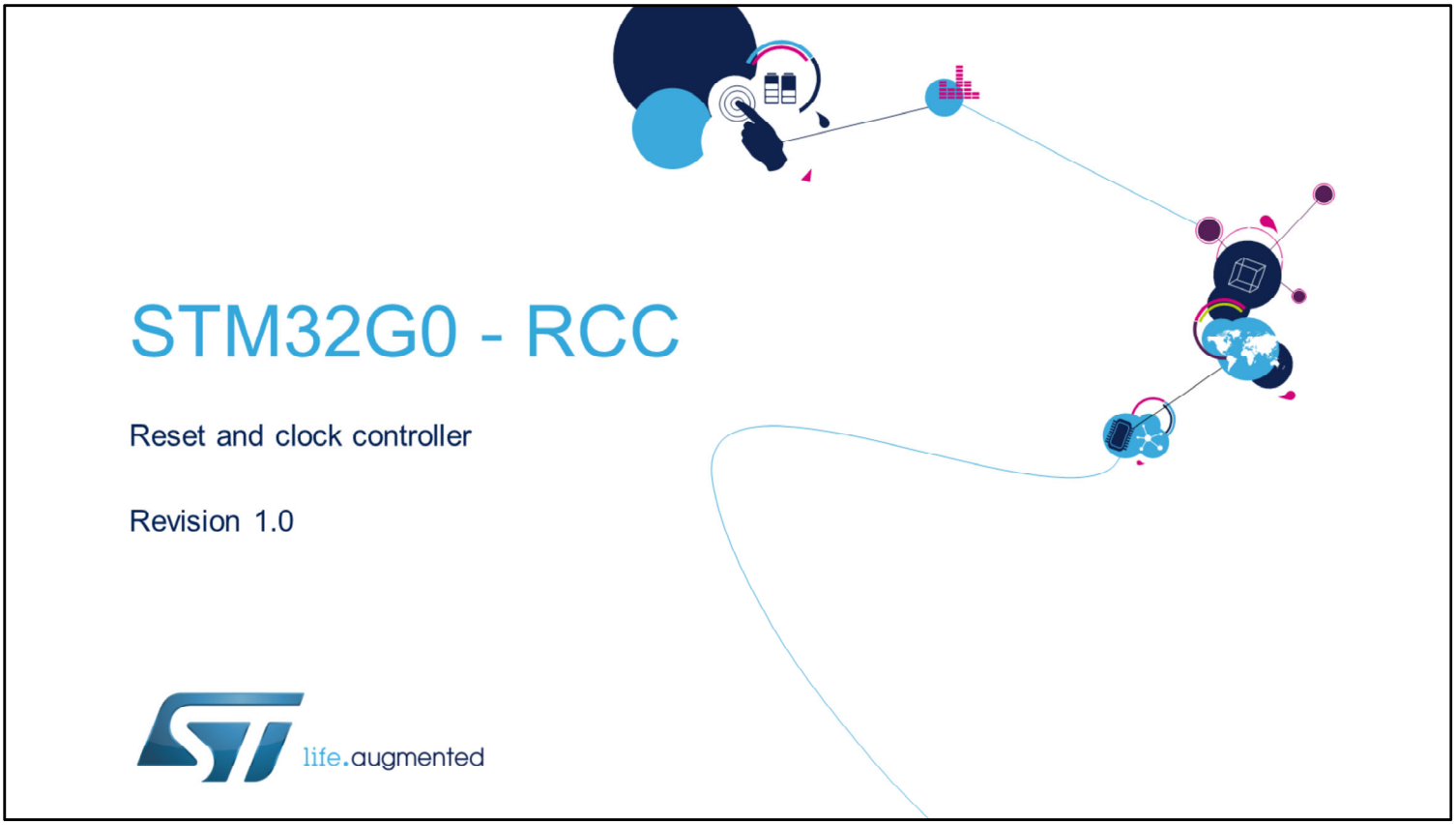

Hello, and welcome to this presentation of the STM32G0 reset and clock controller.

Main Differences with STM32F0

- The Reset and Clock Controller is similar to the one implemented in the F0 family with some enhancements

	STM32F0	STM32G0
NRST	Input & output	GPIO, Input, Input & output
Reset Holder	No	Yes
PLL	One output	Three outputs
CSS on LSE + LSCO *	No	Yes
HSI divider to SYSCLK	No	Yes
Timer 1 & 15 running at 2xSYSCLK	No	Yes

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* CSS on HSE was already available for both F0 and G0 products

The RCC unit implemented in the STM32G0 offers new features with regard to STM32F0 microcontrollers.
The NRST pin has 3 possible usages:

1. reset input used by an external logic to signal a reset condition to the STM32G0
2. reset input & output (legacy mode), any valid reset signal on the pin is propagated to device internal logic and all internal reset sources are externally driven through a pulse generator to this pin
3. GPIO, in this mode, the pin can be used as standard GPIO, reset is only possible from the device's internal reset sources.

The reset holder option can be used, if enabled in the option bytes, to ensure that the pin is pulled low until its voltage meets the VIL threshold.
The PLL has 3 post-dividers providing 3 independent outputs: PLLPCLK, PLLQCLK and PLLRCLK.

The Clock Security System (CSS) also monitors the LSE and detect failures. If the low-speed external 32.768 kHz oscillator (LSE) is used as system clock, and a failure of LSE clock is detected, the system clock switches automatically to the low-speed internal 32 kHz RC oscillator (LSI).
HSISYS is the high-speed internal 16 MHz RC oscillator (HSI16) divided by a programmable ratio in range 1-128.
PLLQCLK is selectable for high-speed TIM1 and TIM15 timers, its frequency must be set so as not to exceed 128 MHz. This is twice the maximum frequency of the Cortex®-M0+.

Overview

- The STM32G0 reset and clock controller manages system and peripheral clocks
  - 2 internal oscillators
  - 2 external oscillators (crystal or resonator)
  - 1 PLL
  - Many peripherals have independent clocks
- The RCC manages the various system and peripheral resets.

Application benefits

- High flexibility in choice of clock sources to meet consumption and accuracy requirements.
- Many independent peripheral clocks allow for adjusting power consumption without impacting communication baud rates, and to keep some peripherals active in low-power modes.
- Safe and flexible reset management

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The STM32G0 reset and clock controller manages system and peripheral clocks. STM32G0 devices embed two internal oscillators, 2 oscillators for an external crystal or resonator, and one phase-locked loop (PLL). Many peripherals have their own clock, independent of the system clock.
The RCC also manages the various resets present in the device.
The STM32G0 RCC provides high flexibility in the choice of clock sources, which allows the system designer to meet both power consumption and accuracy requirements. The numerous independent peripheral clocks allow a designer to adjust the system power consumption without impacting the communication baud rates, and also keep some peripherals active in low-power modes. Finally, the RCC provides safe and flexible reset management.

Reset key features

Safe and flexible reset management without external components

- Manages three types of reset:
  - System reset
  - Power reset
  - Backup domain reset
- Peripherals have individual reset control bits

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Safe and flexible reset management without any need for external components reduces application costs.
The RCC manages three types of resets: the system reset, the power reset and the backup domain reset.
The peripherals have individual reset control bits.

Reset sources

5

- System reset
  - Resets all registers except certain RCC registers, and the RTC domain
  - Reset sources
    - Low level on the NRST pin (external reset)
    - WWDG event
    - IWDG event
    - A software reset request
    - Low-power-mode security reset
    - Option byte loader reset
    - Brown-out or Power-on reset
  - The Reset Source flag is in the RCC_CSR register

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The first type of reset is the System reset, which resets all the registers except certain registers for the Reset and Clock Controller. It also does not reset the RTC domain.

The System reset sources are:

- The external reset (generated by a low level on the NRST pin),
- A window watchdog event,
- An independent watchdog event,
- A software reset request,
- A low-power-mode security reset (which is generated when Stop, Standby or Shutdown mode is entered but is prohibited by the option byte configuration),
- An option byte loader reset,
- And a Brown-out or Power-on reset.

The reset source flag can be found in the RCC Control and Status register.

Reset sources

- NRST Pin new design => PF2-NRST
  - The configuration of the Reset circuitry is done through the option bytes NRST_MODE[1:0] and IRHEN.

Mode	Configuration		Behavior
	NRST_MODE	IRHEN	
Input/Output (Legacy)	11	0	20 µs output pulse generated on NRST pin in case of Internal Reset
		1	Output pulse maintained until NRST voltage reaches V_{IL} threshold (~0.3 VDD)
Input only	01	x	Internal resets are not propagated outside of the part (PU always ON)
GPIO	10	x	PF2 only, No Reset Pin

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Two fields in the option bytes are used to configure the NRST pin:

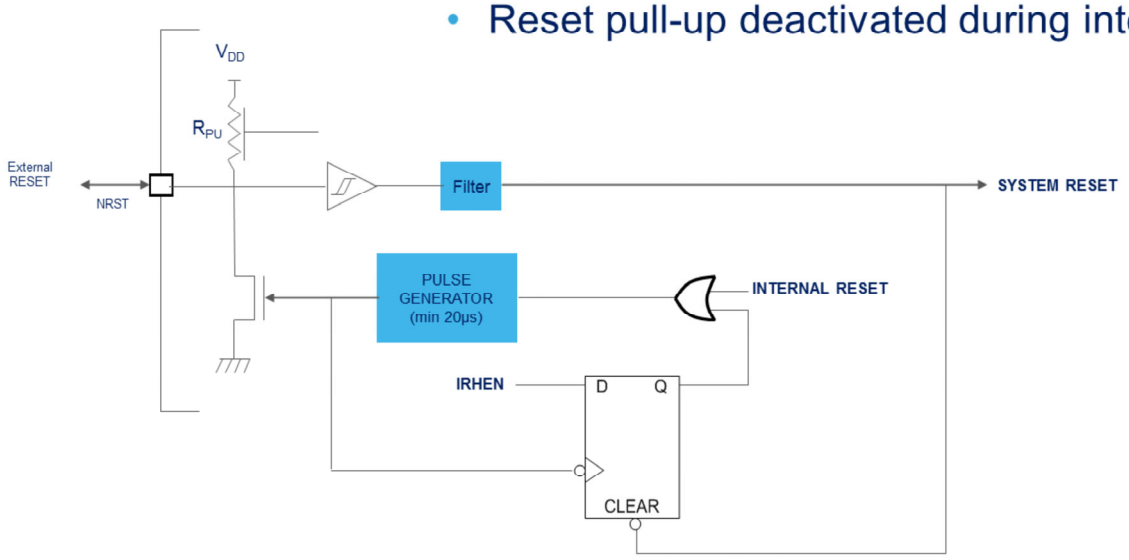
- NRST_MODE selects the operation mode of the NRST pin: input / output reset, input only reset or GPIO.
- IRHEN stands for Internal Reset Holder Enable. When this mode is enabled, the NRST pin is driven low until its voltage level goes under the voltage input low threshold.

Reset sources

No external components are needed due to internal filter and power monitoring

System reset sources can reset external components

- Reset pull-up deactivated during internal reset



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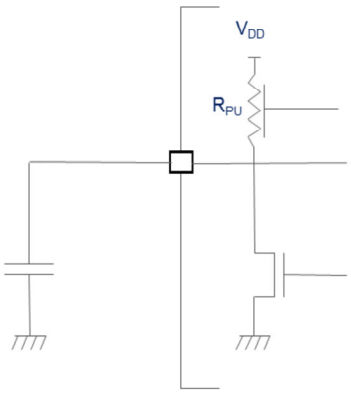
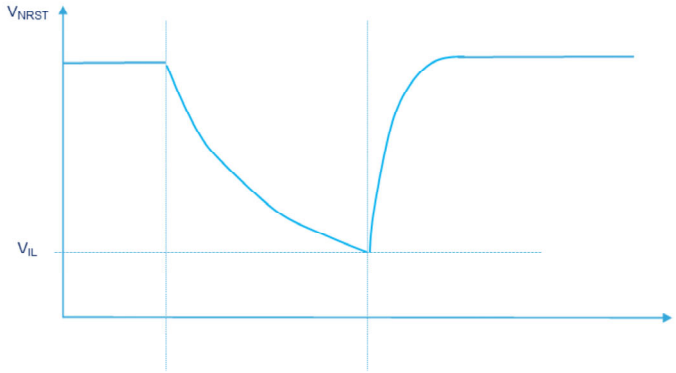
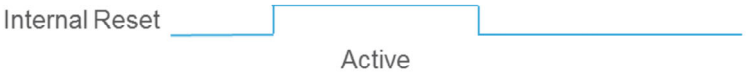
Here is the simplified block diagram of the system reset. All internal reset sources provide a reset signal on the NRST pin, which can be used to reset other components of the application board. In addition, no external reset circuitry is needed due to the internal glitch filter and the safe power monitoring feature which guarantees the reset of the application when VDD is below the selected threshold. The internal pull-up on the NRST pin, which maintains a high level when no reset signal drives it low, is deactivated when an internal reset is driven in order to reduce power consumption under reset. Additionally, except the debug pins and some test pins, all I/O pins are placed in analog mode during and after reset to eliminate power consumption through the Schmitt trigger when the I/Os are floating under reset and before software initialization.

Reset sources

No external components are needed. If there is strong capacitance used for external devices on the line, the Reset Holder can be used.







The purpose of the reset holder is to maintain NRST driven LOW until the voltage level of this signal goes below VIL. This is useful when the NRST line has an important capacitive load.

Reset sources

- Power reset
  - Sources
    - Brown-out reset (BOR) or Power-on reset (POR) => resets all registers except those in the RTC domain
    - Exit from Standby => resets all registers in VCORE domain

      Registers outside the VCORE domain (RTC, WKUP, IWDG, and Standby/Shutdown mode control) are not impacted.
    - Exit from Shutdown generates a BOR reset.
- RTC domain reset
  - Resets RTC registers, Backup registers, and the RCC BDCR register
  - Sources
    - BDRST bit in RCC BDCR register
    - VDD or VBAT power on, if both supplies have previously been powered off

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The second type of reset is the Power reset. The Brown-out reset (BOR) resets all registers except those in the RTC domain powered by VBAT which contains the RTC, the backup registers and the external low-speed oscillator. When exiting Standby mode, all registers powered by the regulator are reset. When exiting Shutdown mode, a Brown-out reset is generated.
The third type of reset is the RTC domain reset, which resets the RTC registers, the Backup registers, and the RTC Domain Control Register. This reset occurs when the BDRST bit is set in the RTC Domain control register. It also occurs when VDD and VBAT are powered on if both supplies have previously been powered off.

Clock key features

Choice of clock sources for low-power, accuracy, and performance

- Two internal clock sources
  - High-speed internal 16 MHz RC oscillator (HSI16)
  - Low-speed internal 32 kHz RC oscillator (LSI)
- Two external oscillators
  - High-speed external 4 to 48 MHz oscillator (HSE) with clock security system
  - Low-speed external 32.768 kHz oscillator (LSE) with clock security system
- One PLL with three independent outputs

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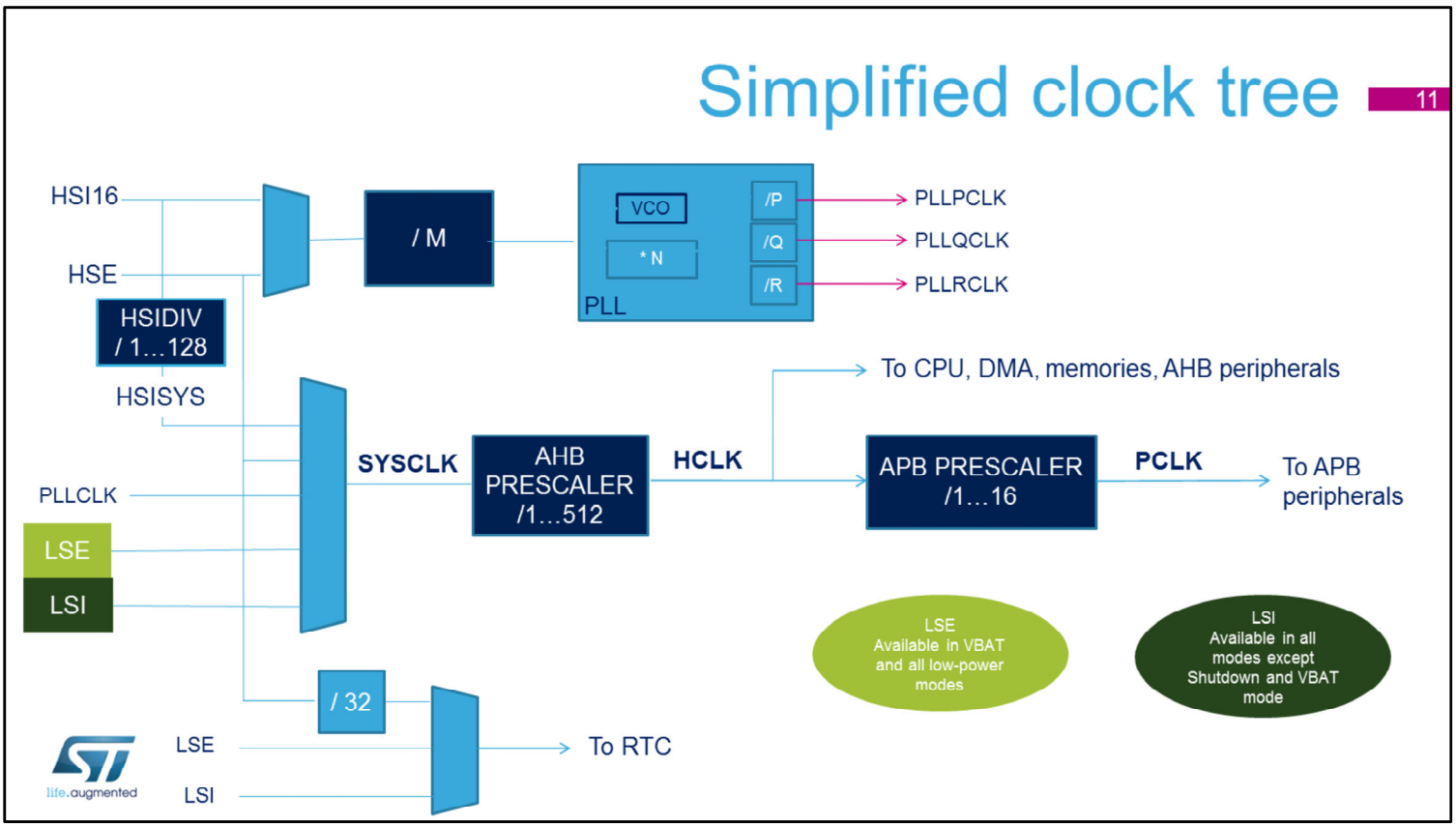
The RCC offers a large choice of clock sources, which can be selected depending on low-power, accuracy, and performance requirements.
STM32G0 devices embed two internal clock sources: a high-speed internal 16 MHz RC oscillator (HSI16) and a low-speed internal 32 kHz RC oscillator (LSI).
STM32G0 devices embed two oscillators for use with an external crystal or resonator: a high-speed external 4 to 48 MHz oscillator (HSE) with a clock security system and a low-speed external 32.768 kHz oscillator (LSE) also with a clock security system.
STM32G0 devices embed a phase-locked loop with three independent outputs for clocking different peripherals at different frequencies.



The system clock can be derived from the high-speed internal 16 MHz RC oscillator (HSI16), the high-speed external 4 to 48 MHz oscillator (HSE), the low-speed internal oscillator (LSI) or the low-speed external oscillator (LSE). The AHB clock, called HCLK, is derived by dividing the system clock by a programmable prescaler. The APB clock, called PCLK is generated by dividing the AHB clock by a programmable prescaler.

The RTC clock is generated by the low-speed external 32.768 kHz oscillator (LSE), the low-speed internal 32 kHz RC oscillator (LSI), or the HSE divided by 32.

The LSE can remain enabled in all low-power modes and in VBAT mode, because the LSE belongs to the RTC power domain.
The LSI can remain enabled in all modes except

Shutdown and VBAT modes.

High-Speed Internal (HSI16) clock

12

1% accuracy and fast wakeup time

- 16 MHz, factory- and user-trimmed (HSI16)
- HSISYS clock is:
  - The wakeup clock from Stop 0 and Stop 1 modes
  - The backup clock for Clock Security System (CSS)
- I2C, USART, LPUART, CEC and UCPD can enable the HSI16 during Stop mode to detect their wakeup sequence.
  - HSI16 remains off during Stop mode except for the peripheral wakeup sequence detection.

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Stop modes (Stop 0 and Stop 1) stop all the clocks in the VCORE domain and disable the PLL as well as the HSI16 and HSE oscillators.
The high-speed internal oscillator (HSI16) is a 16 MHz RC oscillator which provides 1% accuracy and fast wakeup times. The HSI16 is trimmed during production testing, and can also be user-trimmed.
The HSISYS clock (which is the HSI16 clock divided by HSIDIV) is used as the clock at wakeup from Stop 0 or Stop 1 modes.
HSI16 **is** ~~**can be**~~ used as a backup clock source (auxiliary clock) if the HSE crystal oscillator fails, which is detected by the Clock Security System.
The USART1, USART2, LPUART1, CEC, UCPD and I2C1 peripherals can enable the HSI16 oscillator even when the MCU is in Stop mode (if HSI16 is selected as clock source for that peripheral).

HSI16 characteristics

	HSI16 (16 MHz)
Accuracy (typ.)	Over [0-85 °C]: ± 1 %
Consumption (typ.)	180 µA
Startup time (typ.)	1 µs

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This table provides the characteristics of the HSI16 clock.
The HSI16 accuracy can be improved by implementing a trimming procedure, by measuring its frequency with the TIM14, TIM16 or TIM17 by clocking the timer by HSI clock and providing precise clock reference like HSE/32, RTCCLK or LSE on their channel 1 input capture.
The HSI clock has a typical 1 microsecond startup time while the HSE clock has a typical 2 millisecond startup time.

High-Speed External (HSE) clock

Safe crystal system clock

- HSE 4 to 48MHz
  - External source (Bypass mode) up to 48 MHz
  - External crystal/ceramic resonator (4 to 48 MHz)
- Clock Security System (CSS)
  - Automatic detection of HSE failure with switching to HSISYS
    - Non-maskable interrupt generation
    - Break input to TIM1/TIM15/TIM16/TIM17 => critical applications such as motor control can be put in a safe state.

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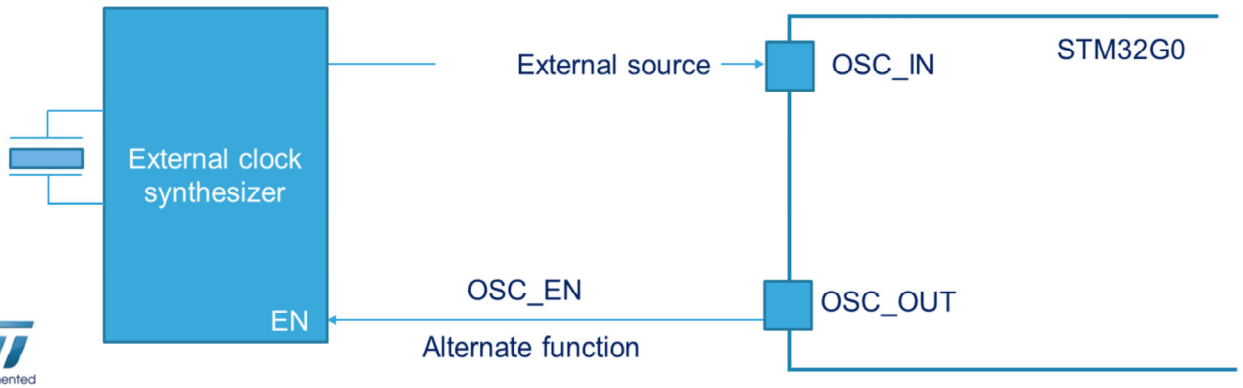
The high-speed external oscillator provides a safe crystal system clock.
The HSE supports a 4 to 48 MHz external crystal or ceramic resonator, and also an external source in Bypass mode.
A clock security system allows an automatic detection of HSE failure. In this case a Non-Maskable Interrupt is generated, and a break input can be sent to timers in order to put critical applications such as motor control in a safe state. When an HSE failure is detected, the HSE oscillator is automatically disabled.
If HSE is selected directly or indirectly (PLLRCLK selected for SYSCLK and HSE selected as PLL input) as system clock, and a failure of HSE clock is detected, the system clock switches automatically to HSISYS, so the application software does not stop in case of crystal oscillator failure.

High-Speed External (HSE) clock

- New Alternate Function is available on the HSE system to be used with oscillators.
  - When the external clock is used in Bypass mode, a new OSC_EN function is available for the application to be used as an ENABLE signal for the external clock. It is used to switch off the external clock when entering low-power modes.



In External source mode, also called HSE bypass mode, an external clock source must be provided. It can have a frequency of up to 48 MHz.
The external clock signal (square, sinus or triangle) with 40-60 % duty cycle depending on the frequency must drive the OSC_IN pin.
The OSC_OUT pin can be used as GPIO or it can be configured as an OSC_EN alternate function to provide a signal enabling the stop of the external clock synthesizer when the device enters low-power modes.

Low-Speed Internal (LSI) clock

Ultra-low-power internal 32 kHz oscillator
Available in all modes except Shutdown and VBAT

	LSI 32 kHz
Accuracy (typ.)	+6.3 / -7.8 %
Consumption (typ.)	110 nA

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STM32G0 devices embed an ultra-low-power 32 kHz RC oscillator, which is available in all modes except Shutdown and VBAT.
The LSI can be used to clock the RTC, the low-power timers, and the independent watchdog. The LSI consumption is typically 110 nA.

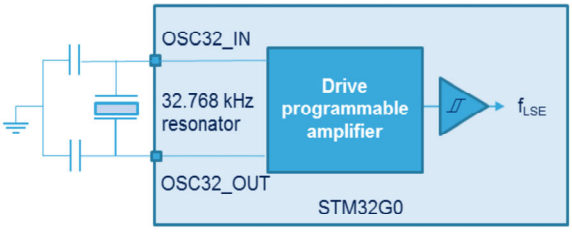
Low-Speed External (LSE) clock

32.768 kHz configurable for low-power or high-drive

Available in all power modes and in VBAT mode

- The LSE can be used with external quartz or resonator, or with external clock source in bypass mode
- Clock Security System (CSS) on LSE: Available in all modes except Shutdown and VBAT
  - Operates under reset
- The LSE can be used for RTC, CEC, USARTs, LPUART, and LPTIMs
- Oscillator driving control capability:

Mode	Maximum critical crystal gm (µA/V)	Consumption (nA)
Ultra-low power	0.5	250
Medium-low driving	0.75	315
Medium-high driving	1.7	500
High driving	2.7	630



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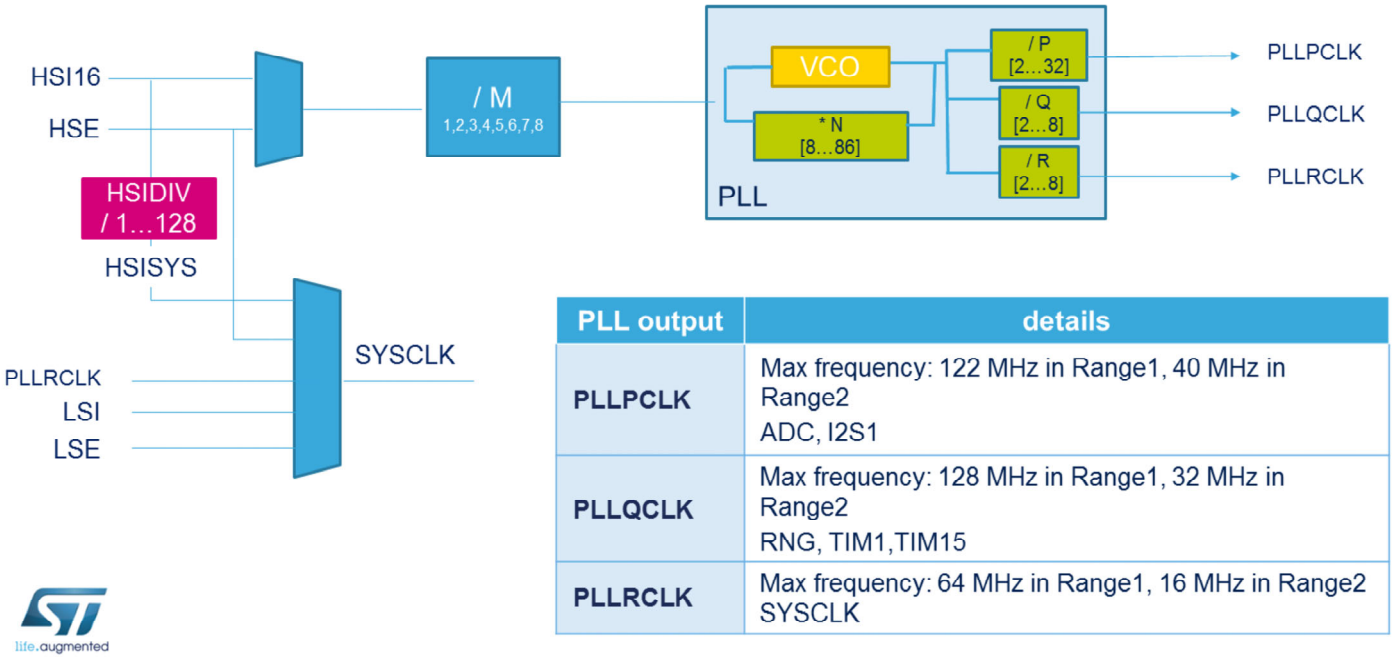
The 32.768 kHz low-speed external oscillator can be used with external quartz or resonator, or with an external clock source in Bypass mode. The oscillator driving capability is programmable. Four modes are available, from an ultra-low power mode with a consumption of only 250 nanoamperes, to a high-driving mode.

A clock security system monitors for failure of the LSE oscillator. If LSE is used as system clock, and a failure of LSE clock is detected, the system clock switches automatically to LSI. The CSS is functional in all modes except Shutdown and VBAT. It is also functional under reset.

The LSE can be used to clock the RTC, the CEC, the USARTs or low-power UART peripherals, and the low-power timers.

PLL clock



PLL output	details
PLLPCLK	Max frequency: 122 MHz in Range1, 40 MHz in Range2 ADC, I2S1
PLLQCLK	Max frequency: 128 MHz in Range1, 32 MHz in Range2 RNG, TIM1,TIM15
PLLRCLK	Max frequency: 64 MHz in Range1, 16 MHz in Range2 SYSCLK

STM32G0 devices embed a phase-locked loop, each with 3 independent outputs. The input clock of the PLL can be selected between HSI16 and HSE.
PLLQCLK can be used to clock the RNG and timers TIM1 and TIM15.
PLLPCLK can be used to clock I2S1 and ADC.
PLLRCLK can be selected as the system clock called SYSCLK, which is the root clock for AHB and APB clock domains.
Note that PLLQCLK and PLLPCK maximum frequencies are larger than the maximum SYSCLK frequency.
Range 1 and Range 2 are two different power ranges that can be programmed in the main regulator in order to optimize the consumption depending on the system maximum operating frequency.

System clock

- Selected between HSI16, HSE, PLL, LSI, and LSE
- System clock, AHB and APB maximum frequency: 56 MHz

Voltage range	SYSCLK	HSI16	HSE	PLL
Range 1	64 MHz max.	16 MHz	48 MHz	VCO max = 344 MHz
Range 2	16 MHz max.	16 MHz	16 MHz	VCO max = 128 MHz
Low-power run/sleep	2 MHz max.	Allowed with divider	Not allowed	Not allowed

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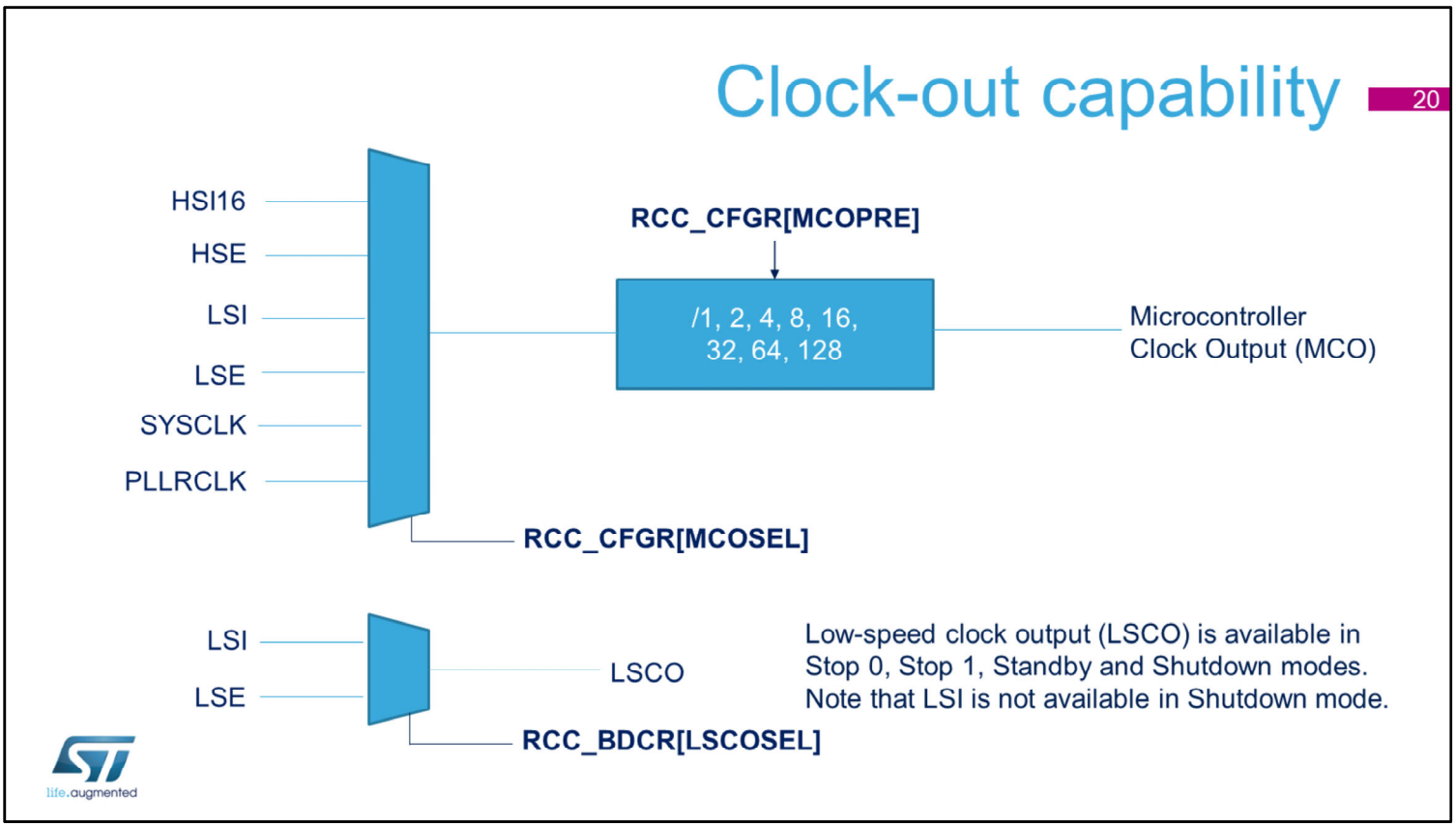
The system clock is selected between the HSI16, HSE, LSI, LSE and PLL output.
The maximum system clock frequency is 64Hz. The APB1 and APB2 bus frequencies are also up to 64 MHz.
The maximum clock source frequency depends on the voltage scaling and power mode. The system clock is limited to 64 MHz in Range 1, 16 MHz in Range 2 and 2 MHz in Low-power run/Low-power sleep modes.



The various clocks can be output on an I/O. The Microcontroller Clock Output feature allows you to output on a pin one of these six clocks, HSI16, HSE, LSI, LSE, SYSCLK, and PLLCLK.

The low-speed clock output (LSCO) feature allows the output of the LSI or LSE clock on a pin. The low-speed clock output is available in Stop 0, Stop 1, Standby and Shutdown modes. This is enabled by setting the LSCOEN bit in the RCC_BDCR register.

Note that LSI is not available in Shutdown mode.

Clock gating

Dynamic consumption optimization in (LP)Run and (LP)Sleep modes

- Peripheral clock enable registers
  - Peripheral clocks disabled by default (except Flash memory)
  - Registers read and write access not supported when clock is disabled.
  - Caution: SRAM do not have enable bit (always enabled in Run/Low-power Run modes)
- Peripheral clock enable registers in Sleep and Stop modes
  - Enables or disables the peripheral clocks in Sleep, Low-power Sleep, Stop 0/1 modes
    - No effect if corresponding peripheral clock enable is cleared
    - Controls both bus and kernel clocks
    - Affects Sleep and Stop modes (for peripheral with independent clock active in Stop mode)
  - Caution: For each peripheral, the related clock is enabled by default in Sleep/Low-power Sleep modes

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The dynamic power consumption can be optimized by using peripheral clock gating.
Each peripheral clock can be gated ON or OFF in Run and Low-power run modes.
By default, the peripheral's clock is disabled, except the Flash memory clock which is enabled by default. When a peripheral's clock is disabled, the peripheral's registers cannot be read or written.
Other registers allow for configuring the peripheral's clock during the Stop, Sleep and Low-power sleep modes. This also affects Stop 0 and Stop 1 modes for peripherals with an independent clock active in Stop modes. These control bits have no effect if the corresponding peripheral clock enable is cleared. By default no active peripheral clock is gated in Stop, Sleep and Low-power Sleep modes. When a peripheral is not needed, its clock enable bit should be cleared to reduce

the power consumption.

Interrupts

Interrupt event	Description
LSE clock security system	Set when a failure is detected in the LSE oscillator
HSE clock security system	Set when a failure is detected in the HSE oscillator
PLL ready interrupt flag	Clock ready caused by PLL lock
HSE ready	HSE oscillator clock ready
HSI16 ready	HSI16 oscillator clock ready
LSE ready	LSE oscillator clock ready
LSI ready	LSI oscillator clock ready

This slide lists the RCC interrupts. The LSE and HSE clock security systems, the PLL ready, and all five oscillator ready signals can generate an interrupt.

Related peripherals

- Refer to these trainings linked to this peripheral
  - STM32G0 Power control (PWR)
  - STM32G0 Interrupts (NVIC-EXTI)

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In addition to this training, you may find the Power Control and Interrupt Controller trainings useful.

References

- For more details, please refer to following sources
  - AN2867 Oscillator design guide for STM8S, STM8A and STM32 microcontrollers
  - AN5126 "Calibrating STM32G0 Series internal RC oscillator

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For more details, please refer to application note AN2867, an oscillator design guide for STM8S, STM8A and STM32 microcontrollers and application note AN5126 which explains how to calibrate STM32G0 internal RC oscillators.