Hello, and welcome to this presentation of the STM32 LCD TFT display controller. It covers all of the features of the LTDC controller which is used to interface with TFT displays.

Overview

- LCD TFT display controller
  - Highly configurable
  - Standard parallel RGB interface

Application benefits

- Flexible programmable display parameters
- Integrated pixel format converter and blender
- Either on-chip memory or external memory can be used as frame buffer

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LCD-TFT stands for Liquid Crystal Display - Thin Film Transistor. The controller is highly configurable and interfaces with standard parallel R G B interfaces.
The benefits of the LCD TFT display controller include flexible programmable display parameters, integrated pixel format converter and blender.
The LCD TFT display controller (LTDC) frame buffer can be located either in on-chip memory or in an external memory depending on the panel resolution.

Key Features

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- 24-bit RGB parallel pixel output.
  - 8 bits per pixel (RGB888)
- AHB master interface with burst access of 16 words to any system memory
  - Dedicated 64-word FIFO per layer
- Programmable timings and polarity to interface with a wide range of display panels.
  - Timings: HSYNC width, VSYNC width, VBP, HBP, VFP, HFP
  - Polarity: HSYNC, VSYNC, not Data Enable, Pixel clock
- Supports only TFT (no STN)

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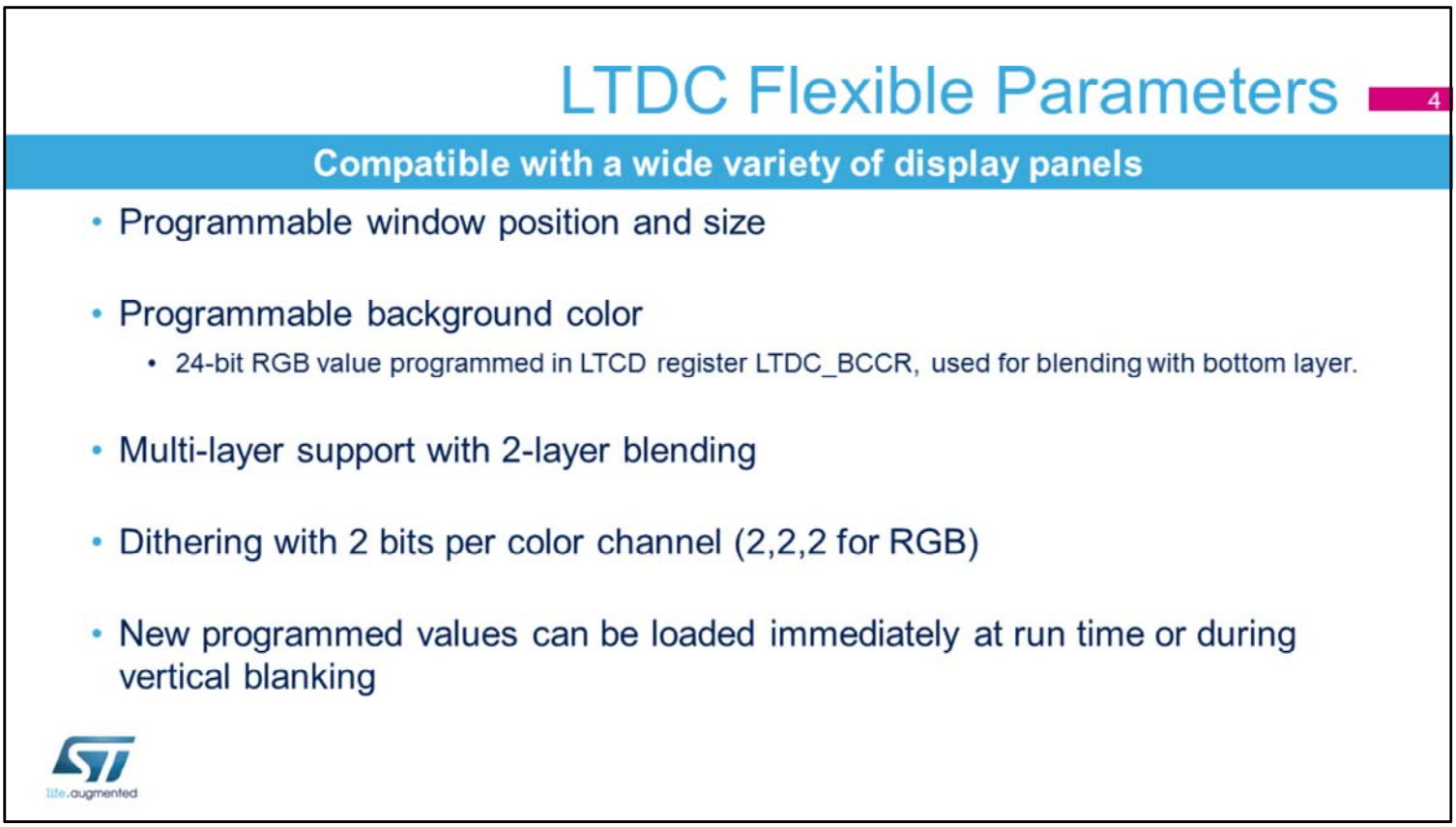
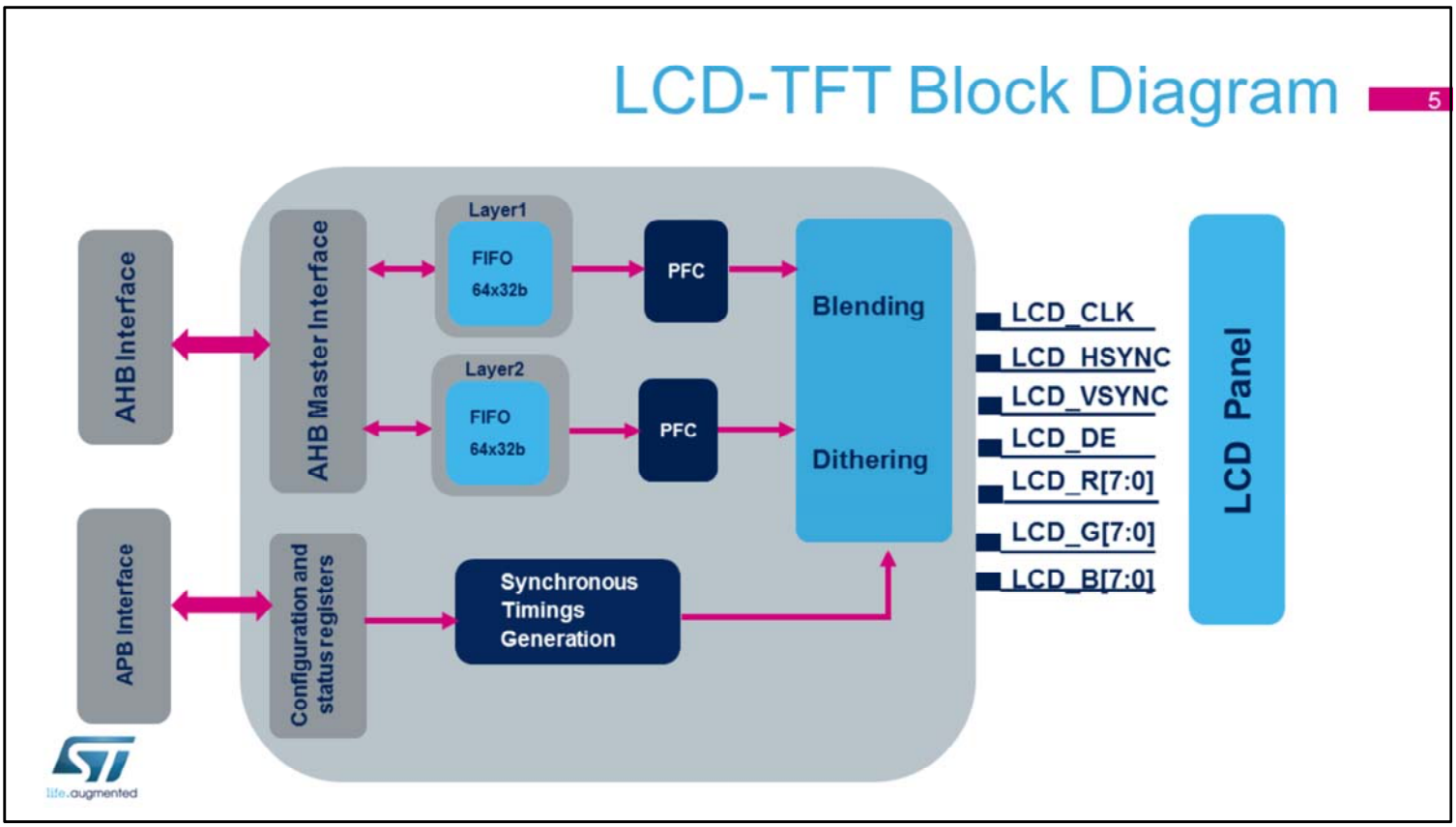
The LCD-TFT display controller provides a 24-bit parallel digital RGB (Red, Green, Blue) interface with additional signals for horizontal and vertical synchronization.
LTDC is a master on the AHB Bus Matrix and can access internal memories like internal Flash, internal SRAM or external memories via FSMC/OCTOSPI interfaces.
It also features a dedicated 64-word FIFO per layer.
It supports programmable timings and polarity parameters to interface with a wide range of display panels.

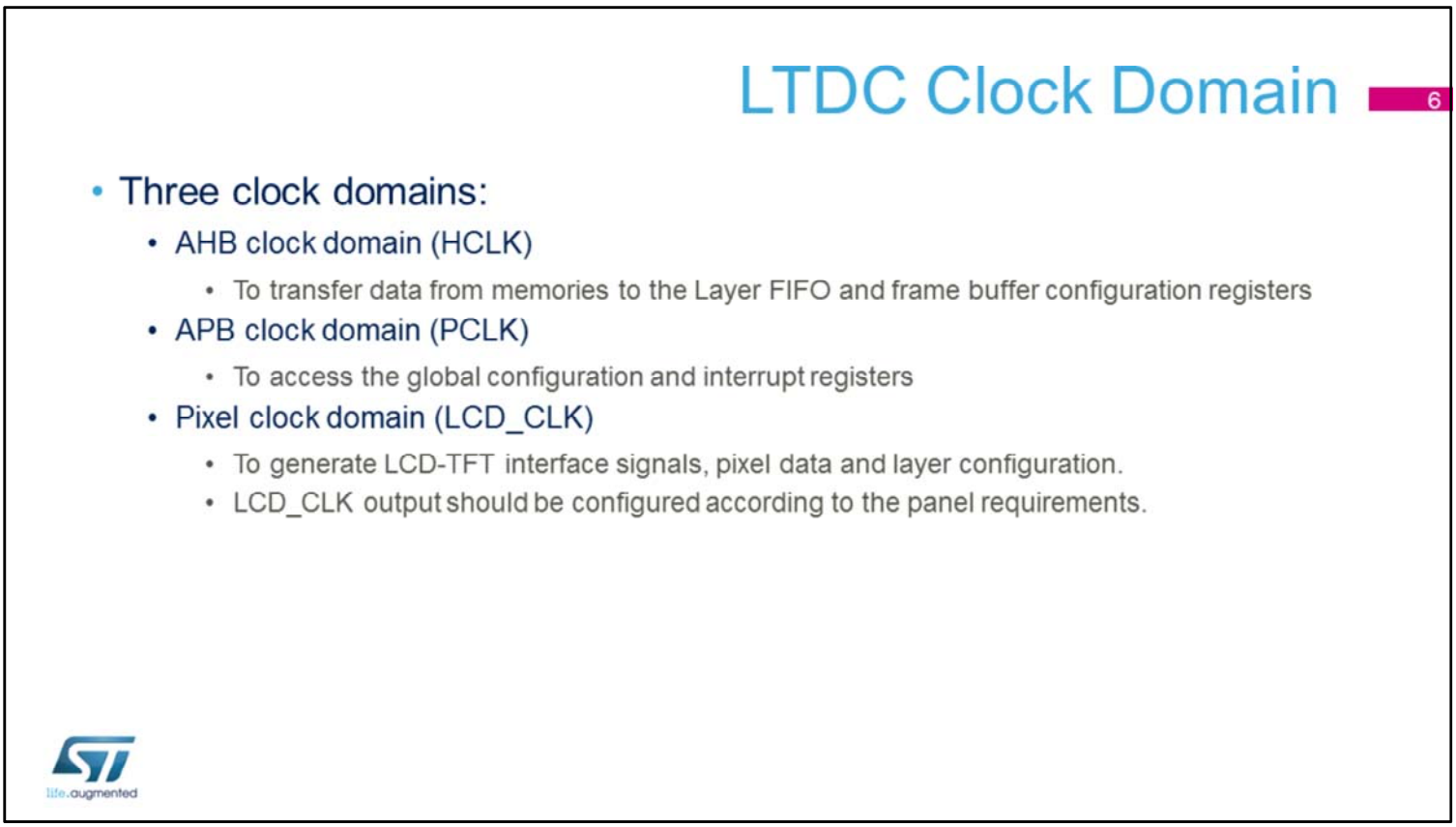


The LTDC offers flexible programmable parameters enabling the support of a wide variety of display panels.

- Programmable display size, examples: QVGA, WQVGA, VGA
- Programmable background color
- 24-bit RGB value programmed in the LCD controller register (LTDC_BCCR), used for blending with the bottom layer.
- Multi-layer Support with 2-layer blending
- Dithering , 2 bits per color channel (2,2,2 for RGB). The Dithering pseudo-random technique is used to add a small random value (threshold) to each pixel color channel (R, G or B) value, thus rounding up the most significant bits in some cases when displaying 24-bit data on an 18-bit display.
- New programmed values can be loaded immediately at run time or during vertical blanking.



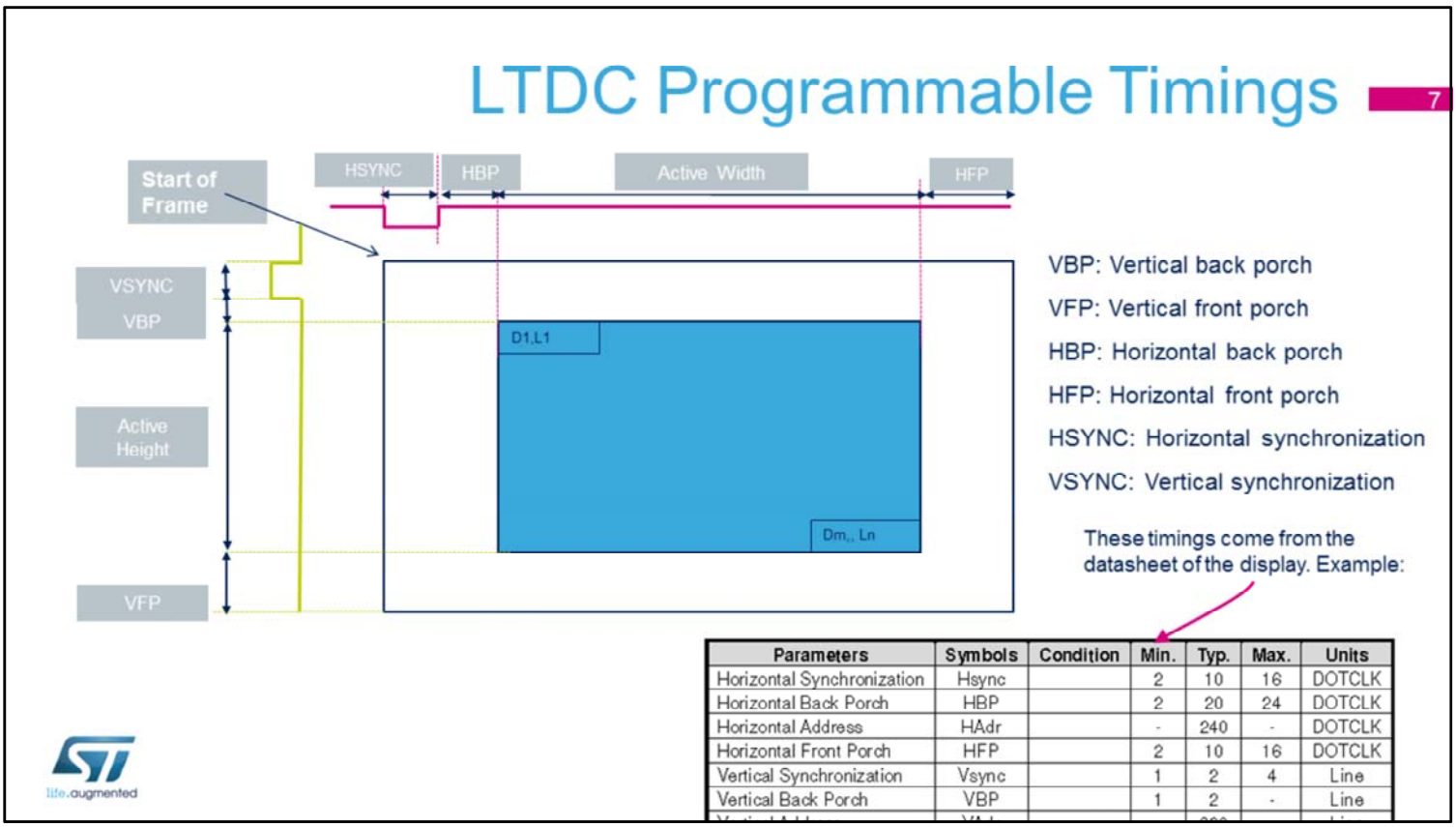
This is the LCD TFT controller block diagram



The LTDC features three clock domains:

- AHB clock domain (HCLK) to transfer data from memories to the Layer FIFO and frame buffer configuration registers
- APB clock domain (PCLK) to access the global configuration and interrupt registers
- The Pixel Clock domain (LCD_CLK) to generate LCD-TFT interface signals, pixel data and layer configuration.

The LCD_CLK output should be configured according to the panel requirements.



Parameters	Symbols	Condition	Min.	Typ.	Max.	Units
Horizontal Synchronization	Hsync		2	10	16	DOTCLK
Horizontal Back Porch	HBP		2	20	24	DOTCLK
Horizontal Address	HAdr		-	240	-	DOTCLK
Horizontal Front Porch	HFP		2	10	16	DOTCLK
Vertical Synchronization	Vsync		1	2	4	Line
Vertical Back Porch	VBP		1	2	-	Line

To interface with TFT panels, all timings are programmable through the LTDC controller. These timings come from the TFT panel datasheet and are:

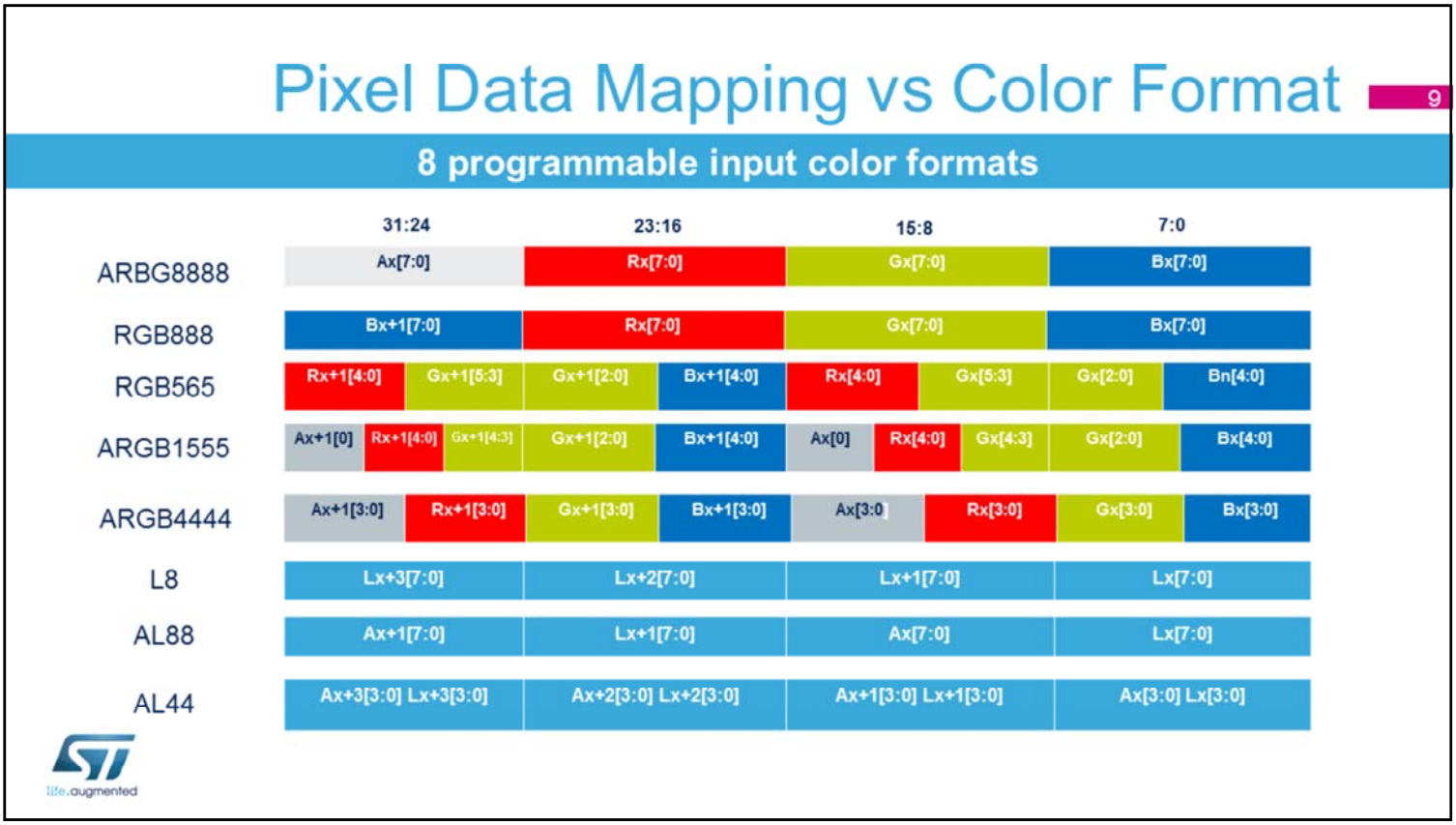
- VBP: Vertical Back porch
- VFP: Vertical Front porch
- HBP: Horizontal Back porch
- HFP: Horizontal Front porch
- HSYNC: Horizontal synchronization
- VSYNC: Vertical synchronization

LTDC Signals

Flexible I/O configuration

LCD-TFT signals	Description
LCD_CLK	Pixel clock output
LCD_HSYNC	Horizontal synchronization
LCD_VSYNC	Vertical synchronization
LCD_DE	No data enabled
LCD_R[7:0]	8-bit red data
LCD_G[7:0]	8-bit green data
LCD_B[7:0]	8-bit blue data

The LTDC output signals are summarized in this table.
The LCD-TFT controller pins must be configured by the user application. The unused pins can be used for other purposes.



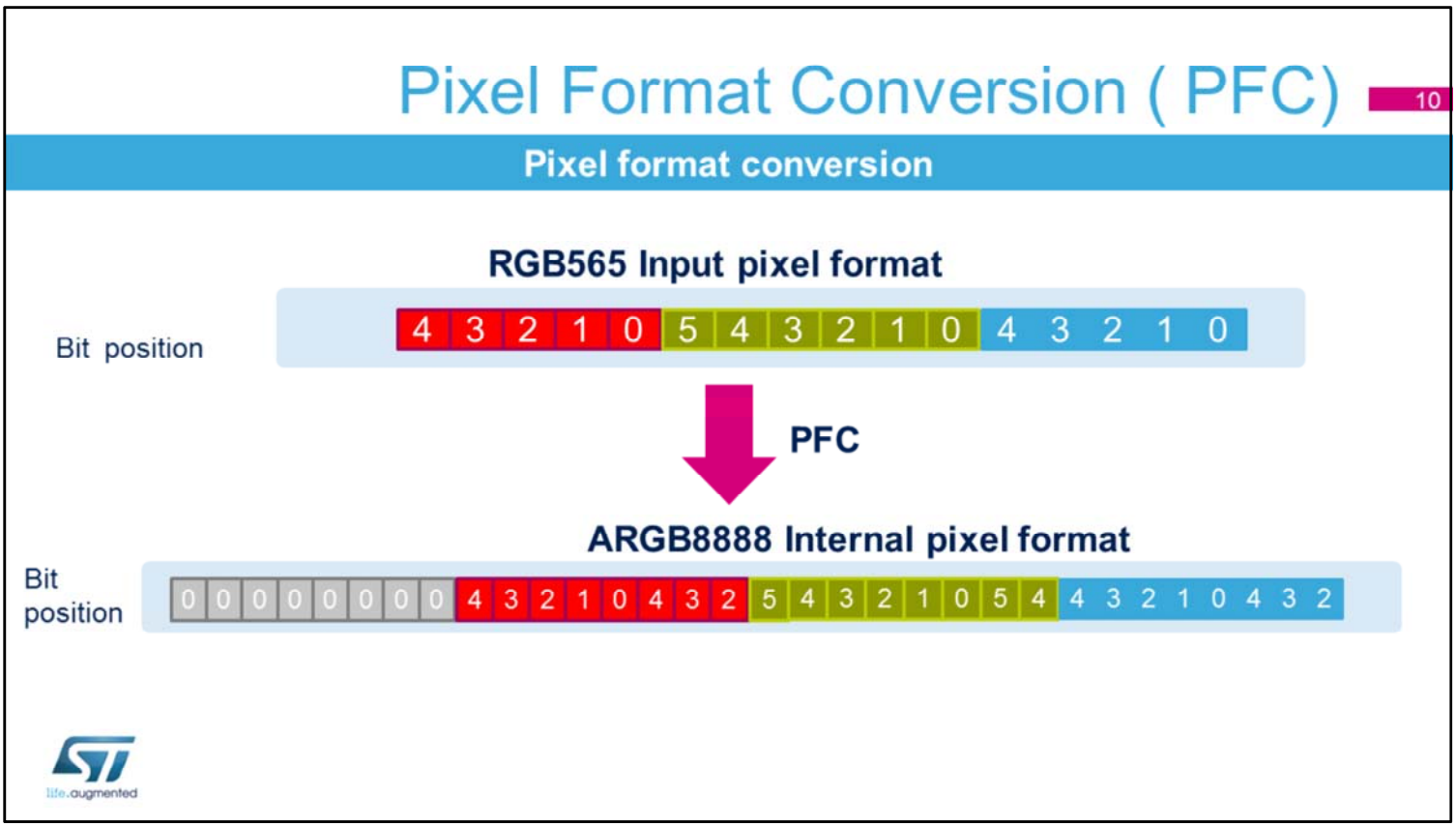
The programmable pixel format is used for the data stored in the frame buffer of a layer.
This table describes the pixel data mapping versus the selected input color format.
The LTDC can be configured with up to 8 programmable input color formats per layer:

Direct Color

- ARGB8888
- RGB888
- RGB565
- ARGB1555
- ARGB4444

Indirect Color

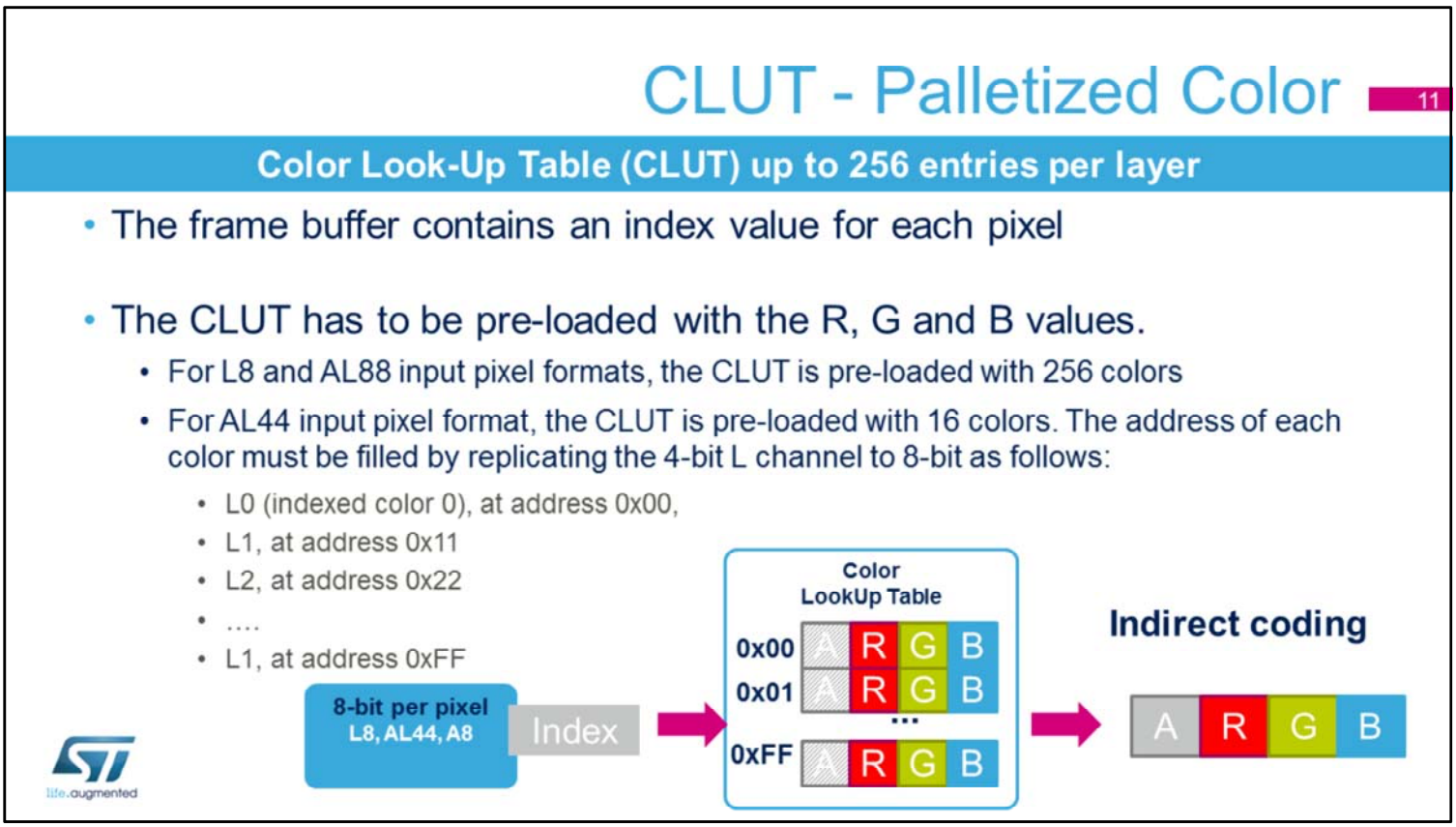
- L8 (8-bit Luminance or CLUT)
- AL44 (4-bit alpha + 4-bit luminance)
- AL88 (8-bit alpha + 8-bit luminance)



Pixel Format Conversion (PFC) is when the color format of a bitmap is converted into another one.

The pixel data is read from the frame buffer and then transformed to the internal ARGB 8888 format as follows: Components which have a width of less than 8 bits get expanded to 8 bits by bit replication. The 8 most significant bits are chosen.

Note that conversion from direct color to indirect color or from indirect color to direct color is easy to do, but converting a direct color to an indirect color format would mean regenerating a Color Look-Up Table or CLUT which is a very complex operation.



The Color Look-Up Table is only used in the case of indexed color for L8, AL44 and AL88 input pixel formats.

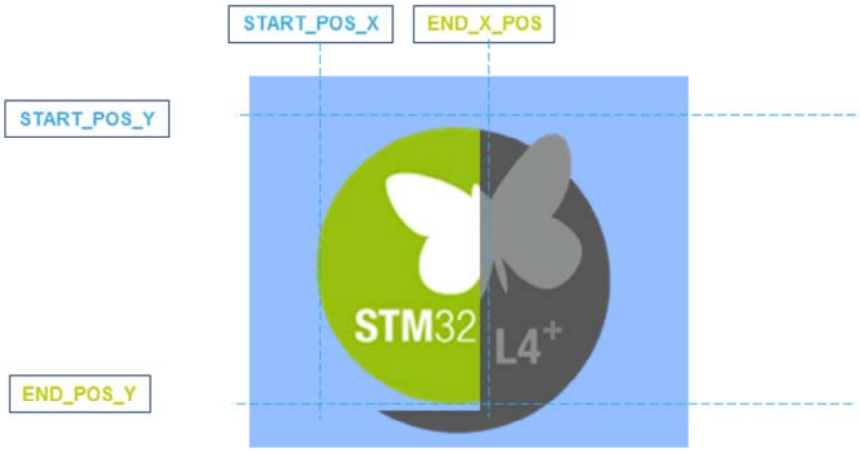
It supports up to 256 entries per layer.

The frame buffer contains an index value for each pixel.

The CLUT has to be loaded with the R, G and B values that will replace the original R, G, B values of that pixel (indexed color). Each color (RGB value) has its own address which corresponds to the position within the CLUT.

Layer Programmable Parameters

Flexible window position and size configuration



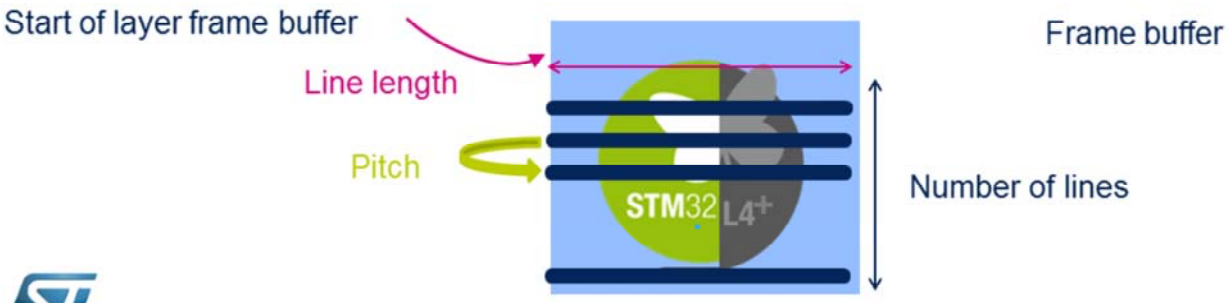
Every layer can be positioned and resized.

The programmable layer position and size define the first/last visible pixel of a line and the first/last visible line in the window. It enables the display of either the full image frame or only a part of the image frame.

Layer Programmable Parameters

Color frame buffer configuration

- The frame buffer size, line length and the number of lines parameters must be correctly configured :
  - If it is set to less bytes than required by the layer, FIFO underrun error will be set.
  - If it is set to more bytes than actually required by the layer, the useless data read is discarded. The useless data is not displayed.



Every layer has a configurable number of lines and line length for the color frame buffer and the pitch.

The pitch is the distance between the start of one line and the beginning of the next line in bytes.

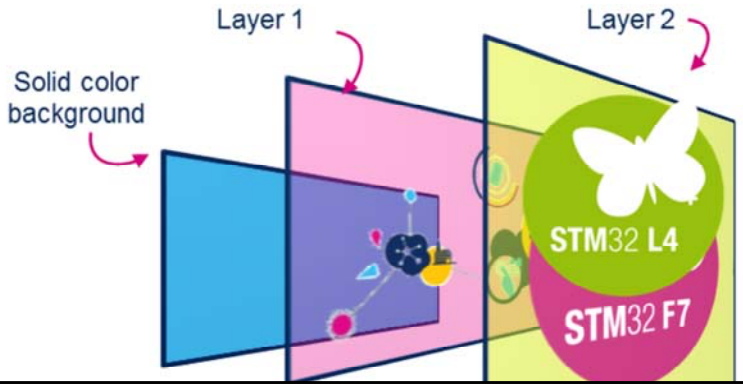
These parameters are expressed in bytes – NOT in pixels! So their values depend on the number of bits per pixel.

The line length and the number of lines parameters are used to stop the prefetching of data from the layer FIFO at the end of the frame buffer.

Layer Programmable Parameters

Multi-layer blending

- Blending is always active using alpha value
- The blending order is fixed and it is bottom up
- Programmable background color for the bottom layer



The LTDC features configurable blending factors. The blending order is fixed and it is bottom up. If two layers are enabled, Layer1 is first blended with the background color, then Layer2 is blended with the result of the previous blending.

Layer Programmable Parameters

Default Color configuration

- The default color (ARGB) is used outside the defined layer window or when a layer is disabled.
- Tricky use case:
  - Layer 1 is enabled
  - Layer 2 is disabled, with default color black.
  - If blending factor is set to Constant Alpha (0xFF), no image is displayed. Only the black window is displayed (default color of layer 2 is black).
- To bypass the default color, set the blending factor to transparent Alpha (0x00).

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Each layer can have a default color in the ARGB format which is used outside the defined layer window or when a layer is disabled.
Here is a tricky use case:

- Layer 1 is enabled
- Layer 2 is disabled, with default color set to black.

If the blending factor is set to Constant Alpha=0xFF, no image is displayed. Only the black window is displayed (default color of layer2 is black).
To bypass the default color, set the blending factor to transparent: Alpha= 0x00.

Layer Programmable Parameters

Color keying

- Transparent color (RGB) can be defined for each layer in the LTDC_LxCKCR register
- When Color Keying is enabled, the current pixels are compared to the color key. If they match for the programmed RGB value, all channels (ARGB) of that pixel are set to 0.
- Color Keying can be enabled on the fly for each layer in the **LTDC_LxCR** register

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A color key (RGB) can be configured to be representative for a transparent pixel.
If Color Keying is enabled, the current pixels (after format conversion and before blending) are compared to the color key. If they match for the programmed RGB value, all channels (ARGB) of that pixel are set to 0.
The Color Key value can be configured and used at run-time to replace the pixel RGB value.
Color Keying is enabled through the LTDC_LxCKCR register.

LTDC Interrupts

Interrupt event	Description
Line	Line Interrupt is generated when a programmed position line is reached.
Register Reload	Register Reload interrupt is generated when the shadow registers reload was performed during the vertical blanking period
FIFO underrun	FIFO Underrun interrupt is generated when a pixel is requested from an empty layer FIFO
Transfer Error	Transfer Error interrupt is generated when an AHB bus error occurs during data transfer

A Line interrupt is :

- Generated when a programmed line position is reached.

A Register Reload interrupt is:

- Generated when the shadow registers are reloaded during the vertical blanking period.

A FIFO Underrun interrupt is:

- Generated when a pixel is requested from an empty layer FIFO.

A Transfer Error interrupt is:

- Generated when an AHB bus error occurs during data transfer.

Low-power Modes

Mode	Description
Run	Active.
Sleep	Active. Peripheral interrupts cause the device to exit Sleep mode.
Low-power run	NA
Low-power sleep	NA.
Stop 0/Stop 1 /Stop 2	Frozen. Peripheral registers content is kept.
Standby	Powered-down. The peripheral must be reinitialized after exiting Standby mode.
Shutdown	Powered-down. The peripheral must be reinitialized after exiting Shutdown mode.

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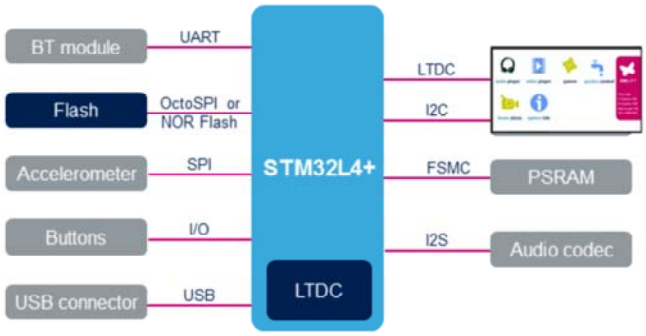
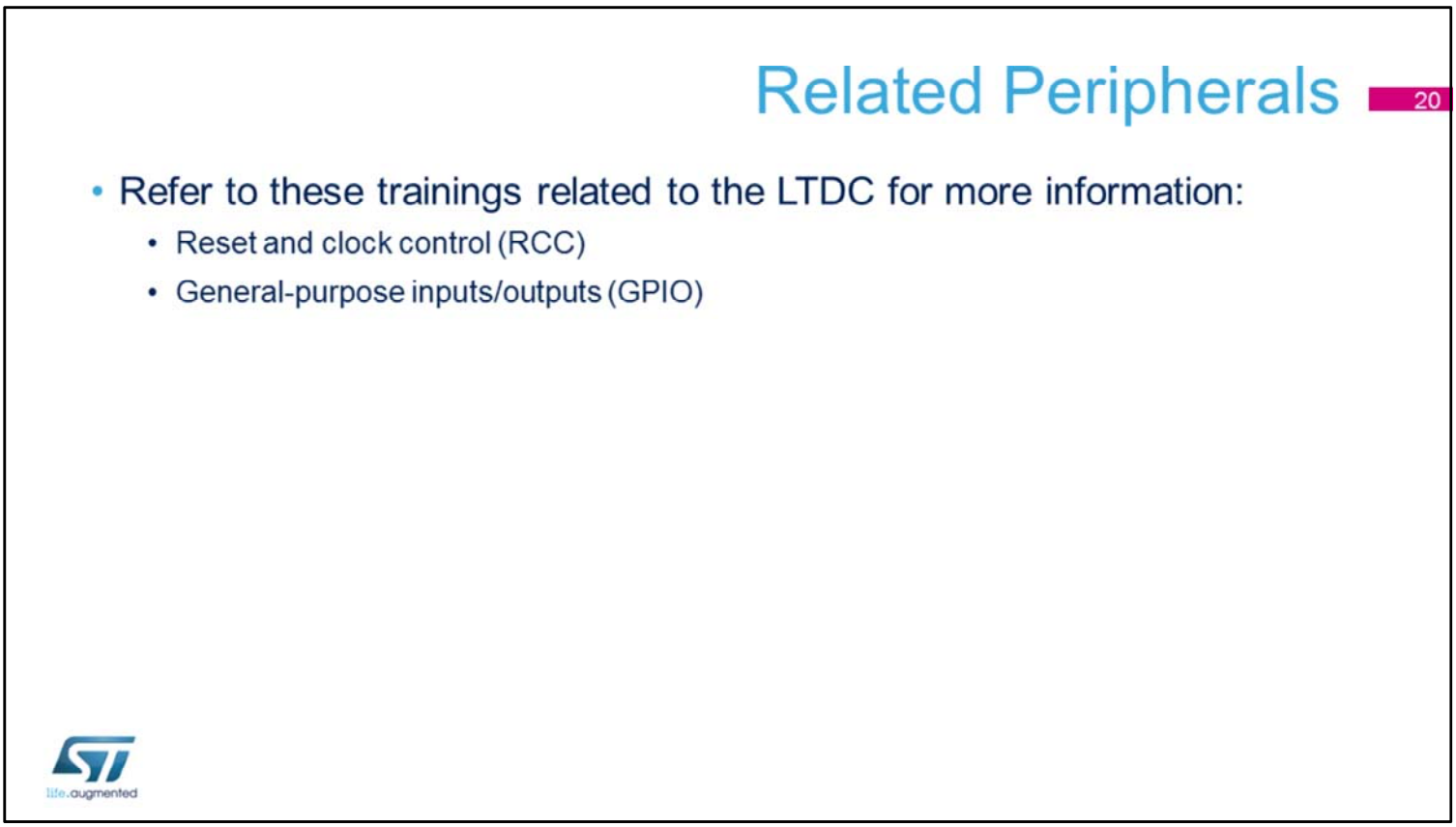
The LTDC is active in Run and Sleep modes. A LTDC interrupt can cause the device to exit Sleep mode.
In Stop 0, Stop1 or Stop2 mode, the LTDC is frozen and its registers content are kept. In Standby or Shutdown mode, the LTDC is powered-down and it must be reinitialized afterwards.

Application Example

- Home appliances including connectivity and HMI



Graphic applications require a high-quality user interface. This can be achieved using the STM32L4+ to connect the display thanks to the LCD-TFT controller.
In addition, the FSMC or OctoSPI interface may be used to access an external Flash memory containing all of the graphical content needed such as background images, high-resolution icons, or fonts to support multiple languages.



This is a list of peripherals related to the LTDC. Please refer to these peripheral trainings for more information if needed.

- Reset and clock control (RCC)
- General-purpose inputs/outputs (GPIO)