STM32L4 - PWR

Power control

Revision 3.3

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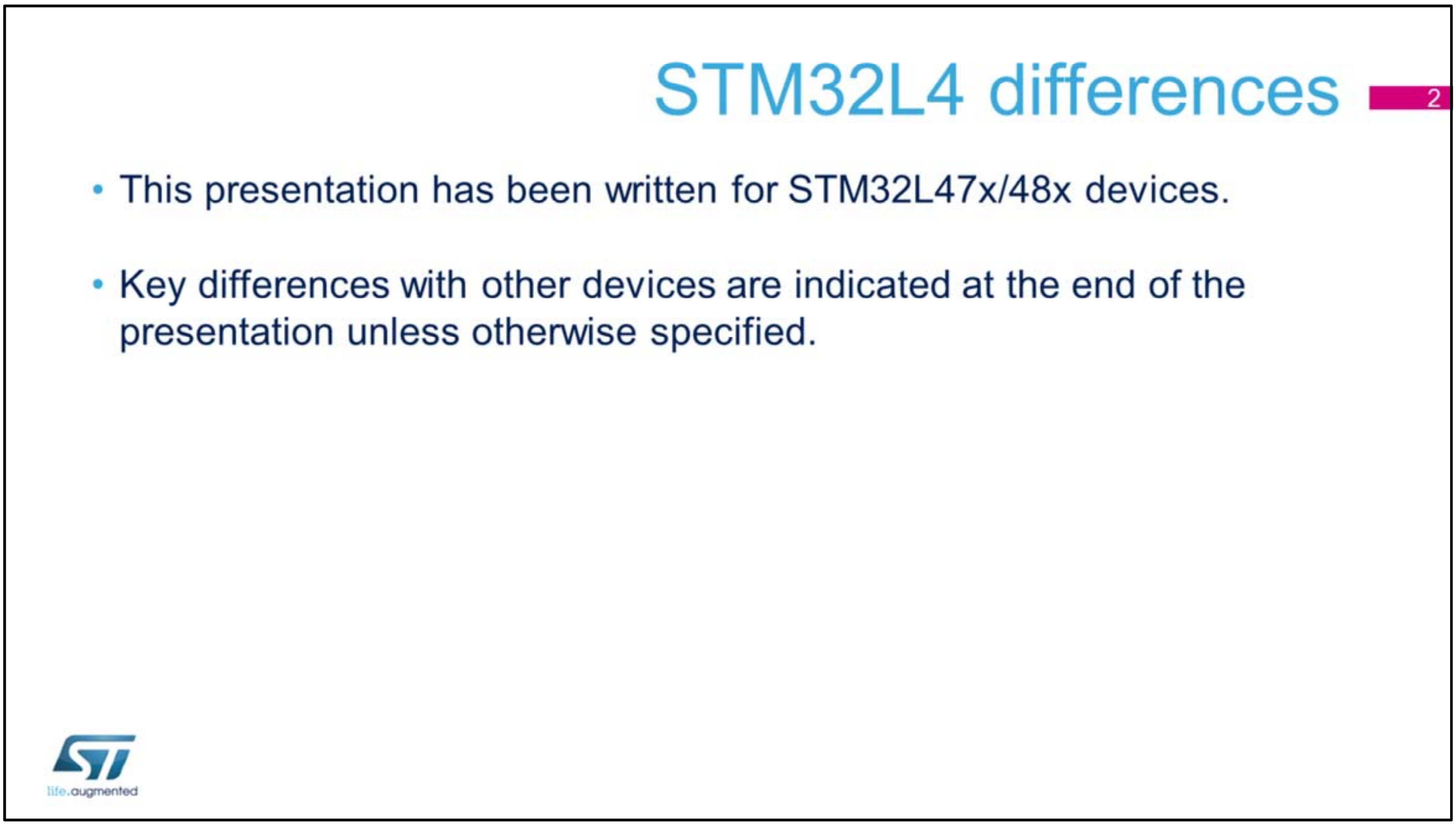
Hello, and welcome to this presentation of the STM32L4 power controller. The STM32L4’s power management functions and all power modes will also be covered in this presentation.



STM32L4 differences

- This presentation has been written for STM32L47x/48x devices.
- Key differences with other devices are indicated at the end of the presentation unless otherwise specified.

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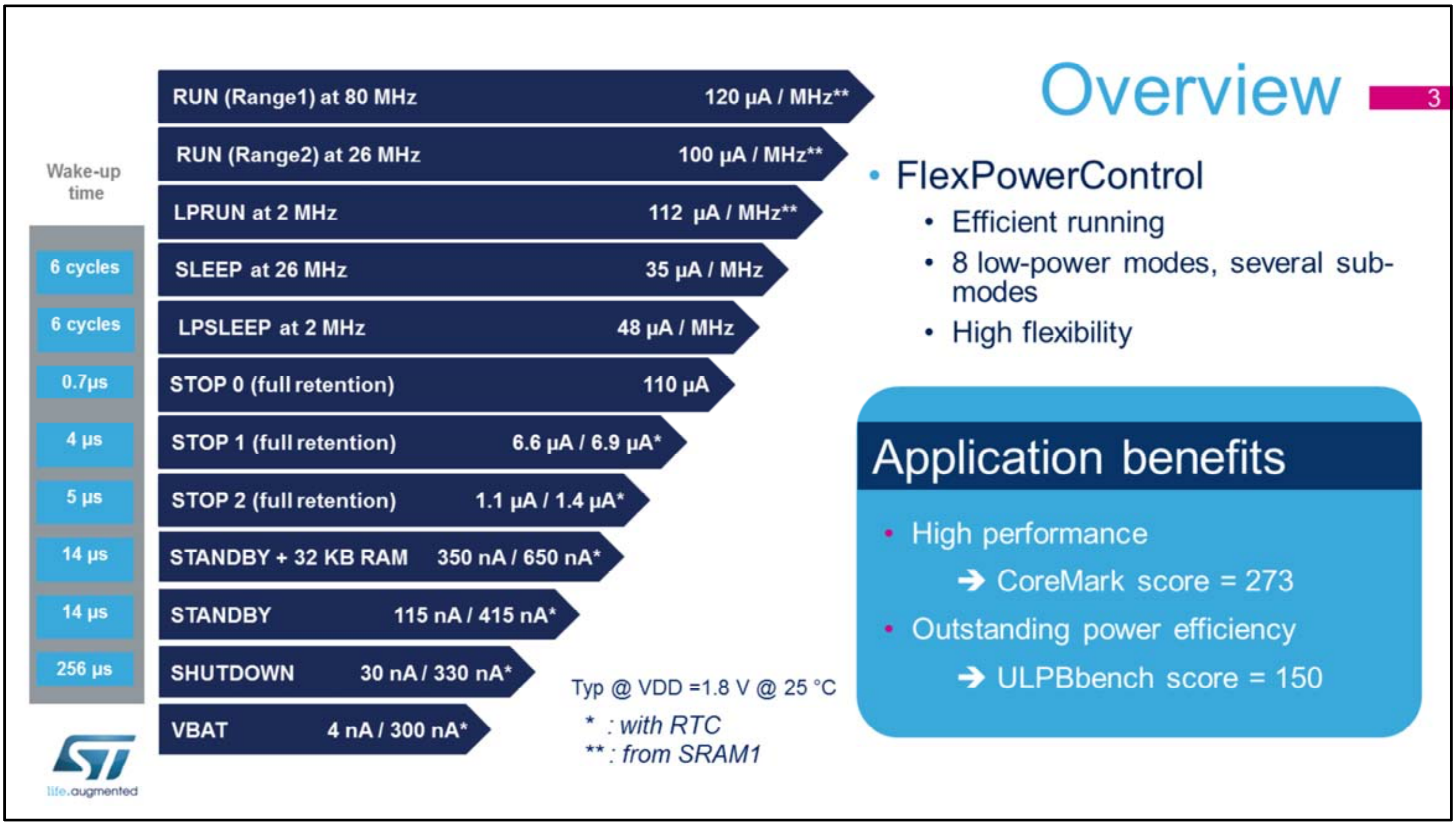


Overview

Wake-up time		
	RUN (Range1) at 80 MHz	120 µA / MHz**
	RUN (Range2) at 26 MHz	100 µA / MHz**
	LPRUN at 2 MHz	112 µA / MHz**
6 cycles	SLEEP at 26 MHz	35 µA / MHz
6 cycles	LPSLEEP at 2 MHz	48 µA / MHz
0.7µs	STOP 0 (full retention)	110 µA
4 µs	STOP 1 (full retention)	6.6 µA / 6.9 µA*
5 µs	STOP 2 (full retention)	1.1 µA / 1.4 µA*
14 µs	STANDBY + 32 KB RAM	350 nA / 650 nA*
14 µs	STANDBY	115 nA / 415 nA*
256 µs	SHUTDOWN	30 nA / 330 nA*
	VBAT	4 nA / 300 nA*

Typ @ VDD =1.8 V @ 25 °C

* : *with RTC*

** : *from SRAM1*

- FlexPowerControl
  - Efficient running
  - 8 low-power modes, several sub-modes
  - High flexibility

Application benefits

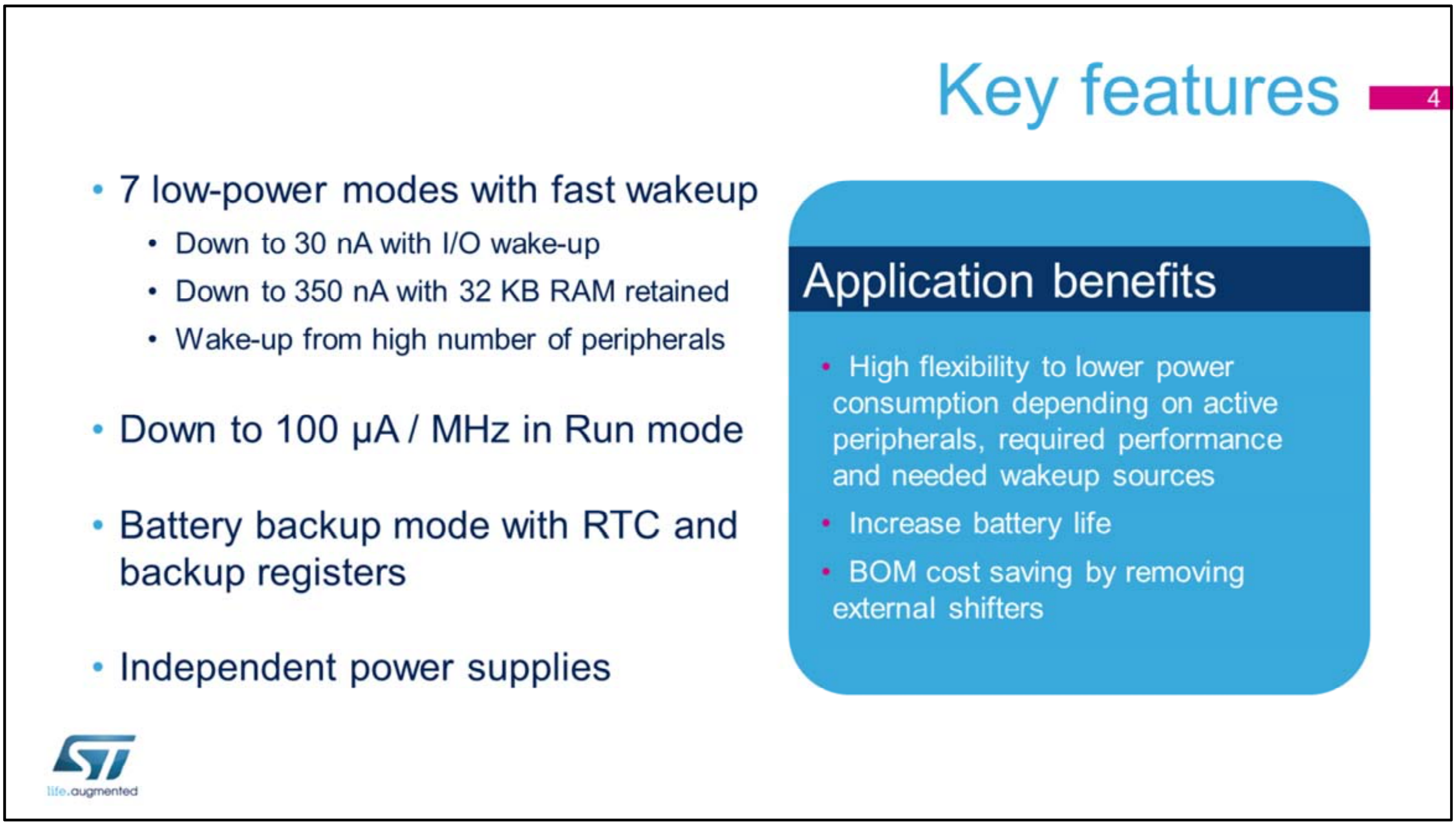
- High performance
  - ➔ CoreMark score = 273
- Outstanding power efficiency
  - ➔ ULPBbench score = 150

STM32L4 devices feature FlexPowerControl, which increases flexibility in power mode management and further reduces the overall application consumption. Run mode can support a system clock running at up to 80 MHz, with only 120 µA/MHz. At 26 MHz, the consumption is even lower: 100 µA/MHz.

STM32L4 devices support 8 main low-power modes: Low-power run, Sleep, Low-power sleep, Stop 0, Stop 1, Stop 2, Standby and Shutdown modes. Each mode can be configured in many ways, providing several additional sub-modes.

In addition, STM32L4 devices support a battery backup domain, called VBAT.

The high flexibility in power management provides both high performance with a CoreMark score equal to 273, together with outstanding power efficiency, demonstrated by the ULPBench score equal to 150.



Key features

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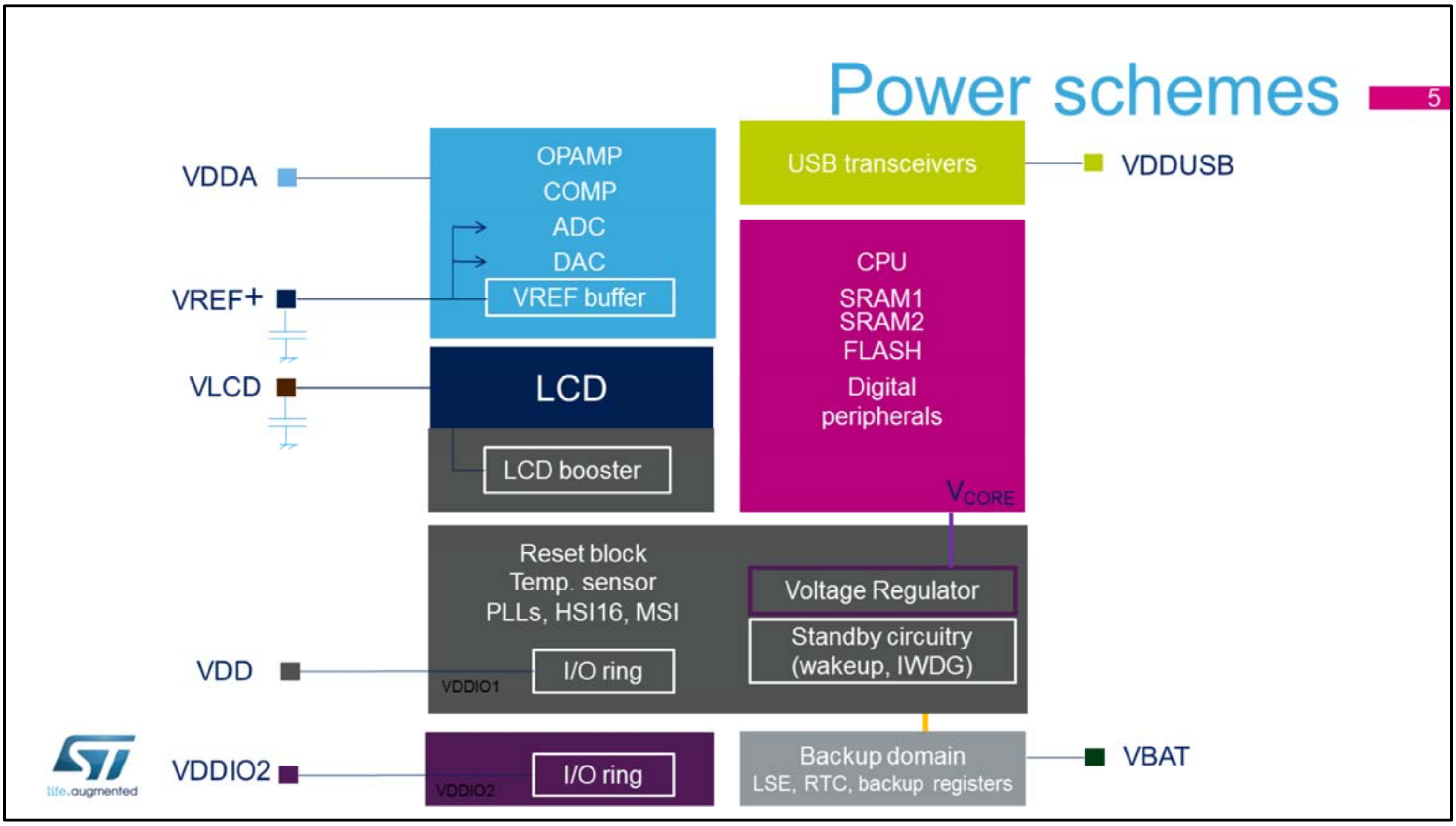
- 7 low-power modes with fast wakeup
  - Down to 30 nA with I/O wake-up
  - Down to 350 nA with 32 KB RAM retained
  - Wake-up from high number of peripherals
- Down to 100 µA / MHz in Run mode
- Battery backup mode with RTC and backup registers
- Independent power supplies

Application benefits

- High flexibility to lower power consumption depending on active peripherals, required performance and needed wakeup sources
- Increase battery life
- BOM cost saving by removing external shifters

The STM32L4 has several key features related to power management:
Several low-power modes, down to 30nA while it is still possible to wake up the MCU with an event on an I/O. For only 350 nA, 32 kilobytes of SRAM can be retained. A large number of peripherals can wake up from the various low-power modes.
Dynamic consumption is down to 100 µA/MHz, executing from Flash memory.
A battery backup domain, called VBAT, including the RTC and certain backup registers.
Several power supplies are independent, allowing to reduce MCU power consumption while some peripherals are supplied at higher voltages.

Thanks to the large number of power modes, STM32L4 devices offer high flexibility to minimize the power consumption and adjust it depending on active peripherals, required performance and needed wake-up sources.



Power schemes

VDDA

OPAMP

COMP

ADC

DAC

VREF buffer

VREF+

VLCD

LCD

LCD booster

USB transceivers

VDDUSB

CPU

SRAM1

SRAM2

FLASH

Digital peripherals

V_{CORE}

Reset block

Temp. sensor

PLLs, HSI16, MSI

Voltage Regulator

Standby circuitry (wakeup, IWDG)

VDD

VDDIO1

I/O ring

VDDIO2

I/O ring

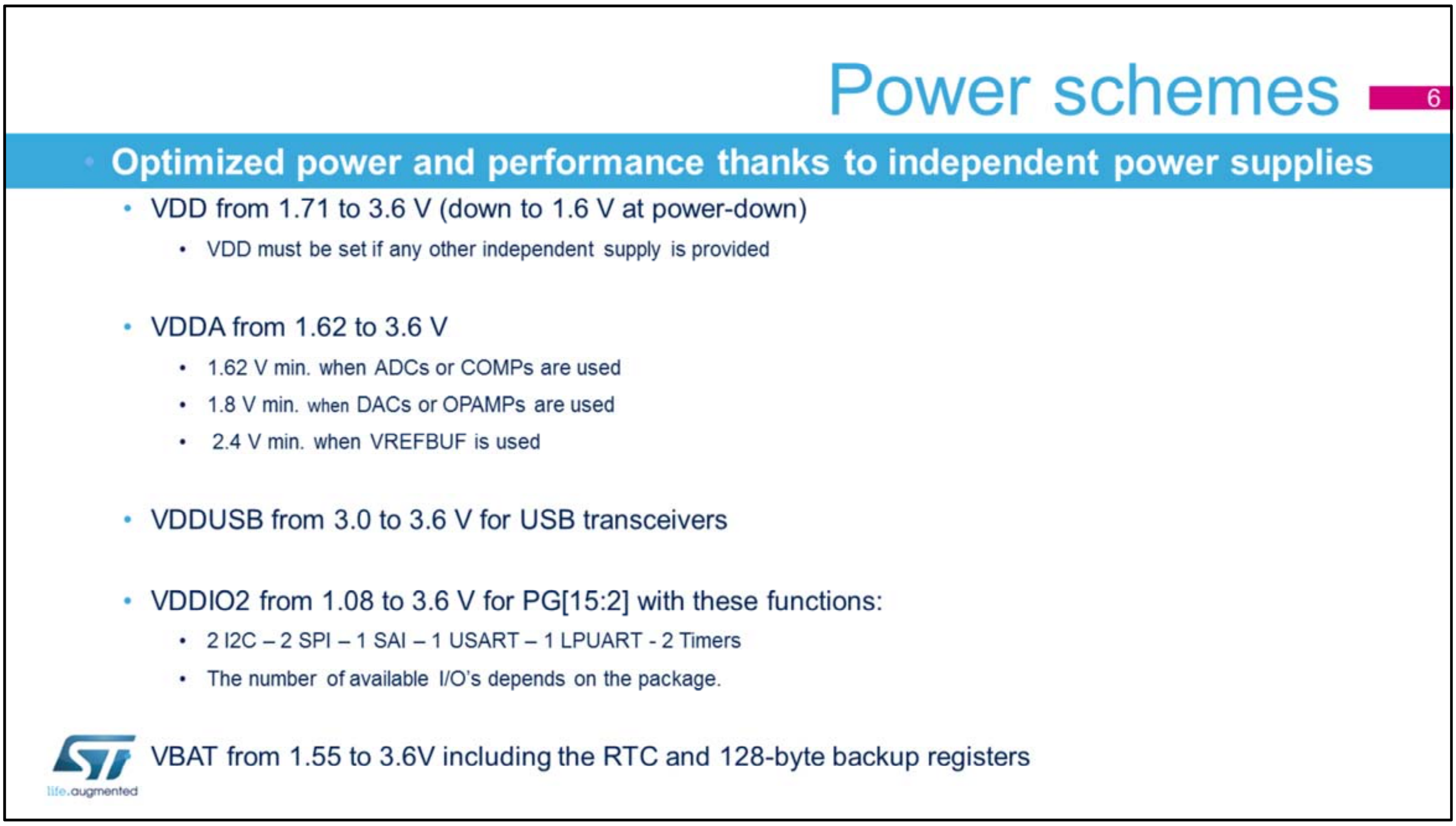
Backup domain

LSE, RTC, backup registers

VBAT

STM32L4 devices have several independent power supplies, which can be set at different voltages or tied together. The main power supply is VDD, supplying almost all I/Os except for 14 I/Os of Port G. VDD also supplies the reset block, temperature sensor and all internal clock sources. In addition, it supplies the Standby circuitry which includes the wakeup logic and independent watchdog. VDD supplies voltage regulators which provide the VCORE supply. VCORE supplies most of the digital peripherals, SRAMs and Flash. STM32L4 MCUs feature several independent supplies for peripherals: VDDA for the analog peripherals, VDDUSB for the USB transceiver and VDDIO2 which supplies the 14 I/Os on Port G. The VLCD pin provides the LCD common and segments reference voltage. The VREF+ pin provides the reference voltage to the analog-to-digital and to digital-to-analog converters and can be used as an external buffer reference for the application.

A backup battery can be connected to VBAT pin to supply the backup domain.



Power schemes

Optimized power and performance thanks to independent power supplies

- VDD from 1.71 to 3.6 V (down to 1.6 V at power-down)
  - VDD must be set if any other independent supply is provided
- VDDA from 1.62 to 3.6 V
  - 1.62 V min. when ADCs or COMPs are used
  - 1.8 V min. when DACs or OPAMPs are used
  - 2.4 V min. when VREFBUF is used
- VDDUSB from 3.0 to 3.6 V for USB transceivers
- VDDIO2 from 1.08 to 3.6 V for PG[15:2] with these functions:
  - 2 I2C – 2 SPI – 1 SAI – 1 USART – 1 LPUART - 2 Timers
  - The number of available I/O's depends on the package.
- VBAT from 1.55 to 3.6V including the RTC and 128-byte backup registers

The main power supply VDD ensures full feature operation in all power modes from 1.71 up to 3.6 V, allowing to be supplied by an external 1.8 V regulator. Device functionality is guaranteed down to 1.6 V, the minimum voltage after which a brown-out reset is generated. Other independent supplies are provided to allow peripherals to operate at a different voltage.

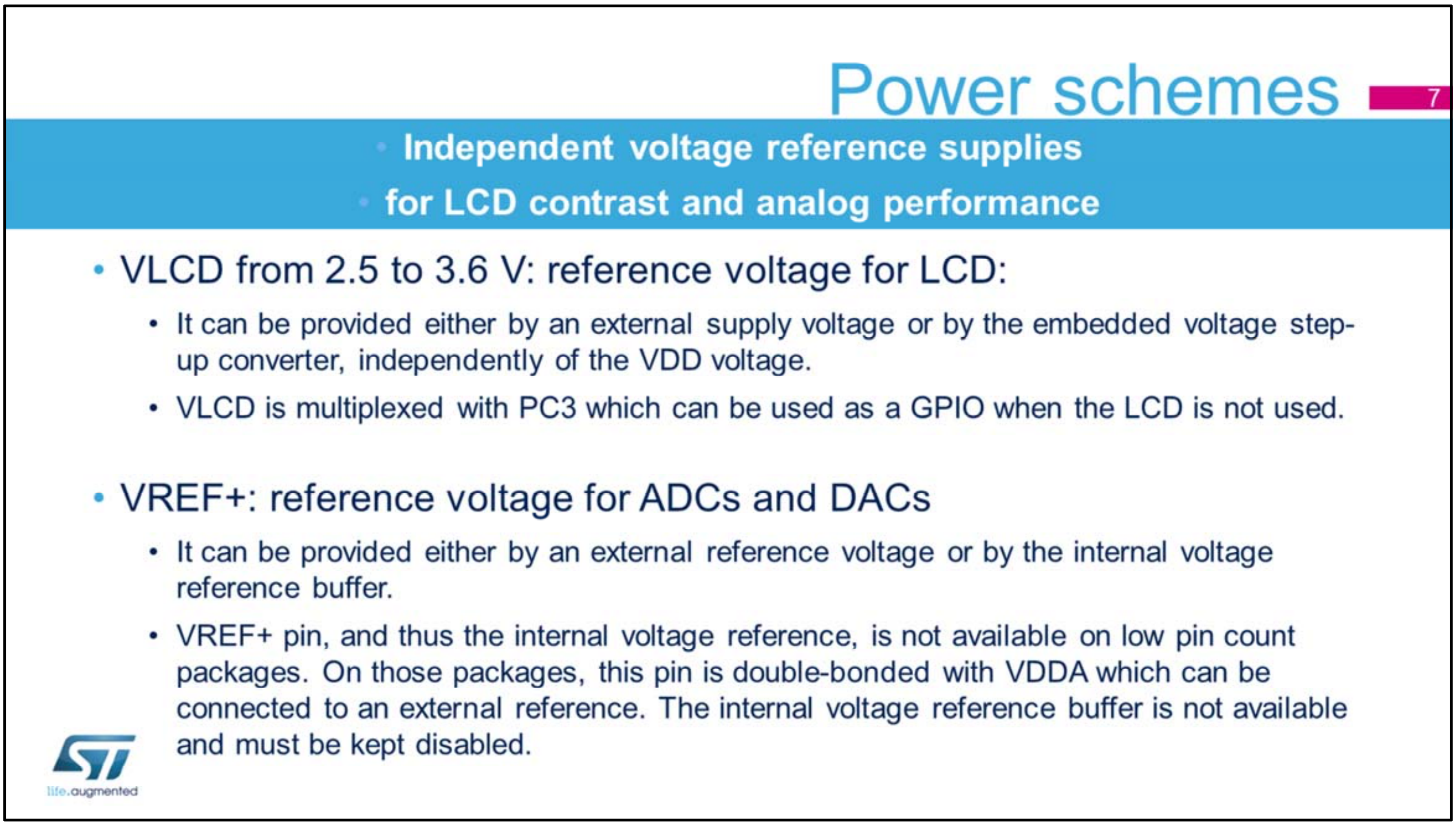
The analog power supply VDDA can be connected to any voltage other than VDD. When the analog-to-digital converters or comparators are used, the VDDA voltage must be greater than 1.62 V. When the digital-to-analog converters or operational amplifiers are used, VDDA must be greater than 1.8 V. When the voltage reference buffer is used, VDDA must be greater than 2.4 V.

The USB power supply VDDUSB can be connected to any voltage other than VDD. When the USB is used, VDDUSB must be greater than 3 V.

14 I/Os of Port G, from PG15 to PG2, are supplied by

VDDIO2 independently from VDD. When these I/Os are used, VDDIO2 can be as low as 1.08 V. Several functions are available on these I/Os: I2C , SPI , serial audio interface, USARTs and Timers. The number of available I/O’s depends on the package.

A backup domain is supplied by VBAT, which must be greater than 1.55 V. The backup domain contains the RTC, the 32.768-kHz LSE external oscillator and the 128-byte backup registers.

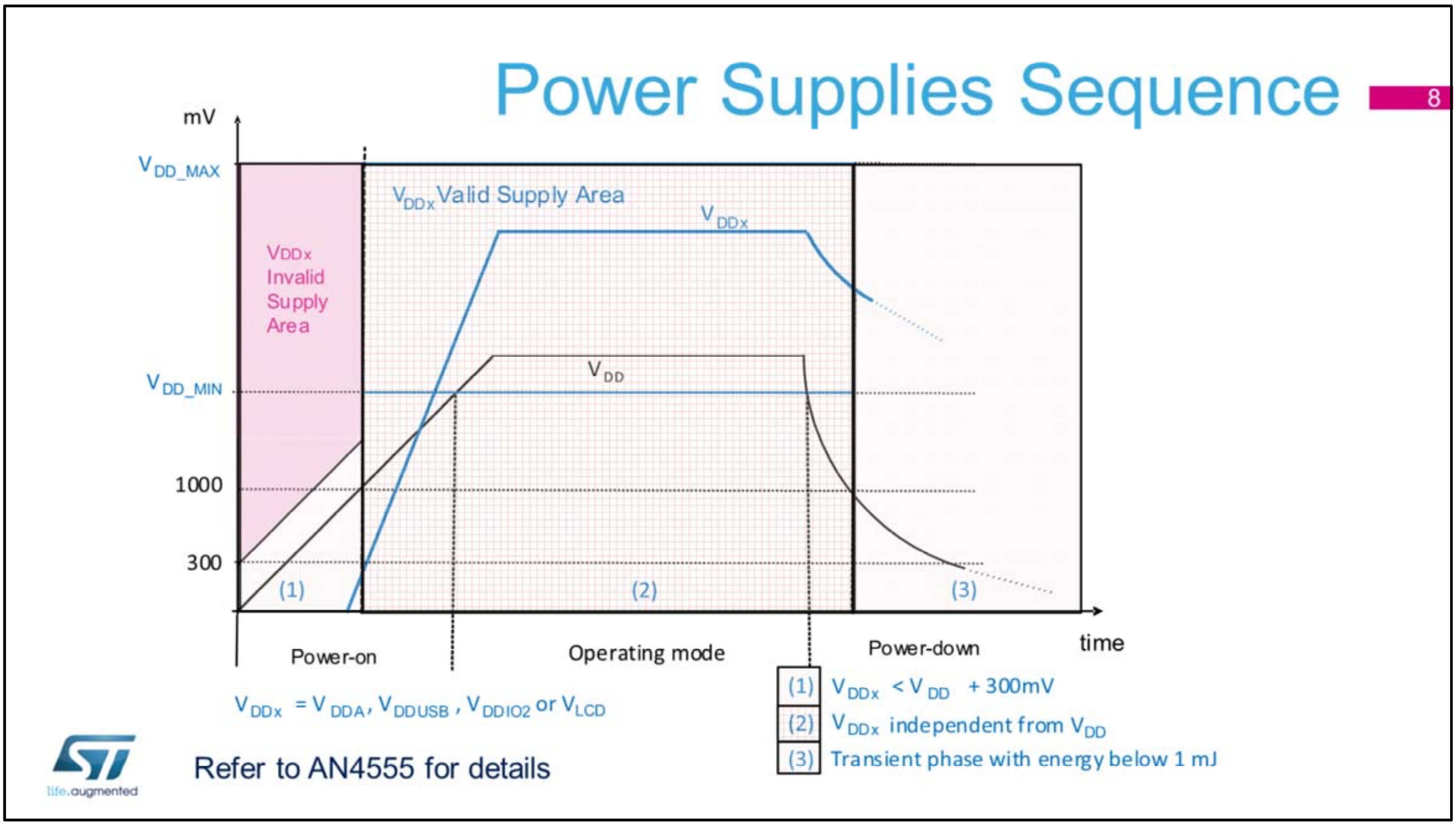


Power schemes

Independent voltage reference supplies for LCD contrast and analog performance

- VLCD from 2.5 to 3.6 V: reference voltage for LCD:
  - It can be provided either by an external supply voltage or by the embedded voltage step-up converter, independently of the VDD voltage.
  - VLCD is multiplexed with PC3 which can be used as a GPIO when the LCD is not used.
- VREF+: reference voltage for ADCs and DACs
  - It can be provided either by an external reference voltage or by the internal voltage reference buffer.
  - VREF+ pin, and thus the internal voltage reference, is not available on low pin count packages. On those packages, this pin is double-bonded with VDDA which can be connected to an external reference. The internal voltage reference buffer is not available and must be kept disabled.

The LCD reference voltage can be provided either by an external supply voltage or by the embedded voltage step-up converter. This reference is independent from the VDD voltage, ensuring the same LCD contrast regardless of the VDD value. VLCD is multiplexed with the PC3 pin which can be used as a GPIO when the LCD is not used.
The ADC and DAC voltage references can be provided either by an external supply voltage or by the internal reference buffer. This allows us to improve converters performance by providing an isolated and independent reference voltage. The VREF+ pin and thus the internal voltage reference, is not available on low pin count packages. In those packages, the VREF+ is double-bonded with VDDA and the internal voltage buffer must be kept disabled. The voltage reference can be provided through the VDDA pin in those packages



Power Supplies Sequence

$V_{DDx} = V_{DDA}, V_{DDUSB}, V_{DDIO2}$ or V_{LCD}

(1) $V_{DDx} < V_{DD} + 300mV$

(2) V_{DDx} independent from V_{DD}

(3) Transient phase with energy below 1 mJ

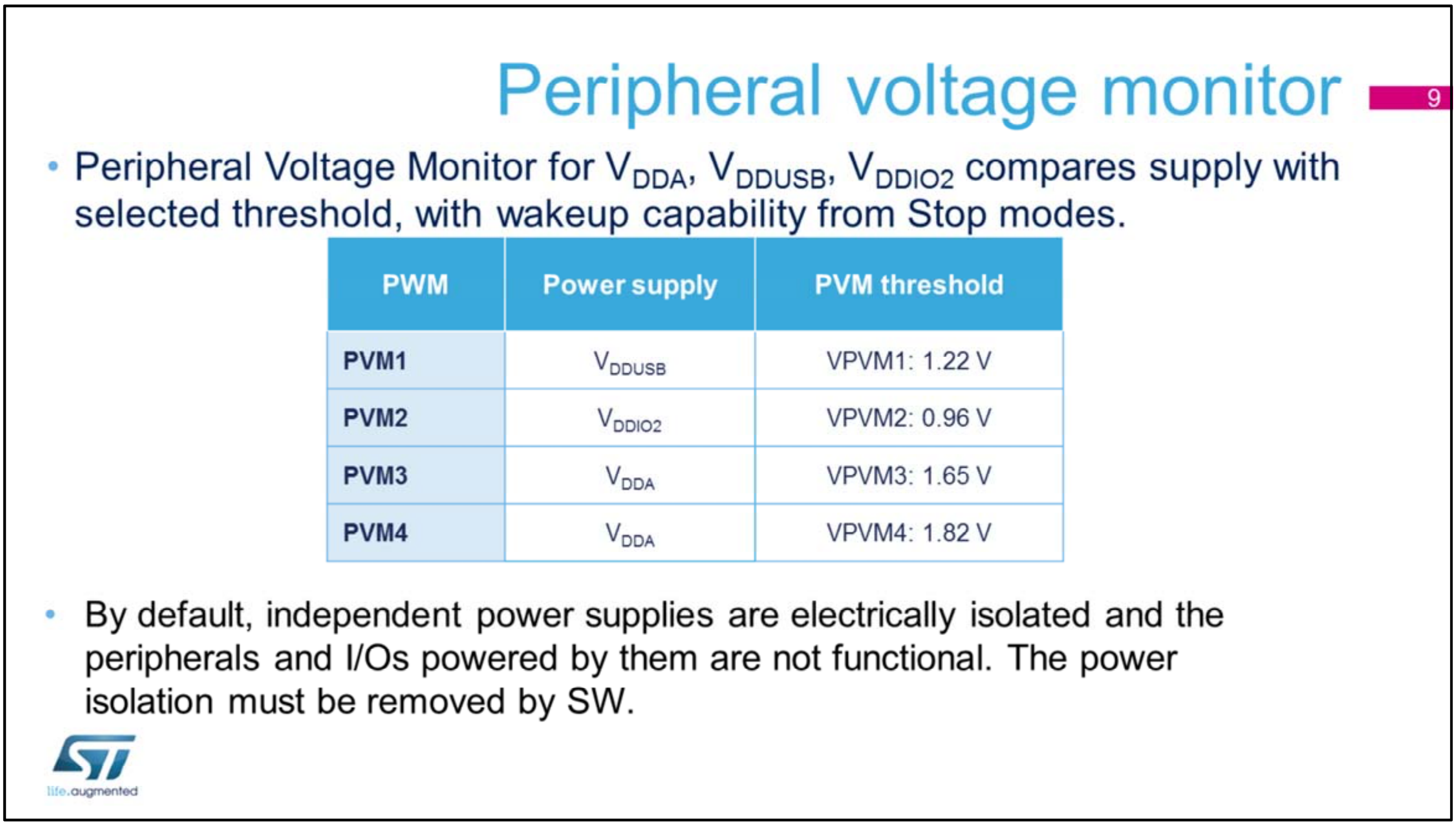
Refer to AN4555 for details

As a general requirement, the VDD power supply has to be provided first and released last.

More precisely, during the power-on phase, the following power sequence requirements must be respected:
- When VDD is below 1 Volt, other power supplies (VDDA, VDDIO2, VDDUSB and VLCD) must remain below VDD +300 millivolts.
- When VDD is above 1 Volt, all power supplies become independent.

During the power-down phase, VDD has to be switched off at the same time or after other power supplies. But VDD can temporarily become lower than other supplies provided that the energy absorbed by the MCU during this transient phase remains below 1 mJ.

Refer to the application note AN4555 for more details on the power supplies sequencing.



Peripheral voltage monitor

- Peripheral Voltage Monitor for V_{DDA}, V_{DDUSB}, V_{DDIO2} compares supply with selected threshold, with wakeup capability from Stop modes.

PWM	Power supply	PVM threshold
PVM1	V_{DDUSB}	VPVM1: 1.22 V
PVM2	V_{DDIO2}	VPVM2: 0.96 V
PVM3	V_{DDA}	VPVM3: 1.65 V
PVM4	V_{DDA}	VPVM4: 1.82 V

- By default, independent power supplies are electrically isolated and the peripherals and I/Os powered by them are not functional. The power isolation must be removed by SW.

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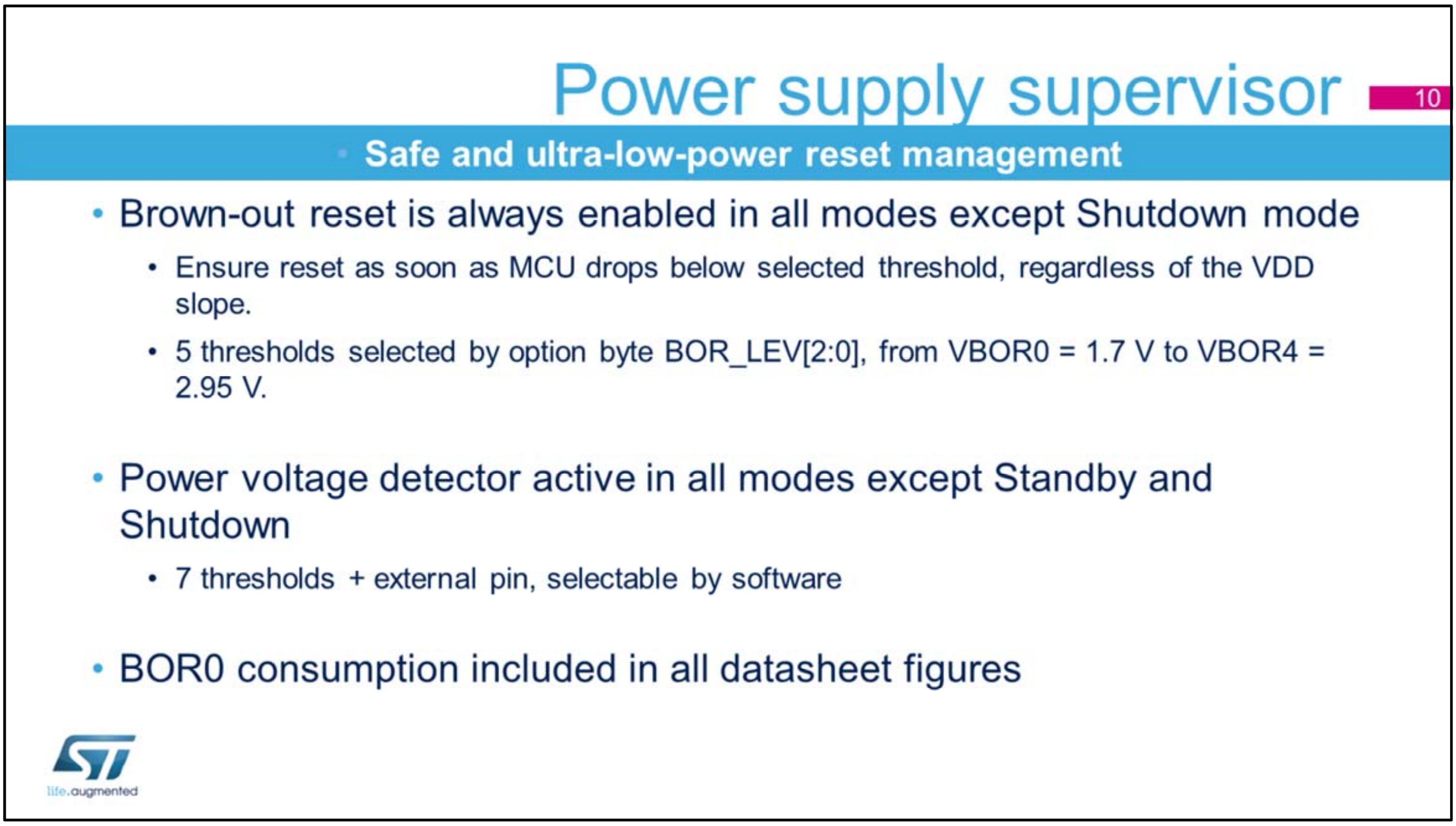
The STM32L4 MCU embeds four Peripheral Voltage Monitors to detect if the independent supply is present or not. These comparators have wake-up from Stop mode capability. The PVM1 compares the VDDUSB voltage with the 1.22 V threshold. The PVM2 compares the VDDIO2 voltage with the 0.96 V threshold. The PVM3 compares the VDDA voltage with the 1.65 V threshold, intended for the comparators and analog-to-digital converters. The PVM4 compares the VDDA voltage with the 1.82 V threshold, intended for the operational amplifiers and digital-to-analog converters.

To guarantee any of the supply sequences on the application, power isolation has been implemented and is active by default. It is the role of software to enable the needed supplies by removing the power isolation.

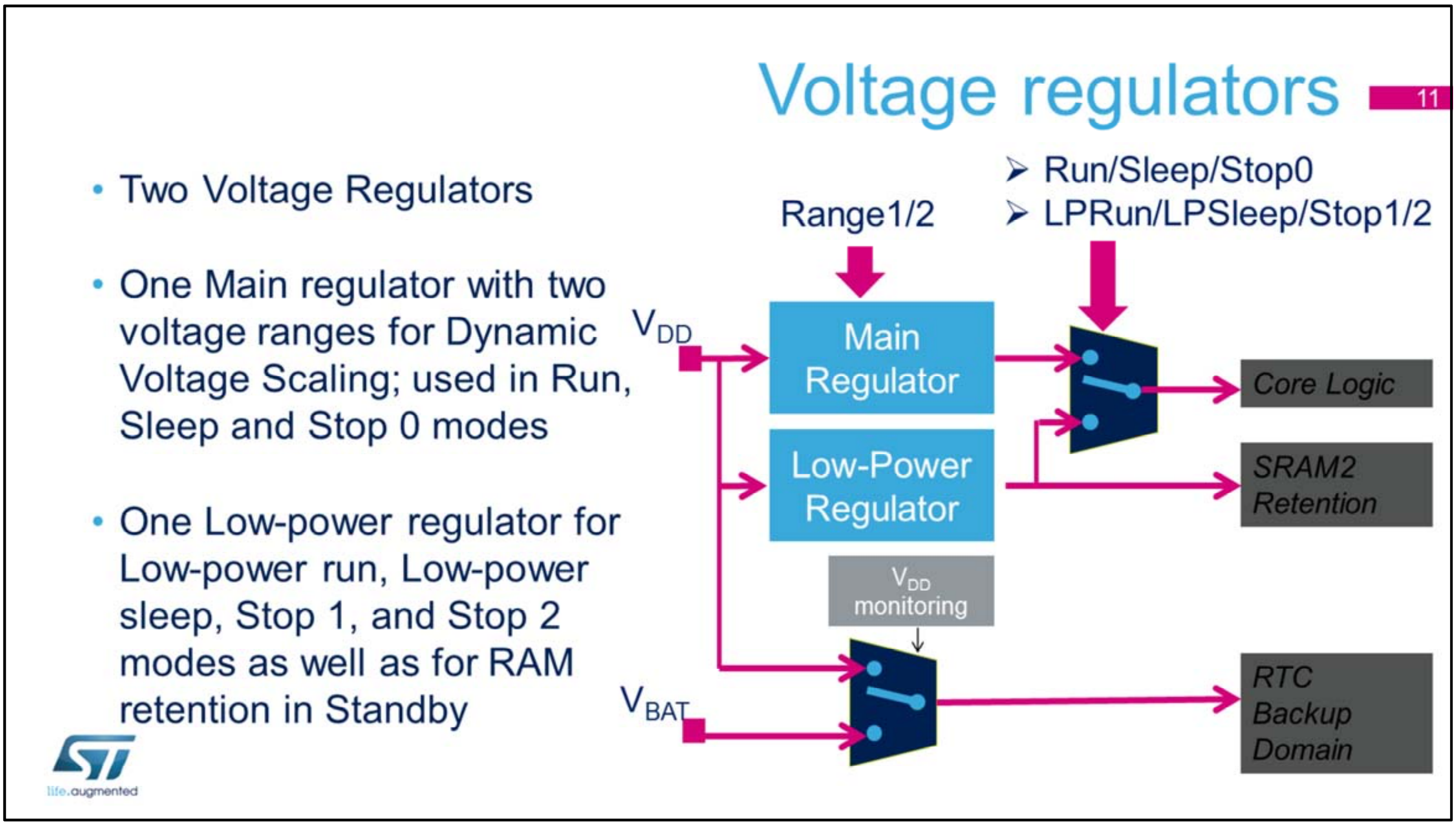


Power supply supervisor

- Safe and ultra-low-power reset management

- Brown-out reset is always enabled in all modes except Shutdown mode
  - Ensure reset as soon as MCU drops below selected threshold, regardless of the VDD slope.
  - 5 thresholds selected by option byte BOR_LEV[2:0], from VBOR0 = 1.7 V to VBOR4 = 2.95 V.
- Power voltage detector active in all modes except Standby and Shutdown
  - 7 thresholds + external pin, selectable by software
- BOR0 consumption included in all datasheet figures

The power supply supervisor guarantees a safe and ultra-low power reset management.
STM32L4 devices embed an ultra-low-power brown-out reset which is always enabled in all power modes except Shutdown mode. The BOR ensures reset generation as soon as the MCU drops below the selected threshold, regardless of the VDD slope. Five thresholds from 1.7 to 2.95 V are selected by option byte programmed in Flash memory.
A power voltage detector can generate an interrupt when VDD crosses the selected threshold. The PVD can be enabled in all modes except Standby and Shutdown modes. 7 thresholds can be selected by software. In addition, comparisons can be done with an external pin.
The BOR consumption with the 1.7 V threshold is included in the datasheet.

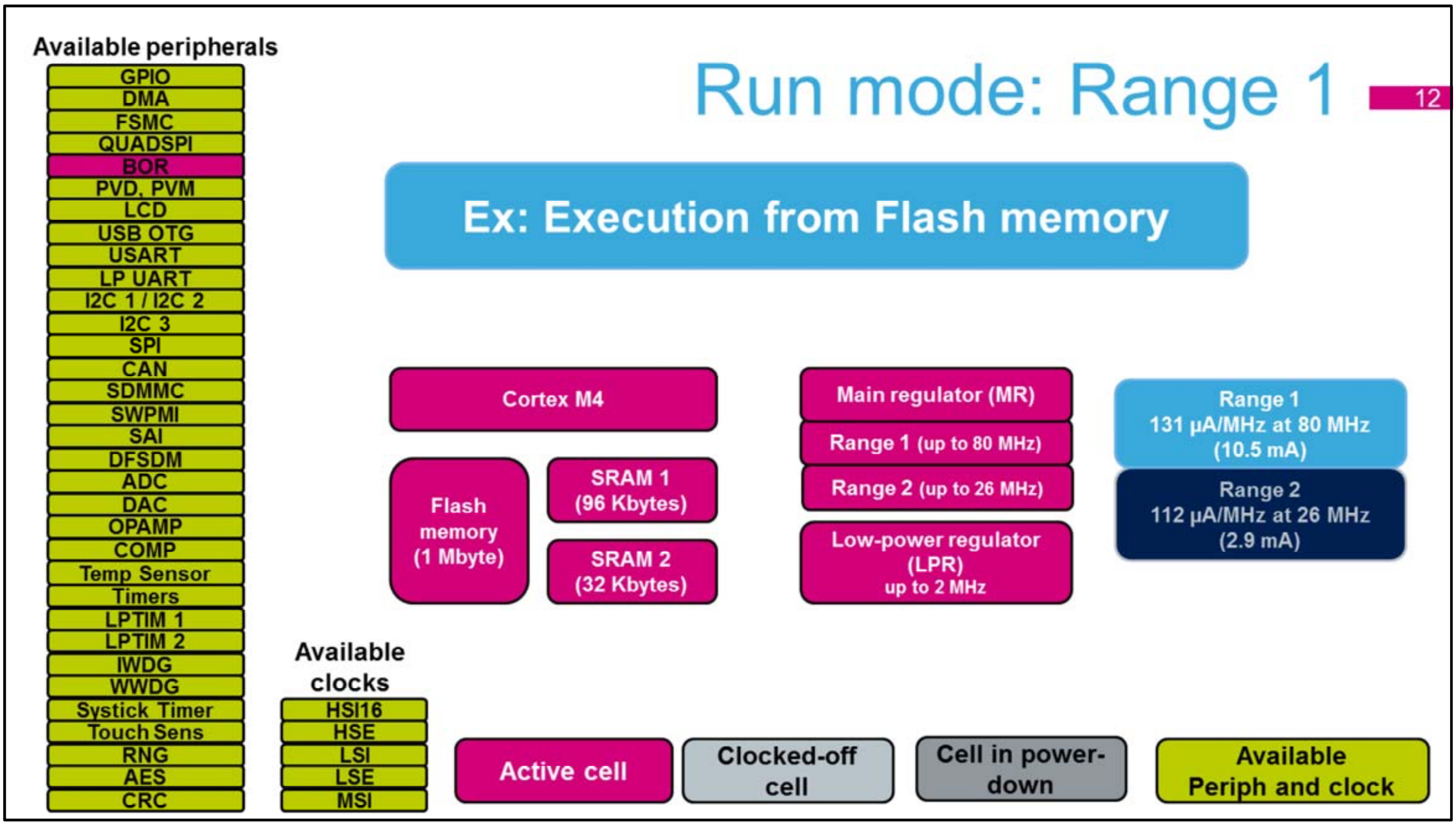


Voltage regulators

- Two Voltage Regulators
- One Main regulator with two voltage ranges for Dynamic Voltage Scaling; used in Run, Sleep and Stop 0 modes
- One Low-power regulator for Low-power run, Low-power sleep, Stop 1, and Stop 2 modes as well as for RAM retention in Standby

Two embedded linear voltage regulators supply all the digital circuitries except for the Standby circuitry and the Backup domain. The regulator output voltage (VCORE) can be programmed by software to two different values depending on the performance and the power consumption requirements. This is called Dynamic Voltage Scaling.

Depending on the application mode, VCORE is provided either by the Main voltage regulator for Run, Sleep and Stop0 modes, or by the Low-power regulator for Low-power run, Low-power sleep, Stop 0, Stop 1 and Stop 2 modes. The regulators are OFF in Standby and Shutdown mode. When SRAM2 content is preserved in Standby mode, the Low-power regulator remains ON and provides the SRAM2 supply.



Run mode: Range 1

Ex: Execution from Flash memory

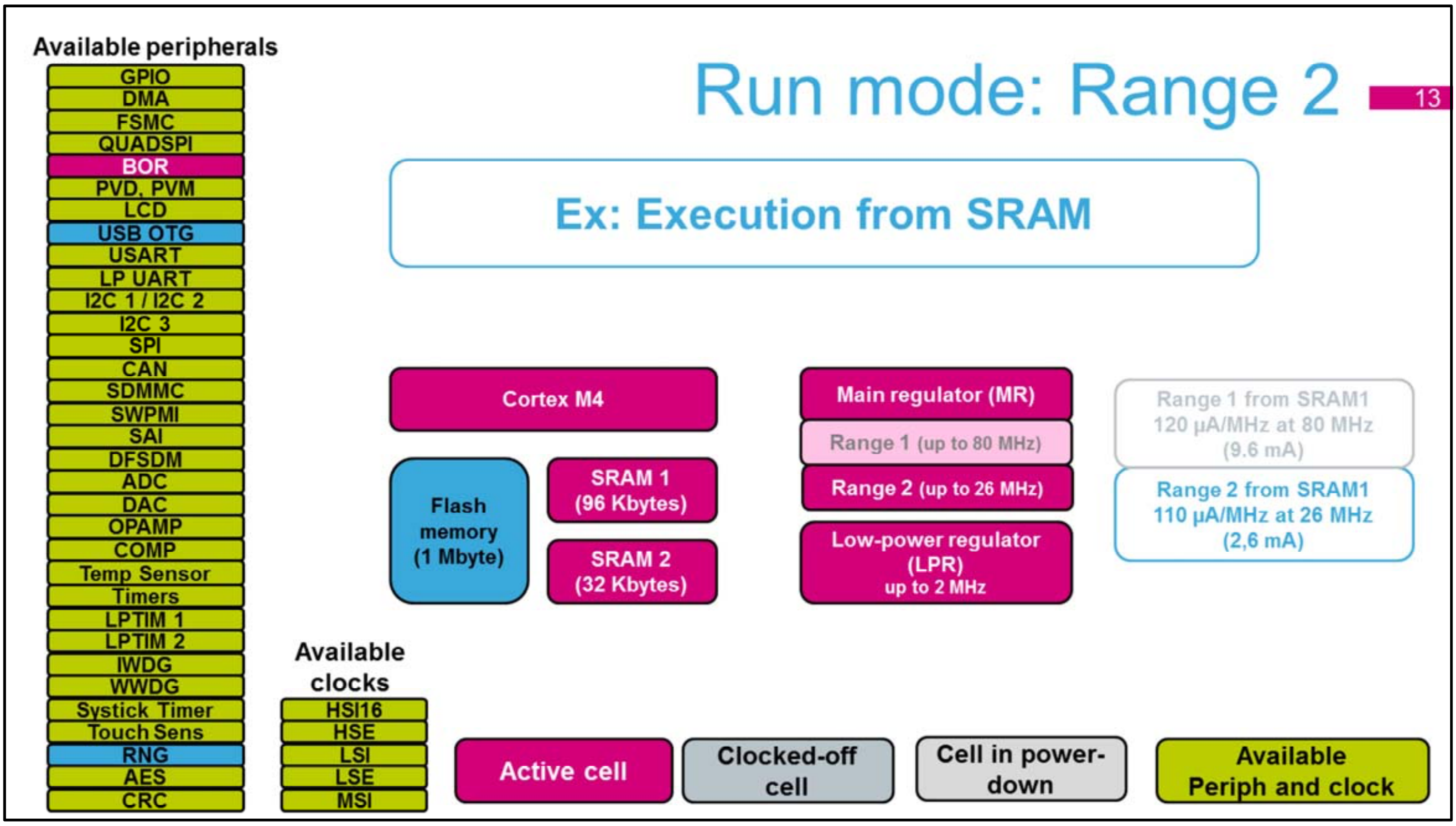
Available peripherals

- GPIO
- DMA
- FSMC
- QUADSPI
- BOR
- PVD, PVM
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
- SPI
- CAN
- SDMMC
- SWPMI
- SAI
- DFSDM
- ADC
- DAC
- OPAMP
- COMP
- Temp Sensor
- Timers
- LPTIM 1
- LPTIM 2
- IWDG
- WWDG
- Systick Timer
- Touch Sens
- RNG
- AES
- CRC

Available clocks

- HSI16
- HSE
- LSI
- LSE
- MSI

In run mode, the voltage scaling Range 1 is the high performance range, allowing a system clock up to 80 MHz.
All peripherals can be activated, all clocks can be enabled.
The Run mode range 1 consumption is 131 µA/MHz at 80 MHz, from Flash memory with the ART accelerator enabled.



Run mode: Range 2

Ex: Execution from SRAM

Available peripherals

- GPIO
- DMA
- FSMC
- QUADSPI
- BOR
- PVD, PVM
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
- SPI
- CAN
- SDMMC
- SWPMI
- SAI
- DFSDM
- ADC
- DAC
- OPAMP
- COMP
- Temp Sensor
- Timers
- LPTIM 1
- LPTIM 2
- IWDG
- WWDG
- Systick Timer
- Touch Sens
- RNG
- AES
- CRC

Available clocks

- HSI16
- HSE
- LSI
- LSE
- MSI

Cortex M4

Flash memory (1 Mbyte)

SRAM 1 (96 Kbytes)

SRAM 2 (32 Kbytes)

Main regulator (MR)

Range 1 (up to 80 MHz)

Range 2 (up to 26 MHz)

Low-power regulator (LPR) up to 2 MHz

Range 1 from SRAM1
120 µA/MHz at 80 MHz
(9.6 mA)

Range 2 from SRAM1
110 µA/MHz at 26 MHz
(2,6 mA)

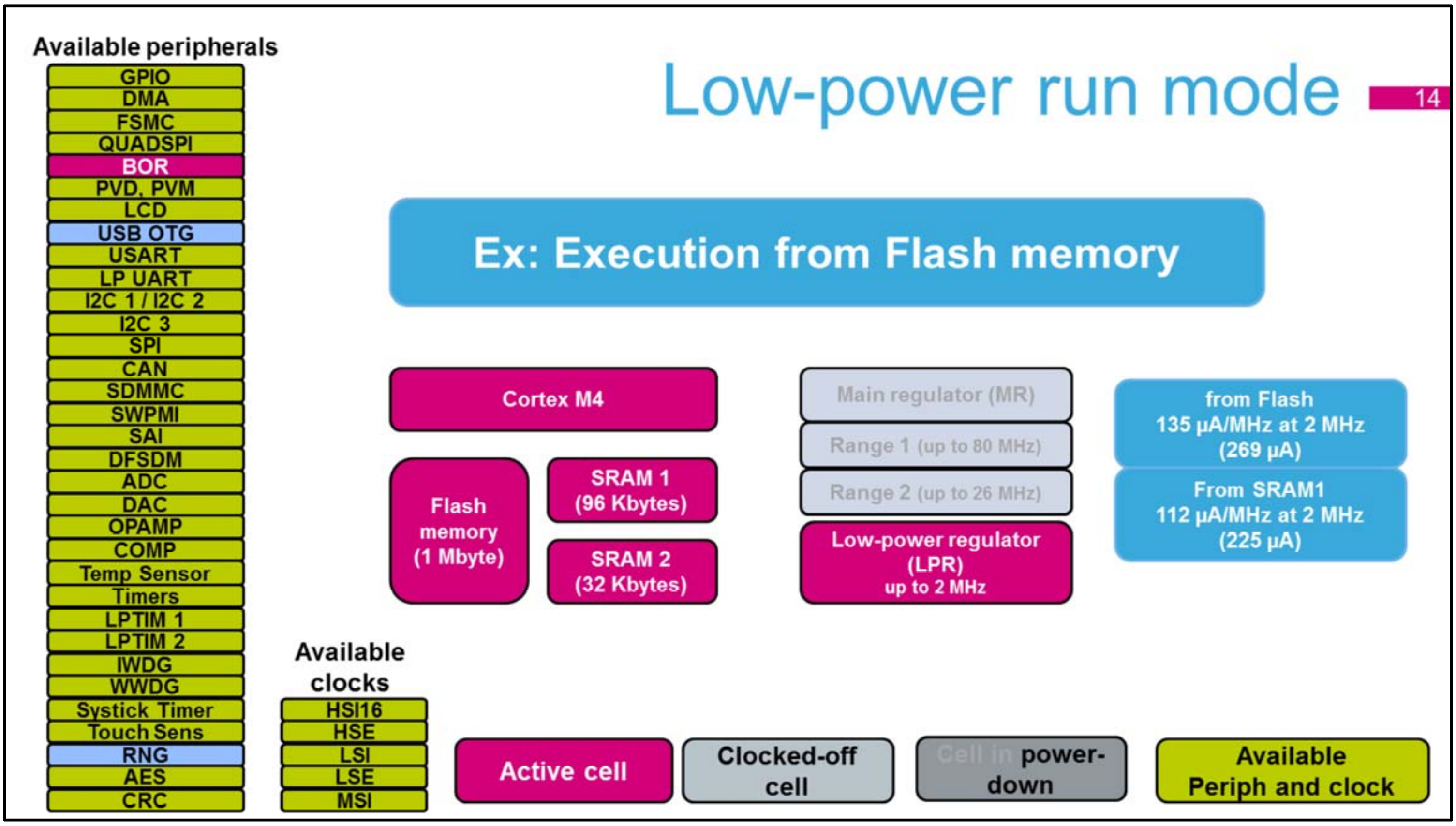
Active cell

Clocked-off cell

Cell in power-down

Available Periph and clock

In Run mode, the voltage scaling Range 2 is the medium performance range, allowing a system clock up to 26 MHz. When executing from SRAM, the Flash consumption can be saved by configuring the Flash in Power-down mode and by gating its clock off.
All peripherals can be activated except the USB OTG and Random Number Generator. All clocks can be enabled.
The Run mode range 2 consumption is 110 µA/MHz at 26 MHz from SRAM.



Low-power run mode

Available peripherals

- GPIO
- DMA
- FSMC
- QUADSPI
- BOR
- PVD, PVM
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
- SPI
- CAN
- SDMMC
- SWPMI
- SAI
- DFSDM
- ADC
- DAC
- OPAMP
- COMP
- Temp Sensor
- Timers
- LPTIM 1
- LPTIM 2
- IWDG
- WWDG
- Systick Timer
- Touch Sens
- RNG
- AES
- CRC

Available clocks

- HSI16
- HSE
- LSI
- LSE
- MSI

Ex: Execution from Flash memory

Cortex M4

Flash memory (1 Mbyte)

SRAM 1 (96 Kbytes)

SRAM 2 (32 Kbytes)

Main regulator (MR)

Range 1 (up to 80 MHz)

Range 2 (up to 26 MHz)

Low-power regulator (LPR) up to 2 MHz

from Flash
135 µA/MHz at 2 MHz
(269 µA)

From SRAM1
112 µA/MHz at 2 MHz
(225 µA)

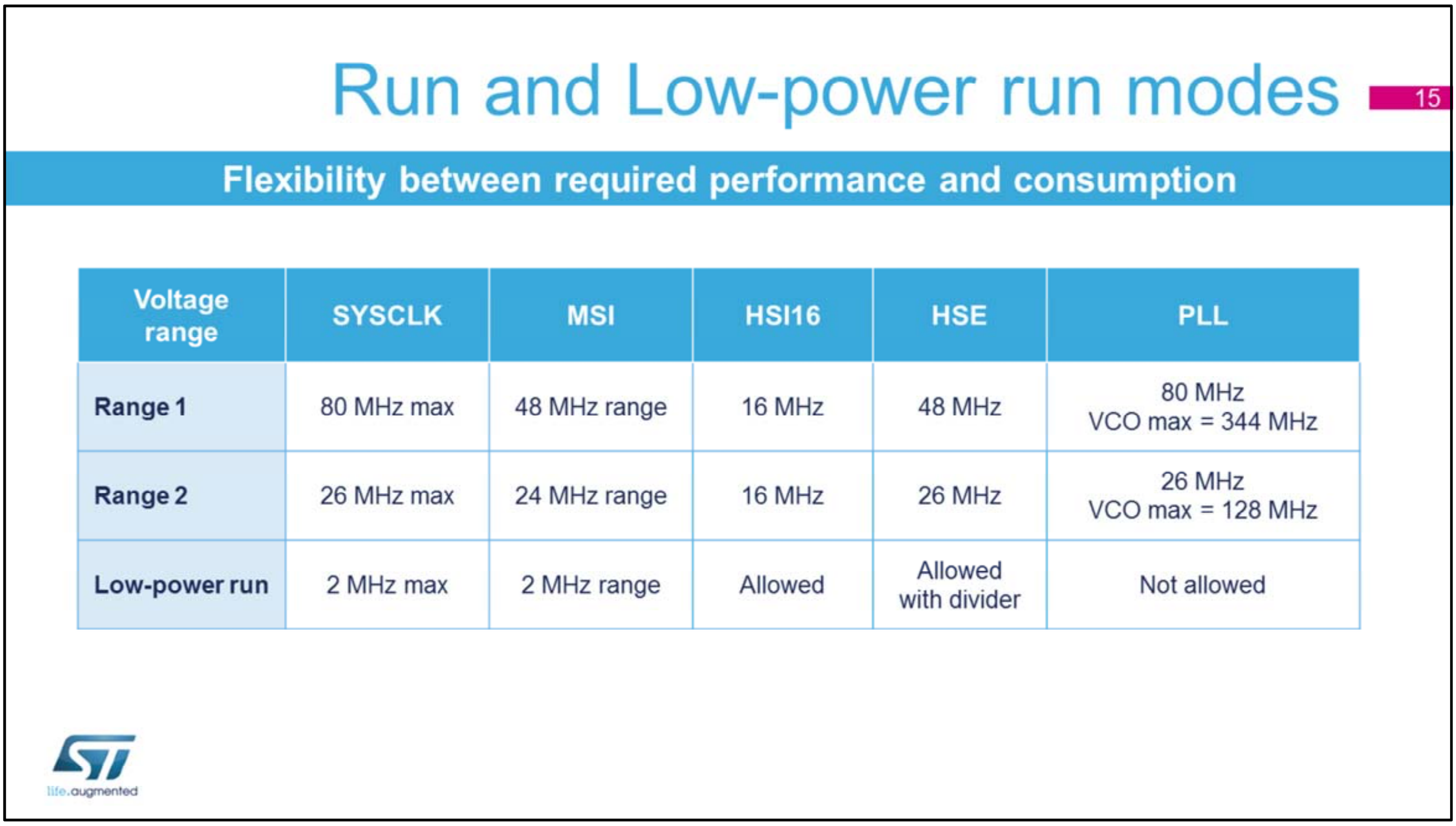
Active cell | Clocked-off cell | Cell in power-down | Available Periph and clock

In Low-power run mode, the main regulator is OFF and the low-power regulator supplies the logic allowing a system clock up to 2 MHz. When executing from SRAM, the Flash consumption can be reduced by configuring the Flash memory in Power-down mode and by gating its clock off.

All peripherals can be activated except the USB OTG and Random Number Generator. All clocks can be enabled. At 2 MHz, there is no limitation regarding the number of peripherals that can be activated.

The Low-power run mode consumption is 135 µA/MHz at 2 MHz when executing from Flash memory with the ART accelerator enabled. It is 112 µA/MHz at 2 MHz when executing from SRAM1.

The I2C, USART, LPUART and SWPMI clocks can be based on the internal high-speed oscillator at 16 MHz.

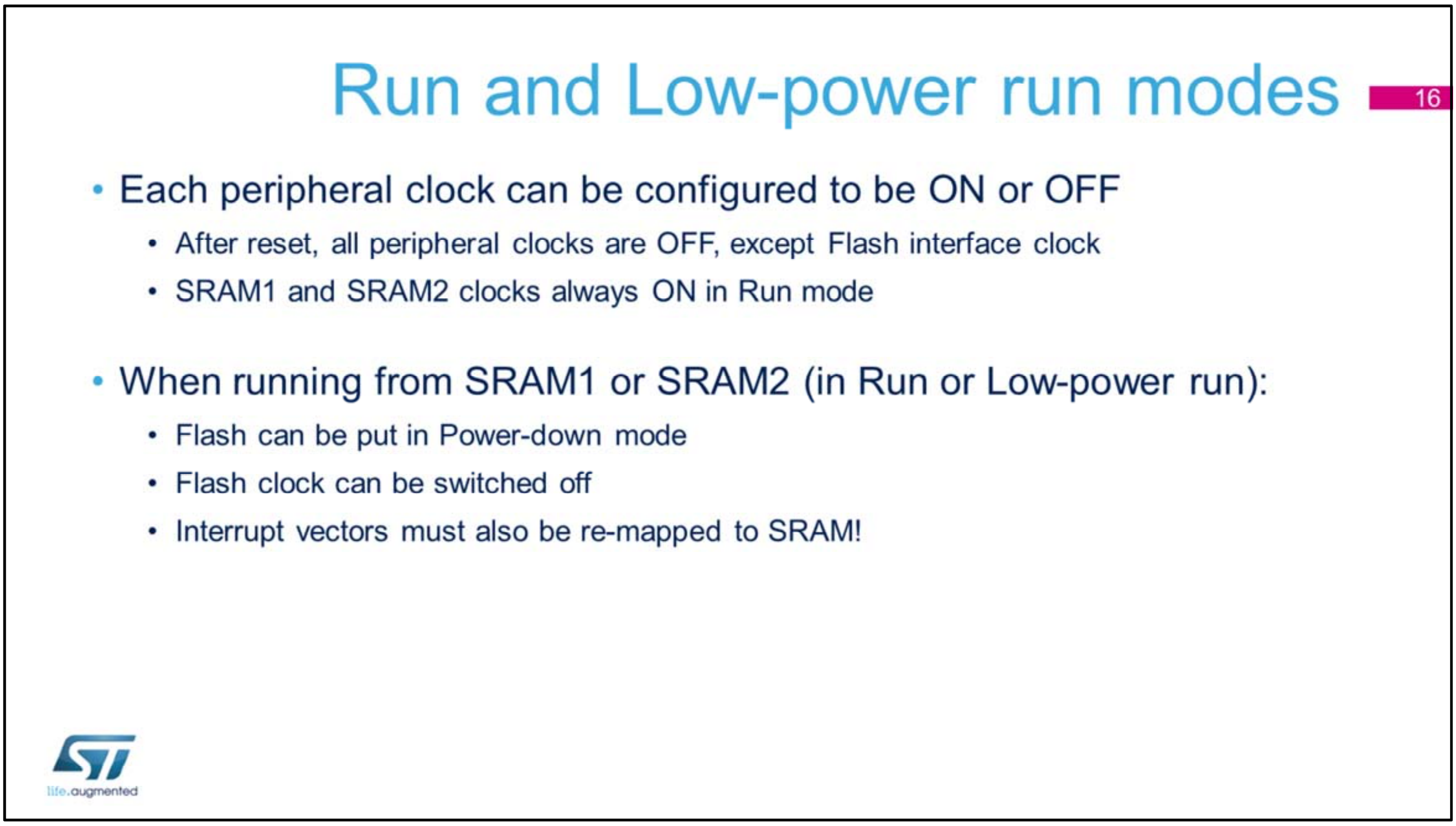


Run and Low-power run modes

Flexibility between required performance and consumption

Voltage range	SYSCLK	MSI	HSI16	HSE	PLL
Range 1	80 MHz max	48 MHz range	16 MHz	48 MHz	80 MHz VCO max = 344 MHz
Range 2	26 MHz max	24 MHz range	16 MHz	26 MHz	26 MHz VCO max = 128 MHz
Low-power run	2 MHz max	2 MHz range	Allowed	Allowed with divider	Not allowed

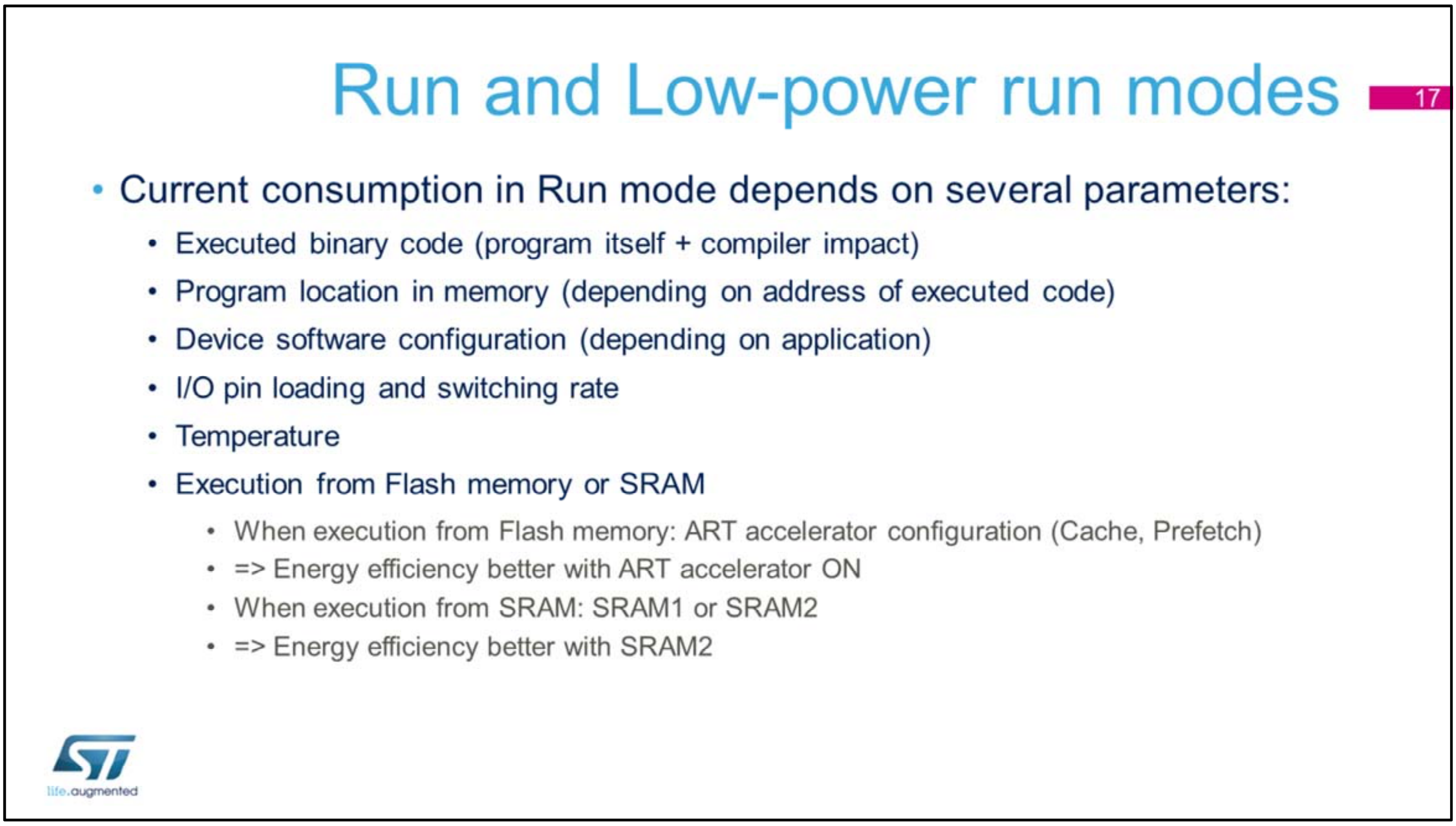
The Run mode, thanks to voltage scaling, and the Low-power run modes offer flexibility between required performance and consumption.
In Run mode range 1, the system clock is limited to 80 MHz and the internal and external oscillators and the PLL can be used. In Run mode range 2, the system clock is limited to 26 MHz and the internal and external oscillators as well as the PLL can be used, but must be limited to 26 MHz. In Low-power run mode, the system clock must be limited to 2 MHz.



Run and Low-power run modes

- Each peripheral clock can be configured to be ON or OFF
  - After reset, all peripheral clocks are OFF, except Flash interface clock
  - SRAM1 and SRAM2 clocks always ON in Run mode
- When running from SRAM1 or SRAM2 (in Run or Low-power run):
  - Flash can be put in Power-down mode
  - Flash clock can be switched off
  - Interrupt vectors must also be re-mapped to SRAM!

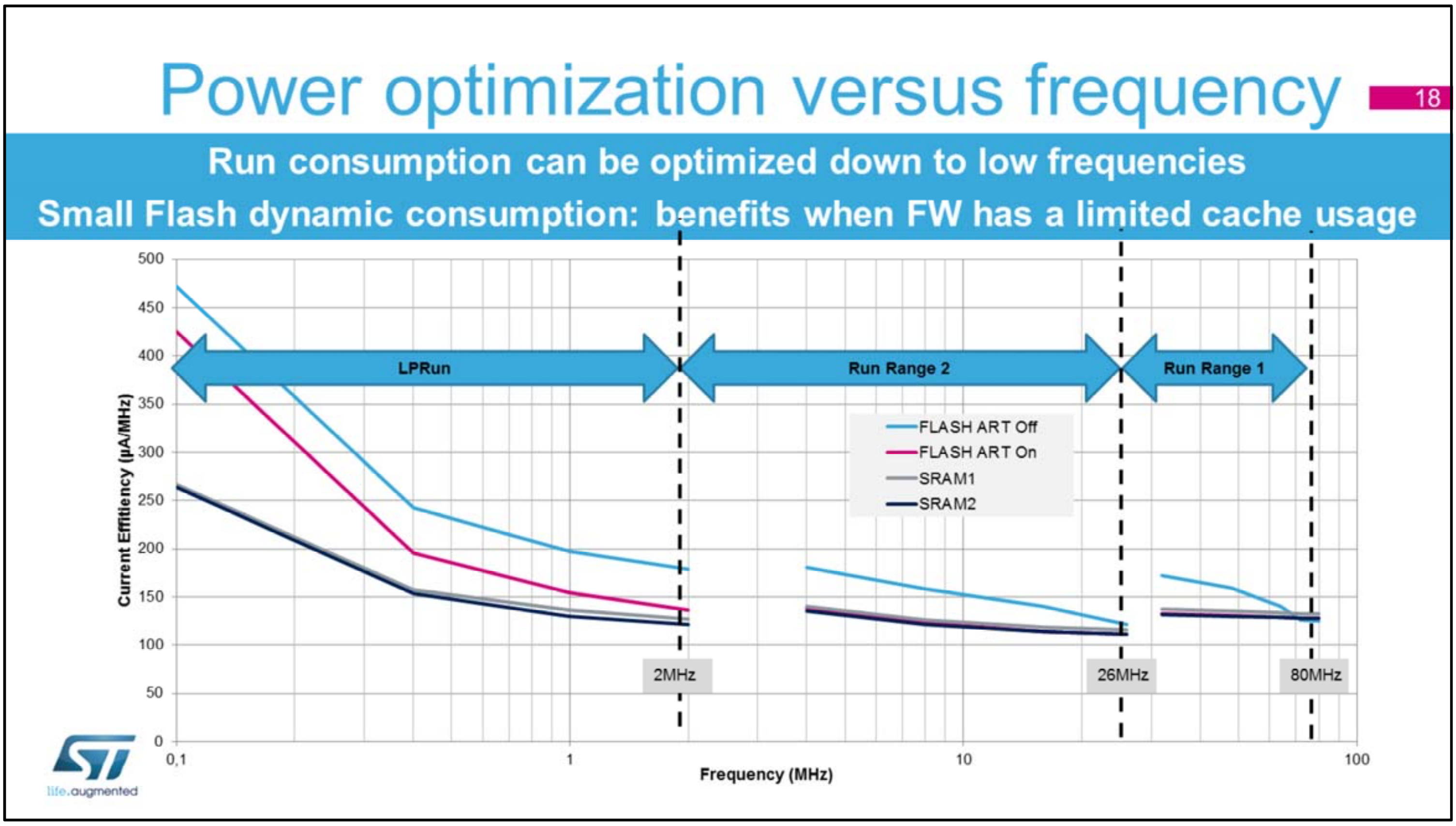
Each peripheral clock can be configured to be ON or OFF in Run and Low-power run modes. By default all peripherals clocks are OFF, except the Flash interface clock. The SRAM1 and SRAM2 clocks are always ON in Run mode.
When running from SRAM1 or SRAM2 (in Run or Low-power run modes), the Flash memory can be put in Power-down mode thanks to software, and the Flash clock can be switched off. The Flash memory must not be accessed when it is switched off, consequently interrupts must be mapped in SRAM, using the Cortex-M4 Vector Table Offset Register.



Run and Low-power run modes

- Current consumption in Run mode depends on several parameters:
  - Executed binary code (program itself + compiler impact)
  - Program location in memory (depending on address of executed code)
  - Device software configuration (depending on application)
  - I/O pin loading and switching rate
  - Temperature
  - Execution from Flash memory or SRAM
    - When execution from Flash memory: ART accelerator configuration (Cache, Prefetch)
    - => Energy efficiency better with ART accelerator ON
    - When execution from SRAM: SRAM1 or SRAM2
    - => Energy efficiency better with SRAM2

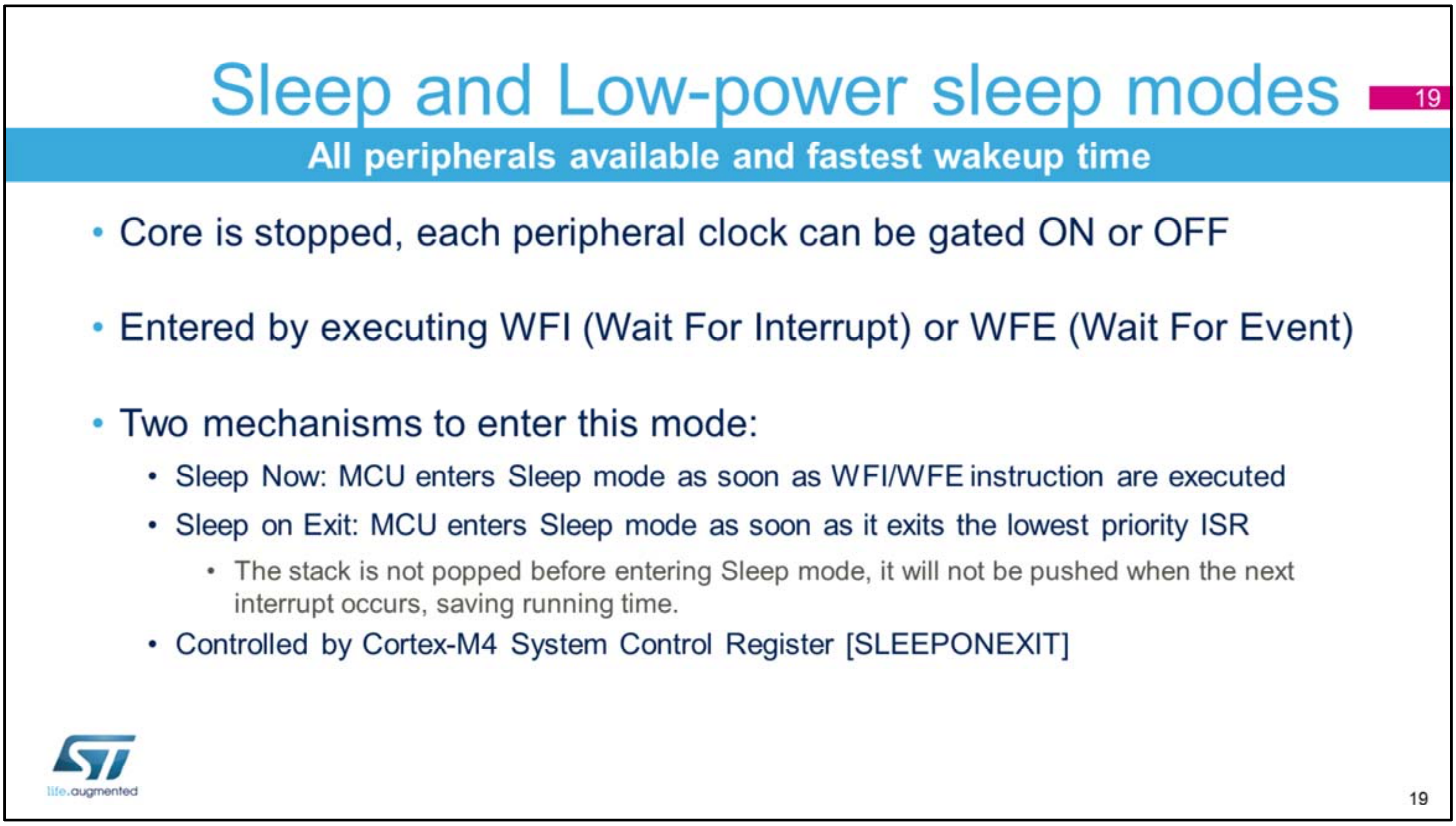
The current consumption in Run or Low-power run modes depends on several parameters: first the executed binary code, that means the program itself plus the compiler impact. Then it depends on the program location in the memory, the device software configuration, the I/O pin loading and switching rate, the temperature and so on…
The consumption also depends on if the code is executed from Flash memory or from SRAM. When code is executed from Flash, the Energy efficiency is better when the Flash accelerator is enable. When code is executed from SRAM, the Energy efficiency is better when executing from SRAM2.



Power optimization versus frequency

Run consumption can be optimized down to low frequencies
Small Flash dynamic consumption: benefits when FW has a limited cache usage

The consumption in Run mode can be optimized down to low frequency, thanks to Low-power run mode. Enabling the ART accelerator increases performance but also reduces the dynamic consumption. Best consumption is most often reached when the Instruction Cache is ON, Data Cache is ON and Prefetch buffer is OFF, as this configuration reduces the number of Flash memory accesses.
The small Flash dynamic consumption allows a small consumption each time the firmware needs to access the Flash memory.
Consumptions from SRAM1 and SRAM2 are quite similar, but SRAM2 is much more power efficient than SRAM1, when not remapped at address 0, thanks to its 0 wait-state access.

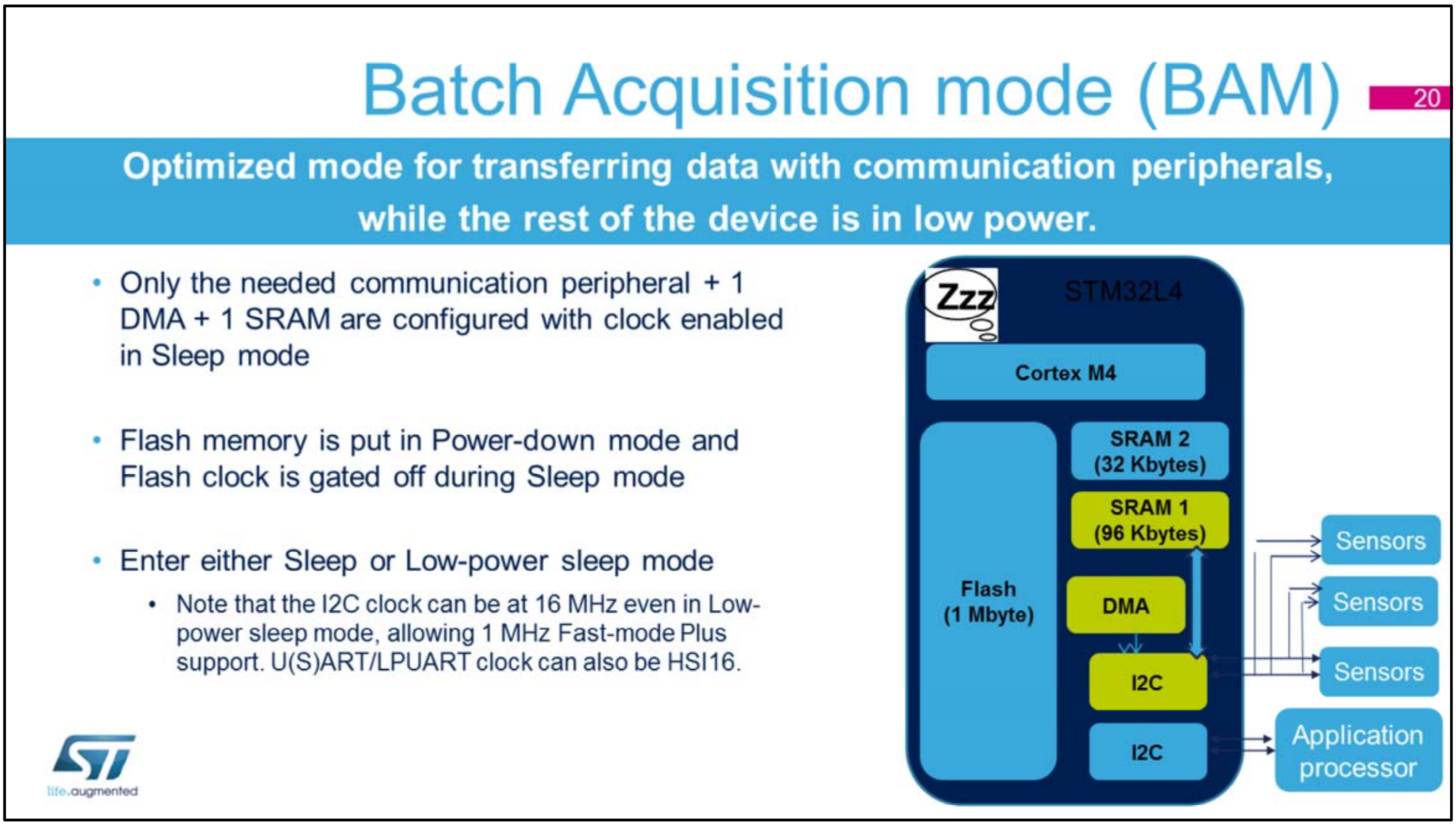


Sleep and Low-power sleep modes

All peripherals available and fastest wakeup time

- Core is stopped, each peripheral clock can be gated ON or OFF
- Entered by executing WFI (Wait For Interrupt) or WFE (Wait For Event)
- Two mechanisms to enter this mode:
  - Sleep Now: MCU enters Sleep mode as soon as WFI/WFE instruction are executed
  - Sleep on Exit: MCU enters Sleep mode as soon as it exits the lowest priority ISR
    - The stack is not popped before entering Sleep mode, it will not be pushed when the next interrupt occurs, saving running time.
  - Controlled by Cortex-M4 System Control Register [SLEEPONEXIT]

Sleep and Low-power sleep modes allows all peripherals to be used and features the fastest wakeup time.
In these modes, the CPU is stopped and each peripheral clock can be configured by software to be gated ON or OFF during the Sleep and Low-power sleep modes.
These modes are entered by executing the assembler instruction Wait for Interrupt or Wait for Event. When executed in Low-power run mode, the device enters Low-power sleep mode.
Depending on the SLEEPONEXIT bit configuration in the CortexM4 System Control Register, the MCU enters Sleep mode as soon as the instruction is executed, or as soon as it exits the lowest priority Interrupt Sub Routine.
This last configuration allows to save time and consumption by saving the need to pop and push the stack.

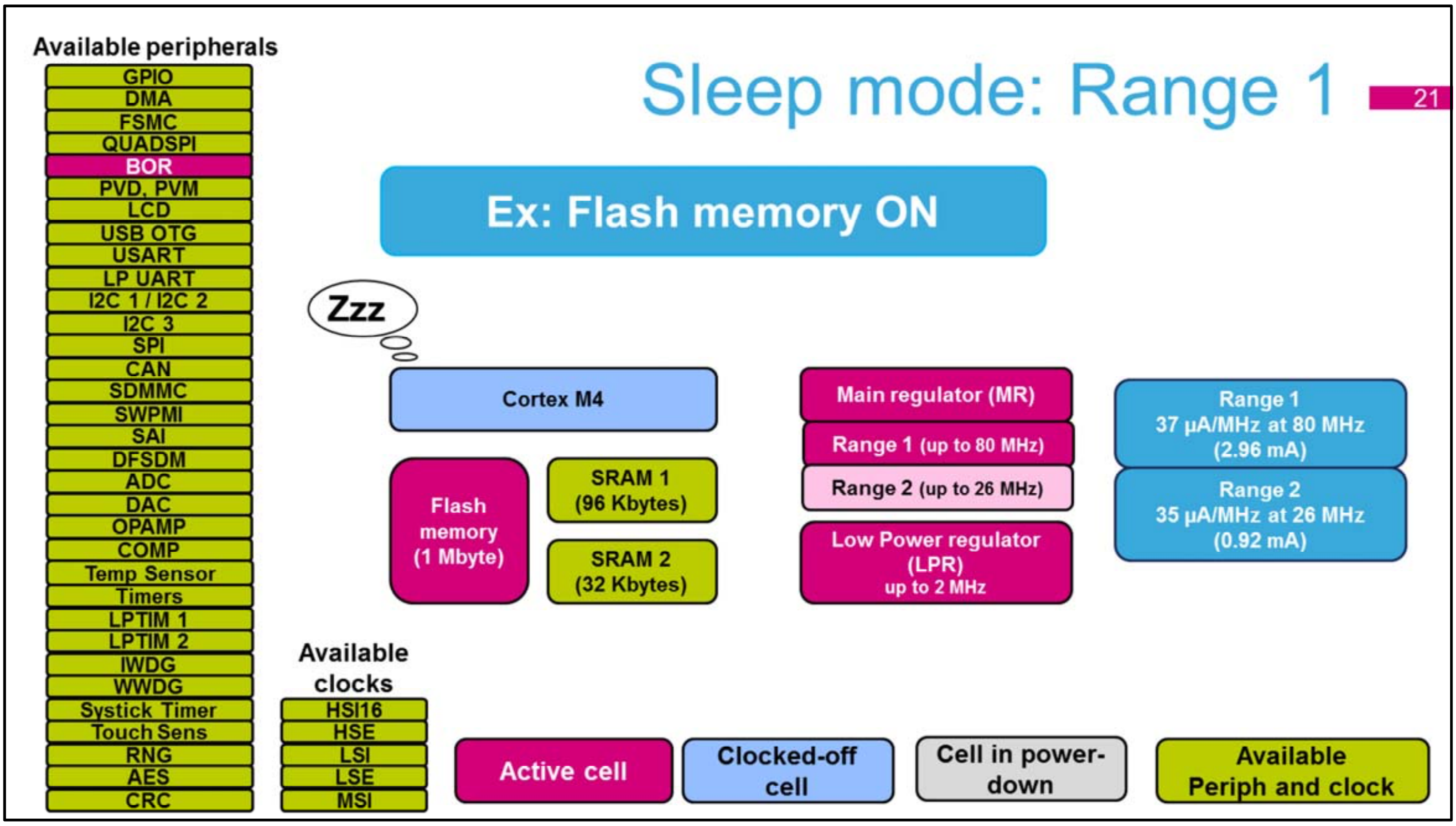


Batch Acquisition mode (BAM)

Optimized mode for transferring data with communication peripherals, while the rest of the device is in low power.

- Only the needed communication peripheral + 1 DMA + 1 SRAM are configured with clock enabled in Sleep mode
- Flash memory is put in Power-down mode and Flash clock is gated off during Sleep mode
- Enter either Sleep or Low-power sleep mode
  - Note that the I2C clock can be at 16 MHz even in Low-power sleep mode, allowing 1 MHz Fast-mode Plus support. U(S)ART/LPUART clock can also be HSI16.

Batch Acquisition Mode is an optimized mode for transferring data.
Only the needed communication peripheral + 1 DMA + SRAM1 or SRAM2 are configured with clock enable in Sleep mode.
Flash memory is put in Power-down mode and the Flash memory clock is gated off during Sleep mode.
Then it can enter either Sleep or Low-power sleep mode.
Note that the I2C clock can be at 16 MHz even in Low-power sleep mode, allowing support for 1-MHz Fast-mode Plus. The USART and LPUART clocks can also be based on the high-speed internal oscillator. Typical applications are sensor hubs.



Sleep mode: Range 1

Ex: Flash memory ON

Available peripherals

GPIO
DMA
FSMC
QUADSPI
BOR
PVD, PVM
LCD
USB OTG
USART
LP UART
I2C 1 / I2C 2
I2C 3
SPI
CAN
SDMMC
SWPMI
SAI
DFSDM
ADC
DAC
OPAMP
COMP
Temp Sensor
Timers
LPTIM 1
LPTIM 2
IWDG
WWDG
Systick Timer
Touch Sens
RNG
AES
CRC

Available clocks

HSI16
HSE
LSI
LSE
MSI

Zzz

Cortex M4

Flash memory (1 Mbyte)

SRAM 1 (96 Kbytes)

SRAM 2 (32 Kbytes)

Main regulator (MR)

Range 1 (up to 80 MHz)

Range 2 (up to 26 MHz)

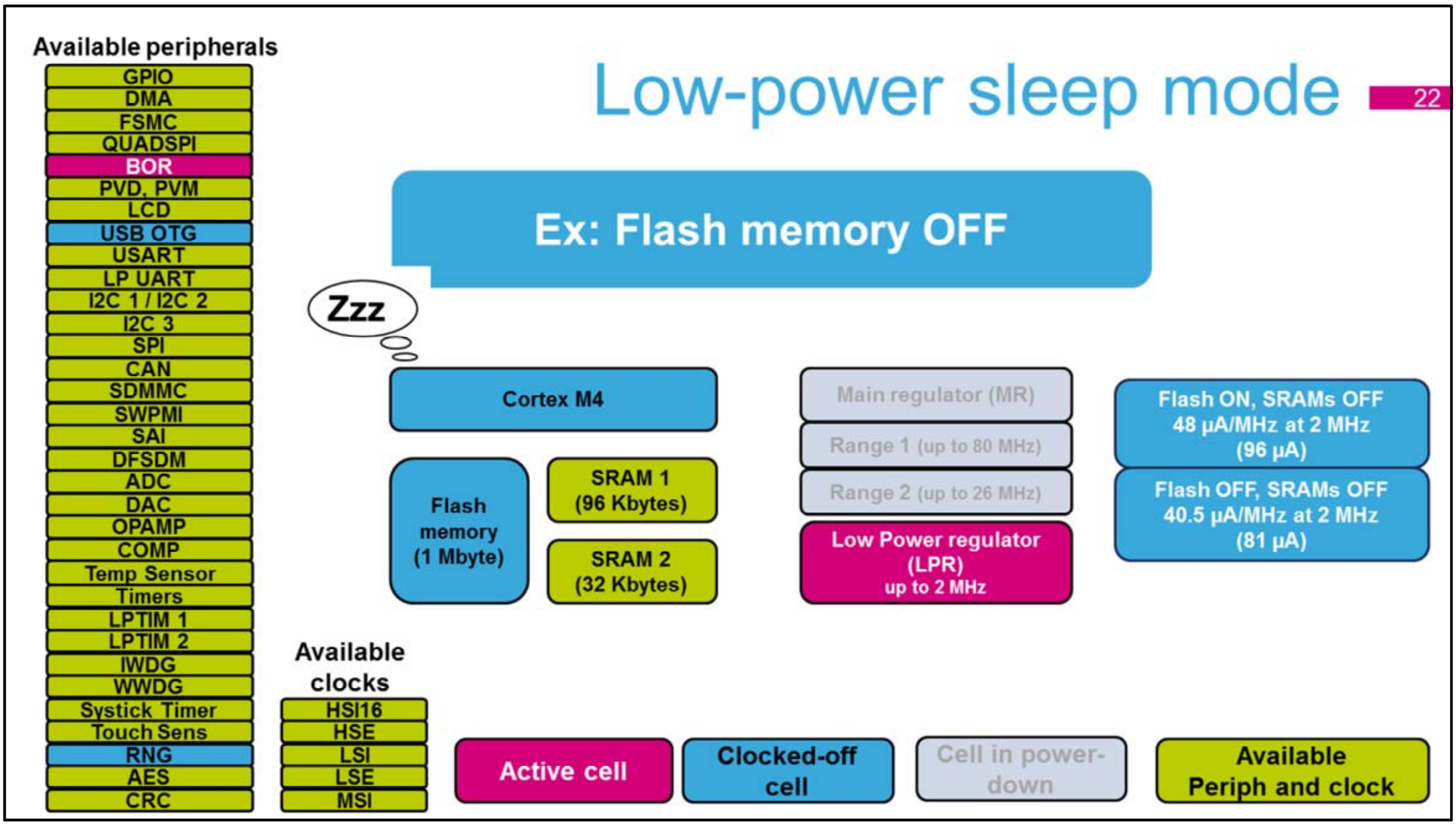
Low Power regulator (LPR) up to 2 MHz

Range 1
37 µA/MHz at 80 MHz
(2.96 mA)

Range 2
35 µA/MHz at 26 MHz
(0.92 mA)

Active cell | Clocked-off cell | Cell in power-down | Available Periph and clock

In Sleep mode, the CPU clocks are OFF. In Range 1, the system clock is up to 80 MHz, in Range 2 it is up to 26 MHz. By default, the SRAM1 and SRAM2 clocks are enabled. They can be gated off during Sleep mode by software.
All peripherals can be activated in Range 1. In Range 2, all peripherals can be activated except the USB OTG and Random Number Generator.
The Sleep mode consumption is 37 µA/MHz in Range 1 at 80 MHz with the Flash memory ON.



Low-power sleep mode

22

Ex: Flash memory OFF

Available peripherals

GPIO
DMA
FSMC
QUADSPI
BOR
PVD, PVM
LCD
USB OTG
USART
LP UART
I2C 1 / I2C 2
I2C 3
SPI
CAN
SDMMC
SWPMI
SAI
DFSDM
ADC
DAC
OPAMP
COMP
Temp Sensor
Timers
LPTIM 1
LPTIM 2
IWDG
WWDG
Systick Timer
Touch Sens
RNG
AES
CRC

Zzz

Cortex M4

Flash memory (1 Mbyte)

SRAM 1 (96 Kbytes)

SRAM 2 (32 Kbytes)

Main regulator (MR)

Range 1 (up to 80 MHz)

Range 2 (up to 26 MHz)

Low Power regulator (LPR) up to 2 MHz

Flash ON, SRAMs OFF
48 µA/MHz at 2 MHz
(96 µA)

Flash OFF, SRAMs OFF
40.5 µA/MHz at 2 MHz
(81 µA)

Available clocks

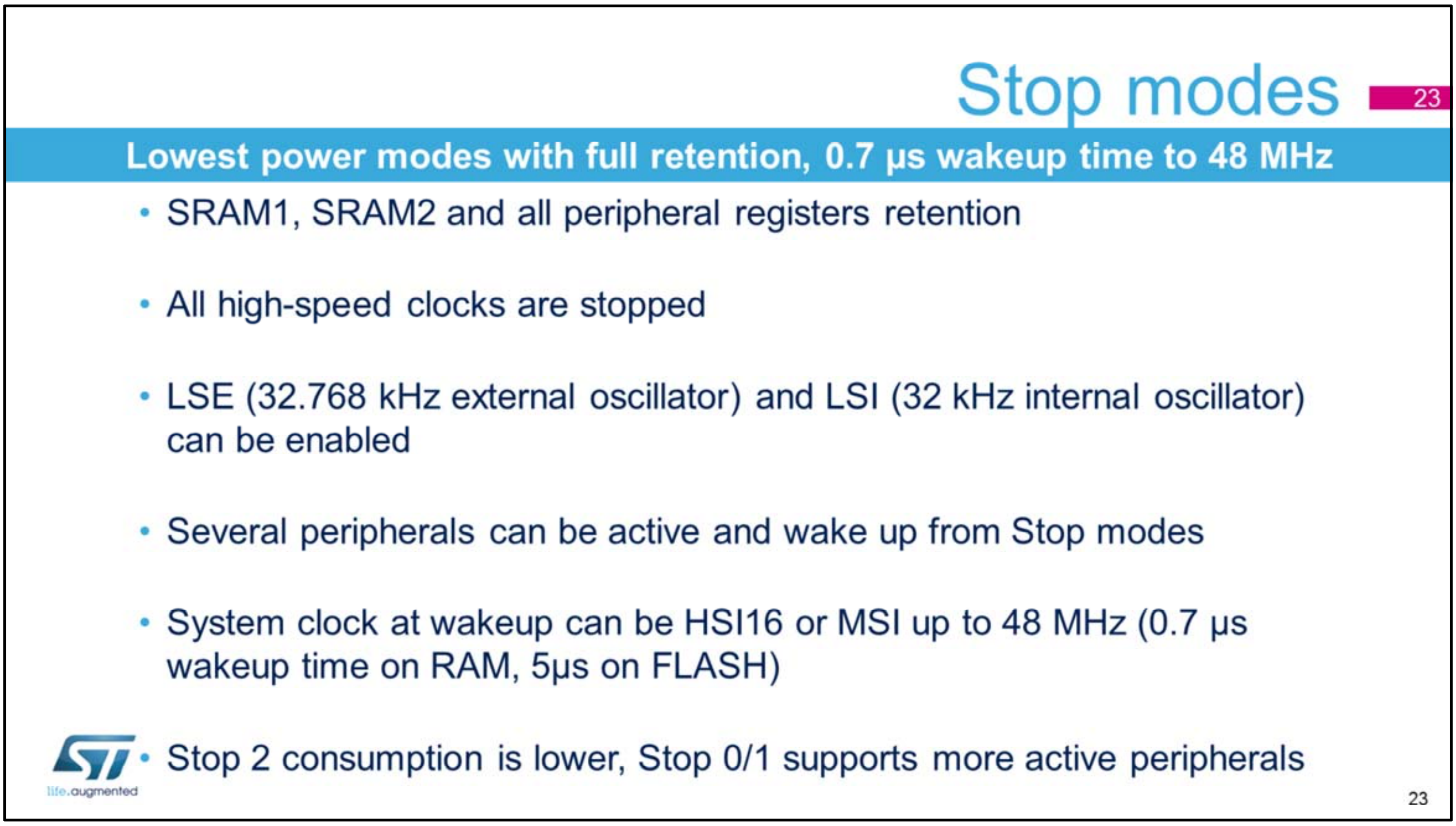
HSI16
HSE
LSI
LSE
MSI

Active cell | Clocked-off cell | Cell in power-down | Available Periph and clock

In Low-power sleep mode, the CPU clocks are OFF and the logic is supplied by the low-power regulator. The system clock is up to 2 MHz. Flash memory can be configured in Power down and can be gated off; SRAM1 and SRAM2 can be gated off.

All peripherals can be activated except the USB OTG and Random Number Generator.

The Low-power sleep mode consumption is 40 µA/MHz at 2 MHz with Flash memory and SRAM OFF.

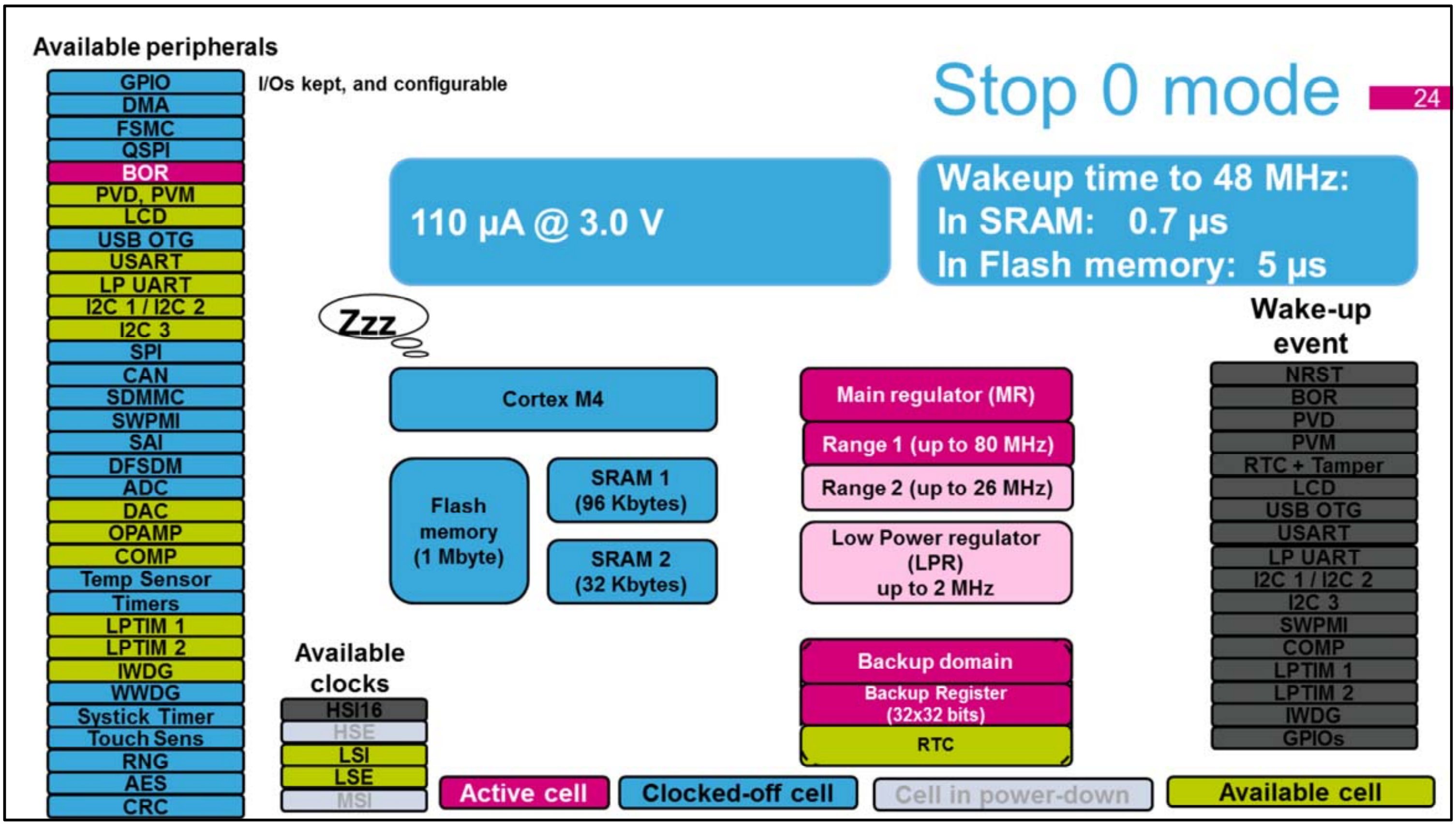


Stop modes

Lowest power modes with full retention, 0.7 µs wakeup time to 48 MHz

- SRAM1, SRAM2 and all peripheral registers retention
- All high-speed clocks are stopped
- LSE (32.768 kHz external oscillator) and LSI (32 kHz internal oscillator) can be enabled
- Several peripherals can be active and wake up from Stop modes
- System clock at wakeup can be HSI16 or MSI up to 48 MHz (0.7 µs wakeup time on RAM, 5µs on FLASH)
- Stop 2 consumption is lower, Stop 0/1 supports more active peripherals

STM32L4 devices features three Stop modes: Stop 0, 1 and 2, which are the lowest power modes with full retention and only a 0.7-µs wakeup time to Run mode at 48 MHz.
The contents of SRAM1, SRAM2 and all peripherals registers are preserved in Stop modes.
All high speed clocks are stopped.
The 32.768 kHz external oscillator and 32 kHz internal oscillator can be enabled.
Several peripherals can be active and wake up from Stop mode.
System clock on wake-up can be the internal high-speed and multi-speed oscillators up to 48 MHz with only a 0.7µs wakeup time from RAM or 5µs from FLASH.
Stop 2 consumption is lower than Stop 1, but Stop 0 and 1 supports more active peripherals.



Stop 0 mode

24

Available peripherals

GPIO
DMA
FSMC
QSPI
BOR
PVD, PVM
LCD
USB OTG
USART
LP UART
I2C 1 / I2C 2
I2C 3
SPI
CAN
SDMMC
SWPMI
SAI
DFSDM
ADC
DAC
OPAMP
COMP
Temp Sensor
Timers
LPTIM 1
LPTIM 2
IWDG
WWDG
Systick Timer
Touch Sens
RNG
AES
CRC

I/Os kept, and configurable

110 µA @ 3.0 V

Wakeup time to 48 MHz:
In SRAM: 0.7 µs
In Flash memory: 5 µs

Zzz

Cortex M4

Flash memory (1 Mbyte)

SRAM 1 (96 Kbytes)

SRAM 2 (32 Kbytes)

Main regulator (MR)
Range 1 (up to 80 MHz)
Range 2 (up to 26 MHz)

Low Power regulator (LPR) up to 2 MHz

Backup domain
Backup Register (32x32 bits)
RTC

Available clocks

HSI16
HSE
LSI
LSE
MSI

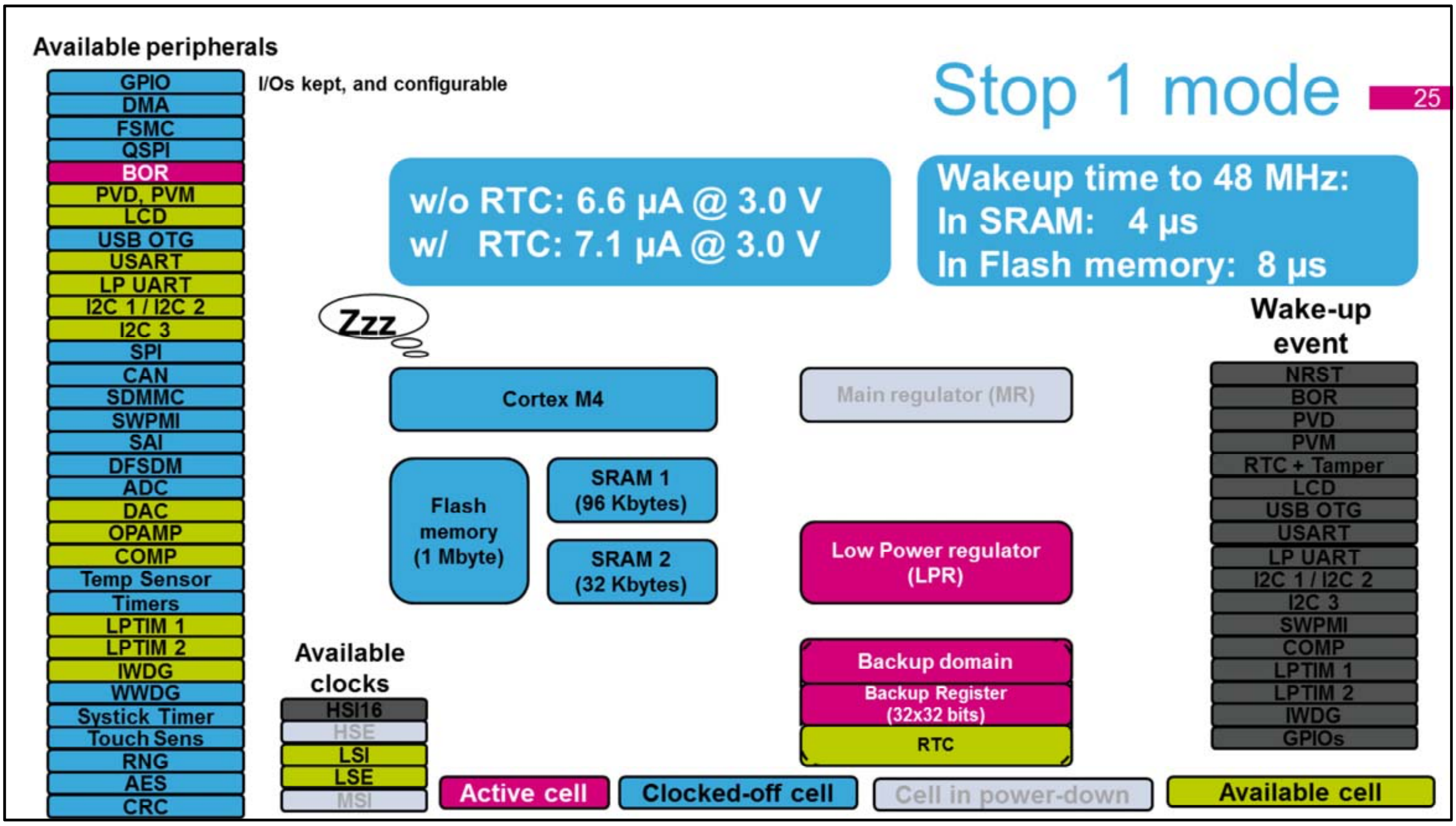
Wake-up event

NRST
BOR
PVD
PVM
RTC + Tamper
LCD
USB OTG
USART
LP UART
I2C 1 / I2C 2
I2C 3
SWPMI
COMP
LPTIM 1
LPTIM 2
IWDG
GPIOs

Active cell
Clocked-off cell
Cell in power-down
Available cell

In Stop 0 mode, the system clock is frozen and all high-speed clocks are powered down. The RTC, clocked by the internal or external low-speed oscillator, can be activated.
The brown-out reset is always enabled. Most of the peripheral clocks are gated off. Several peripherals can be functional in Stop 0 mode: Power voltage detector, peripherals voltage monitor, LCD controller, digital to analog converters, operational amplifiers, comparators, independent watchdog, low power timers, I2C, UART and low-power UART.
The events from all I/Os can wake up from Stop 0 mode, plus the interrupt generated by the active peripherals. In addition, SWPMI and USB can wake up from Stop 0 mode. The I2C and UART or LPUART can switch the HSI16 ON during the Stop mode in order to recognize their wakeup condition.

The Stop 0 mode consumption is 110 µA typical at 3V. The wakeup time is 0.7 µs when the system clock at wakeup is MSI at 48 MHz, and the code is executed from SRAM.



Stop 1 mode

Available peripherals

I/Os kept, and configurable

- GPIO
- DMA
- FSMC
- QSPI
- BOR
- PVD, PVM
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
- SPI
- CAN
- SDMMC
- SWPMI
- SAI
- DFSDM
- ADC
- DAC
- OPAMP
- COMP
- Temp Sensor
- Timers
- LPTIM 1
- LPTIM 2
- IWDG
- WWDG
- Systick Timer
- Touch Sens
- RNG
- AES
- CRC

w/o RTC: 6.6 µA @ 3.0 V
w/ RTC: 7.1 µA @ 3.0 V

Wakeup time to 48 MHz:
In SRAM: 4 µs
In Flash memory: 8 µs

Available clocks

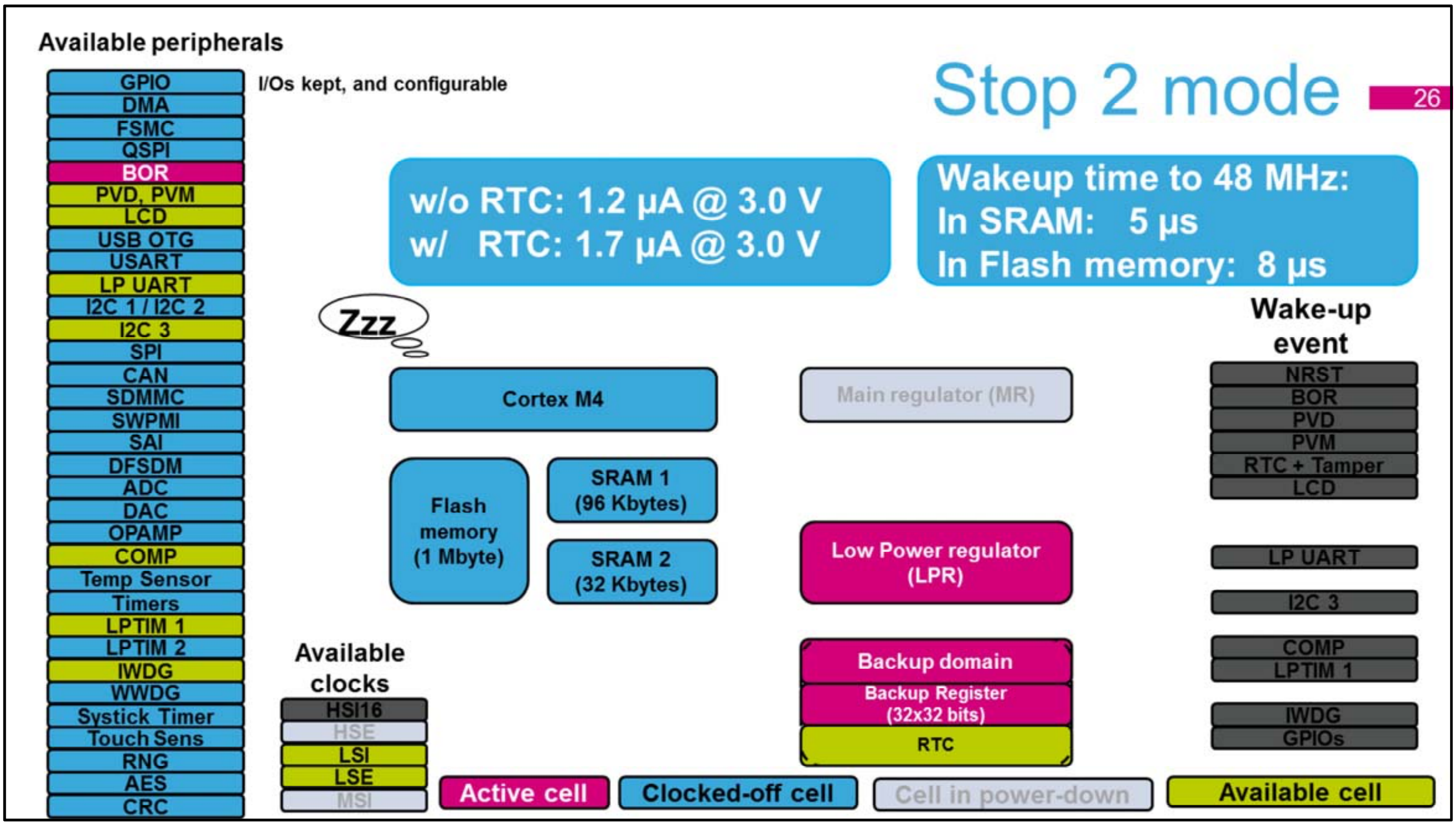
- HSI16
- HSE
- LSI
- LSE
- MSI

Wake-up event

- NRST
- BOR
- PVD
- PVM
- RTC + Tamper
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
- SWPMI
- COMP
- LPTIM 1
- LPTIM 2
- IWDG
- GPIOs

Active cell | Clocked-off cell | Cell in power-down | Available cell

Stop 1 mode is very similar to Stop 0 except that the power figures are much lower as the main regulator is stopped and replaced by the low Power Regulator.
The Stop 1 mode consumption without RTC is 6.6 µA typical at 3V.
The wakeup time is 4 µs when the system clock at wakeup is MSI at 48 MHz, and the code is executed from SRAM.



Stop 2 mode

w/o RTC: 1.2 µA @ 3.0 V
w/ RTC: 1.7 µA @ 3.0 V

Wakeup time to 48 MHz:
In SRAM: 5 µs
In Flash memory: 8 µs

Available peripherals

I/Os kept, and configurable

- GPIO
- DMA
- FSMC
- QSPI
- BOR
- PVD, PVM
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
- SPI
- CAN
- SDMMC
- SWPMI
- SAI
- DFSDM
- ADC
- DAC
- OPAMP
- COMP
- Temp Sensor
- Timers
- LPTIM 1
- LPTIM 2
- IWDG
- WWDG
- Systick Timer
- Touch Sens
- RNG
- AES
- CRC

Available clocks

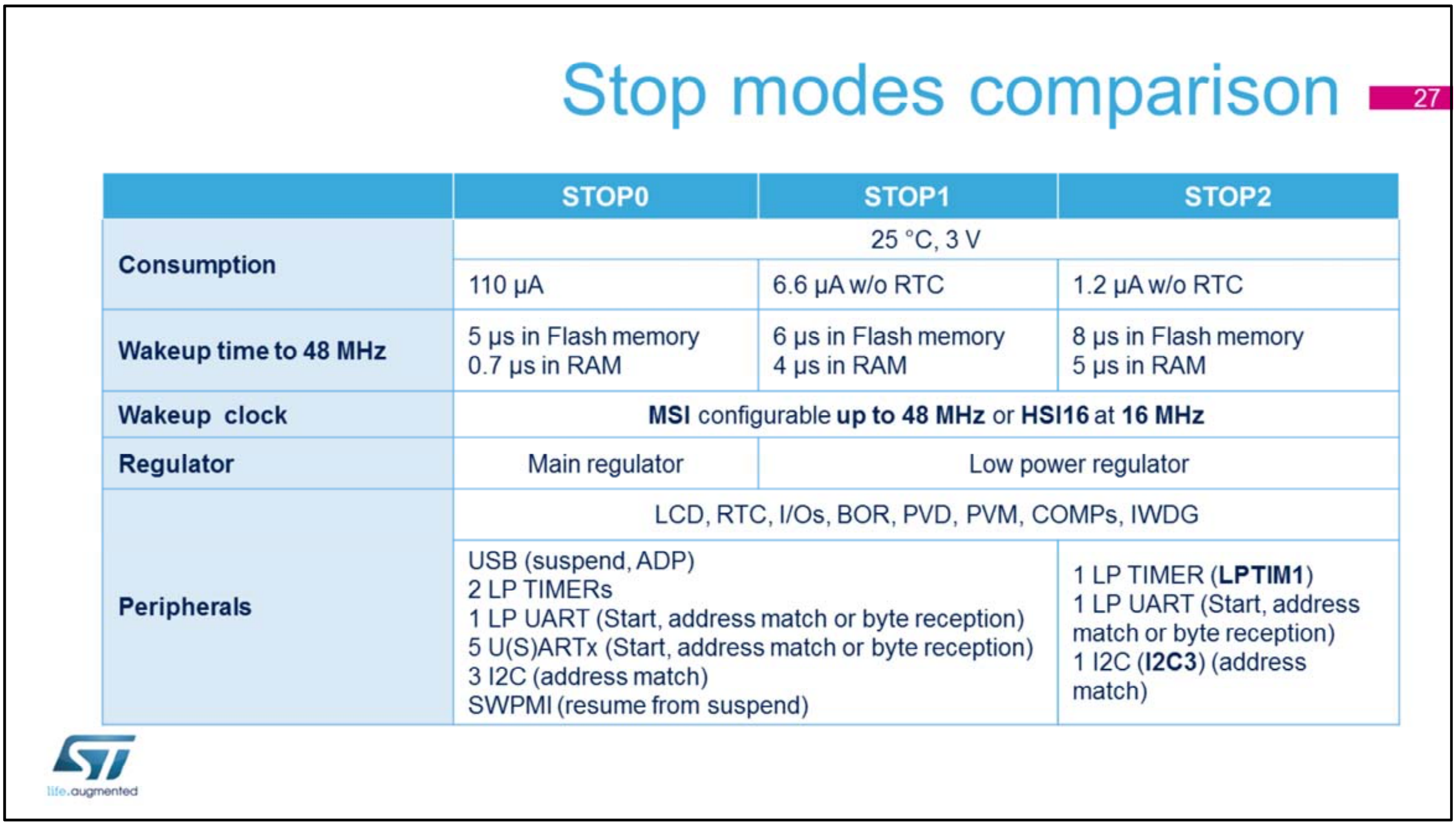
- HSI16
- HSE
- LSI
- LSE
- MSI

Wake-up event

- NRST
- BOR
- PVD
- PVM
- RTC + Tamper
- LCD
- LP UART
- I2C 3
- COMP
- LPTIM 1
- IWDG
- GPIOs

In Stop 2 mode, the system clock is frozen and all high-speed clocks are powered down. The RTC, clocked by the internal or external low-speed oscillator, can be activated.
The brown-out reset is always enabled. Most of the peripheral clocks are gated off. Several peripherals can be functional in Stop 2 mode: power voltage detector, peripheral voltage monitors, LCD controller, comparators, independent watchdog, low power timer 1, I2C3, and the low-power UART.
The events from all I/Os can wake up from Stop 2 mode, plus the interrupt generated by the active peripherals.
The I2C3 and LPUART can switch the HSI16 ON during Stop mode in order to recognize their wakeup condition.
The consumption in Stop 2 mode without the RTC is 1.2 µA typical at 3 V. The wakeup time is 5 µs when the system clock at wakeup is MSI at 48 MHz, and the code

is executed from SRAM.



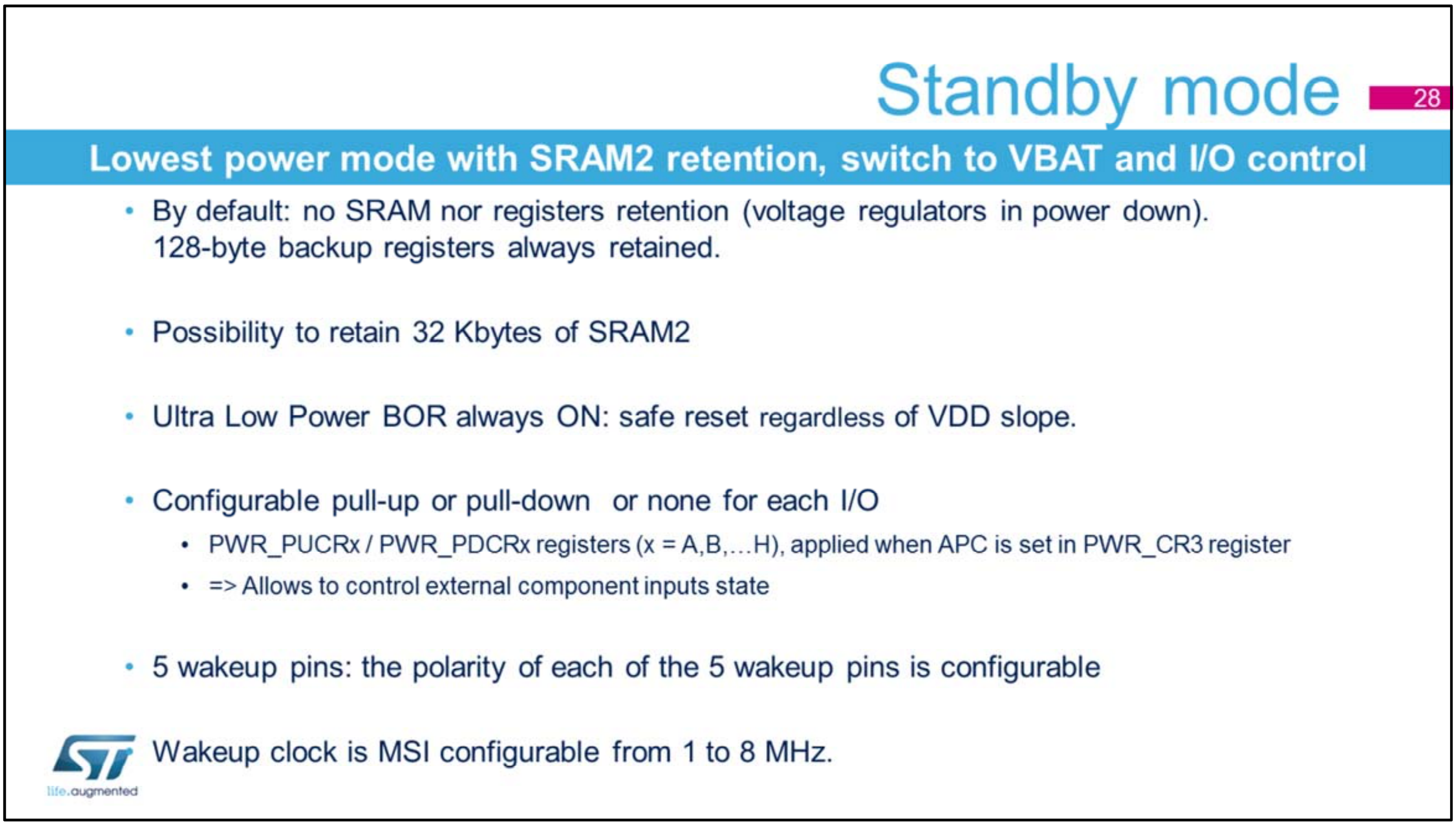
Stop modes comparison

	STOP0	STOP1	STOP2
Consumption	25 °C, 3 V		
	110 µA	6.6 µA w/o RTC	1.2 µA w/o RTC
Wakeup time to 48 MHz	5 µs in Flash memory 0.7 µs in RAM	6 µs in Flash memory 4 µs in RAM	8 µs in Flash memory 5 µs in RAM
Wakeup clock	**MSI** configurable **up to 48 MHz** or **HSI16** at **16 MHz**		
Regulator	Main regulator	Low power regulator	
Peripherals	LCD, RTC, I/Os, BOR, PVD, PVM, COMPs, IWDG		
	USB (suspend, ADP) 2 LP TIMERs 1 LP UART (Start, address match or byte reception) 5 U(S)ARTx (Start, address match or byte reception) 3 I2C (address match) SWPMI (resume from suspend)		1 LP TIMER (**LPTIM1**) 1 LP UART (Start, address match or byte reception) 1 I2C (**I2C3**) (address match)

When comparing Stop modes:
Stop 1 mode consumption is higher than Stop 2 mode consumption, but the wakeup time is shorter and the number of active peripherals is higher.
Stop 0 mode keep the Main regulator enabled, allowing a very short wake-up time lower than 1µs when restarting from the RAM to the expense of a higher consumption than Stop 1.
It is possible to wake up from Stop 0 or 1 mode with the USB Resume from Suspend event or with Attach Detection, but it is not supported in Stop 2 mode. A SWPMI Resume from Suspend event can also wake up the MCU from Stop 0 or 1 mode, but not from Stop 2.
The I2C address recognition is functional in both Stop modes, and can generate a wakeup event in case of an address match. Only 1 I2C is supported in Stop 2 versus 3 I2Cs in other Stop.
The UART byte reception is functional in both Stop modes and can generate a wakeup event in case of Start detection or Byte reception or Address match event. Only the low-power UART is

supported in Stop 2 mode. In other Stop modes, all 5 UARTs and the low-power UART can generate a wakeup event.

When clocked by the internal or external low-speed oscillator, or when clocked by an external pin, the low-power timer can wake up the MCU with all its events. In Stop 0 or 1 mode, both low-power timers are supported whereas only LPTIM1 is supported in Stop 2 mode.



Standby mode

28

Lowest power mode with SRAM2 retention, switch to VBAT and I/O control

- By default: no SRAM nor registers retention (voltage regulators in power down). 128-byte backup registers always retained.
- Possibility to retain 32 Kbytes of SRAM2
- Ultra Low Power BOR always ON: safe reset regardless of VDD slope.
- Configurable pull-up or pull-down or none for each I/O
  - PWR_PUCRx / PWR_PDCRx registers (x = A,B,…H), applied when APC is set in PWR_CR3 register
  - => Allows to control external component inputs state
- 5 wakeup pins: the polarity of each of the 5 wakeup pins is configurable
- Wakeup clock is MSI configurable from 1 to 8 MHz.

The Standby mode is the lowest power mode in which 32 Kbytes of SRAM2 can be retained, the automatic switch from VDD to VBAT is supported and the I/Os level can be configured by independent pull-up and pull-down circuitry.

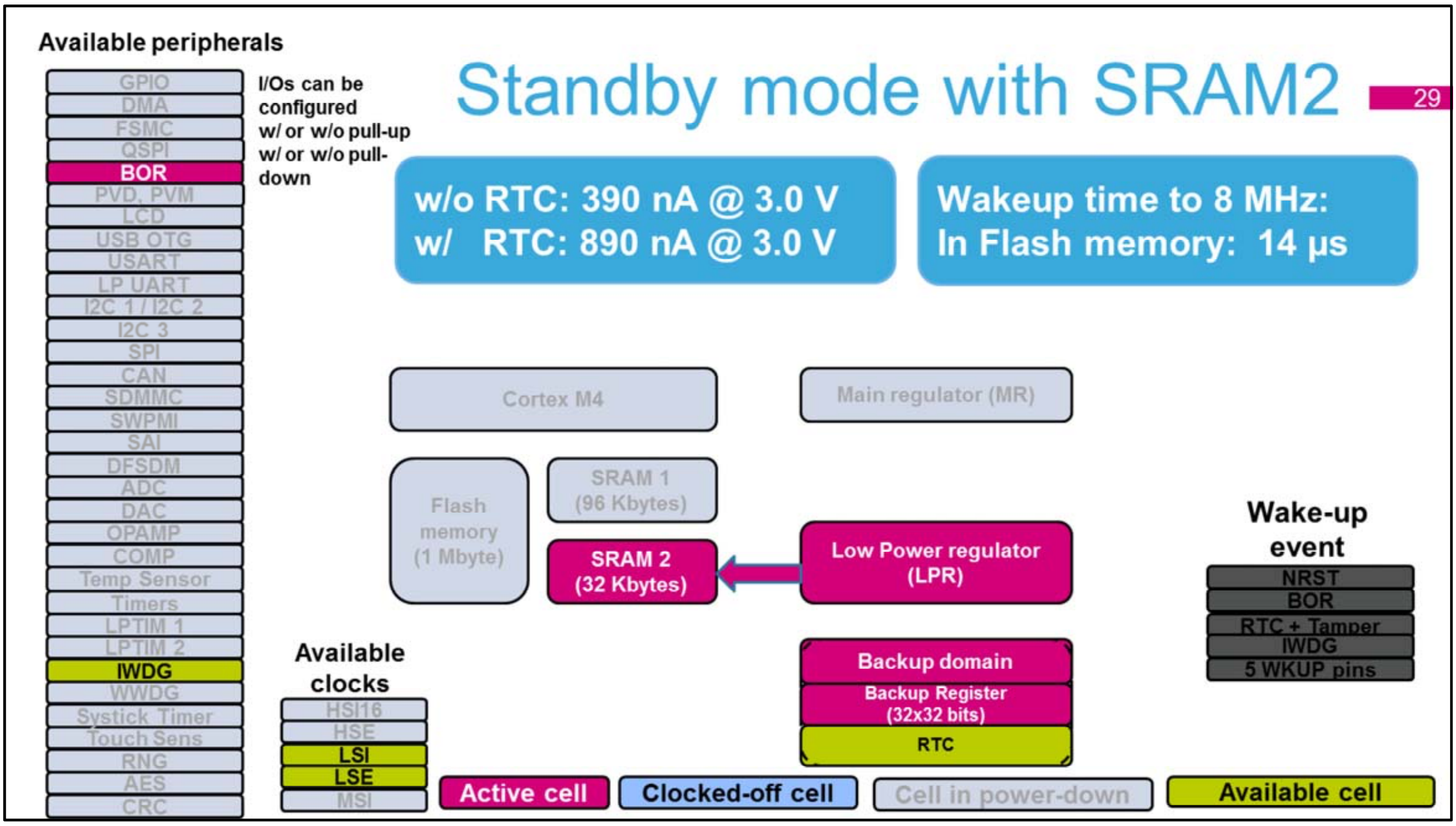
By default, the voltage regulators are in Power down mode and the SRAMs and the peripherals registers are lost. The 128-byte backup registers are always retained.

Thanks to software, it is possible to retain 32 Kbytes of SRAM2.

The ultra-low-power brown-out reset is always ON to ensure a safe reset regardless of the VDD slope.

Each I/O can be configured with or without a pull-up or pull-down, which is applied and released thanks to the APC control bit. This allows you to control the inputs state of external components even during Standby mode.

5 wakeup pins are available to wake up the device from Standby mode. The polarity of each of the 5 wakeup pins is configurable.
The wakeup clock is MSI with a frequency configurable from 1 to 8 MHz.



Standby mode with SRAM2

w/o RTC: 390 nA @ 3.0 V
w/ RTC: 890 nA @ 3.0 V

Wakeup time to 8 MHz:
In Flash memory: 14 µs

Available peripherals

- GPIO
- DMA
- FSMC
- QSPI
- BOR
- PVD, PVM
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
- SPI
- CAN
- SDMMC
- SWPMI
- SAI
- DFSDM
- ADC
- DAC
- OPAMP
- COMP
- Temp Sensor
- Timers
- LPTIM 1
- LPTIM 2
- IWDG
- WWDG
- Systick Timer
- Touch Sens
- RNG
- AES
- CRC

I/Os can be configured w/ or w/o pull-up w/ or w/o pull-down

Available clocks

- HSI16
- HSE
- LSI
- LSE
- MSI

Cortex M4

Main regulator (MR)

Flash memory (1 Mbyte)

SRAM 1 (96 Kbytes)

SRAM 2 (32 Kbytes)

Low Power regulator (LPR)

Backup domain
Backup Register (32x32 bits)
RTC

Wake-up event

- NRST
- BOR
- RTC + Tamper
- IWDG
- 5 WKUP pins

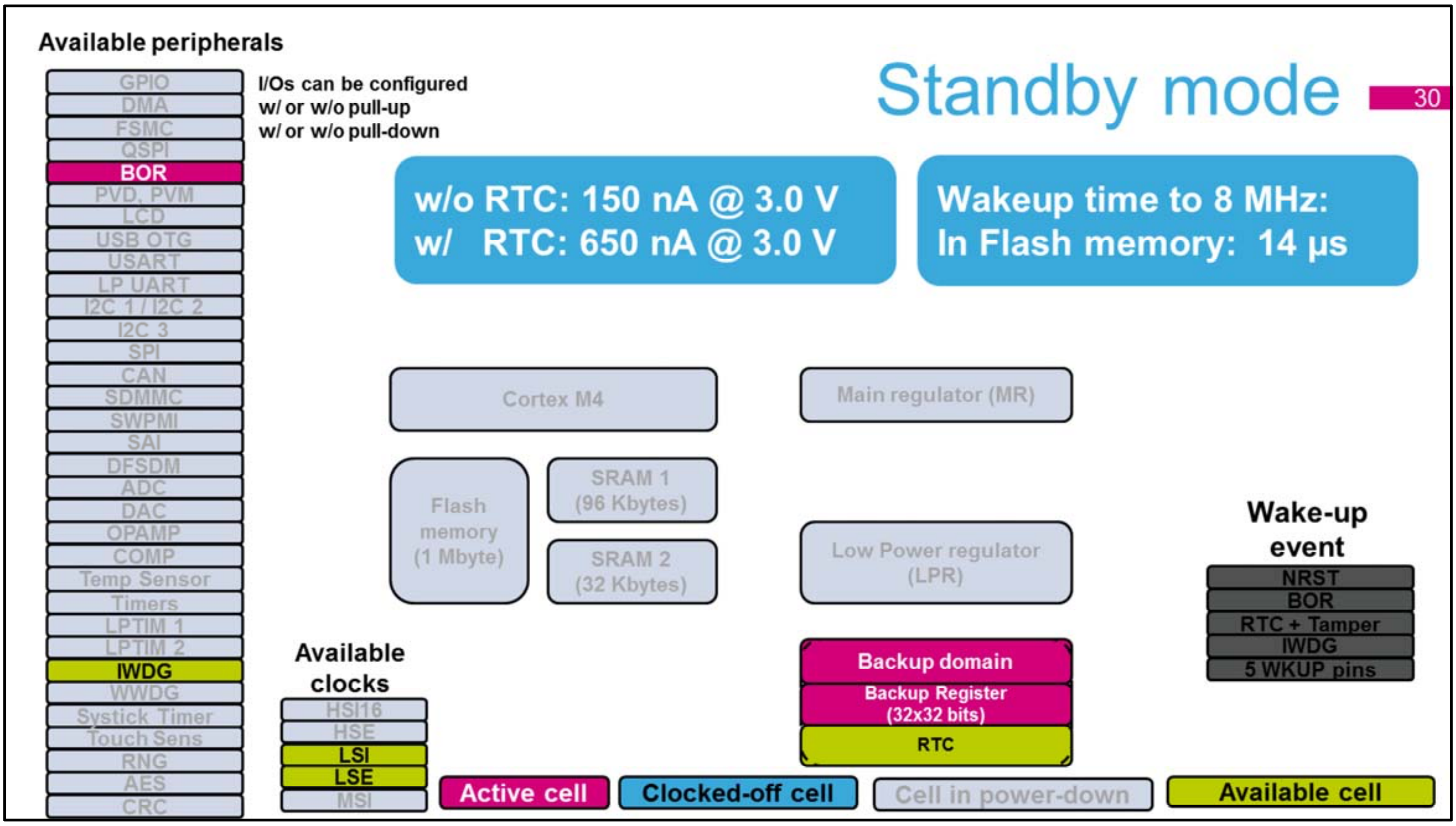
Active cell | Clocked-off cell | Cell in power-down | Available cell

In Standby mode with SRAM2, the main regulator is powered down and the low power regulator supplies the SRAM2 to preserve its content. The RTC, clocked by the internal or external low-speed oscillator, can be activated.

The brown-out reset is always enabled. The independent watchdog can also be enabled in Standby mode.

Reset, brown-out reset, RTC and tamper detection, independent watchdog and any event on the 5 wakeup pins can exit the MCU from Standby mode.

The Standby with SRAM2 consumption without the RTC is around 390 nA typical at 3 V. The wakeup time is approximately 14 µs.



Standby mode

w/o RTC: 150 nA @ 3.0 V
w/ RTC: 650 nA @ 3.0 V

Wakeup time to 8 MHz:
In Flash memory: 14 µs

Available peripherals

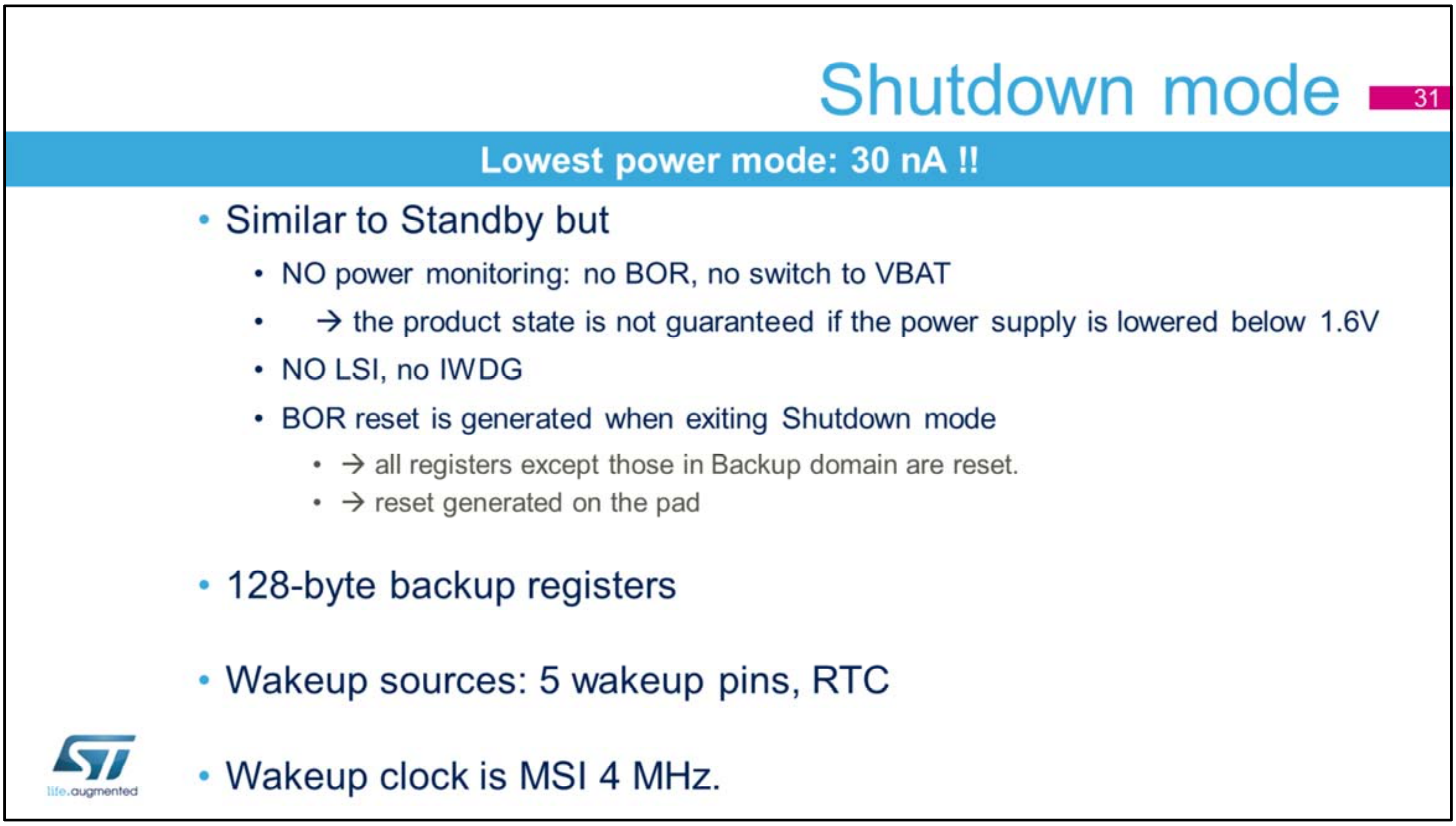
I/Os can be configured
w/ or w/o pull-up
w/ or w/o pull-down

In Standby mode without SRAM2, the main regulator and the low-power regulator are powered down. The RTC, clocked by the internal or external low-speed oscillator, can be activated.

The brown-out reset is always enabled. The independent watchdog can also be enabled in Standby mode.

The wakeup events are the same as those described in Standby mode with SRAM2.

The Standby consumption without RTC is 150 nA typical at 3 V. The wakeup time is approximately 14 µs.



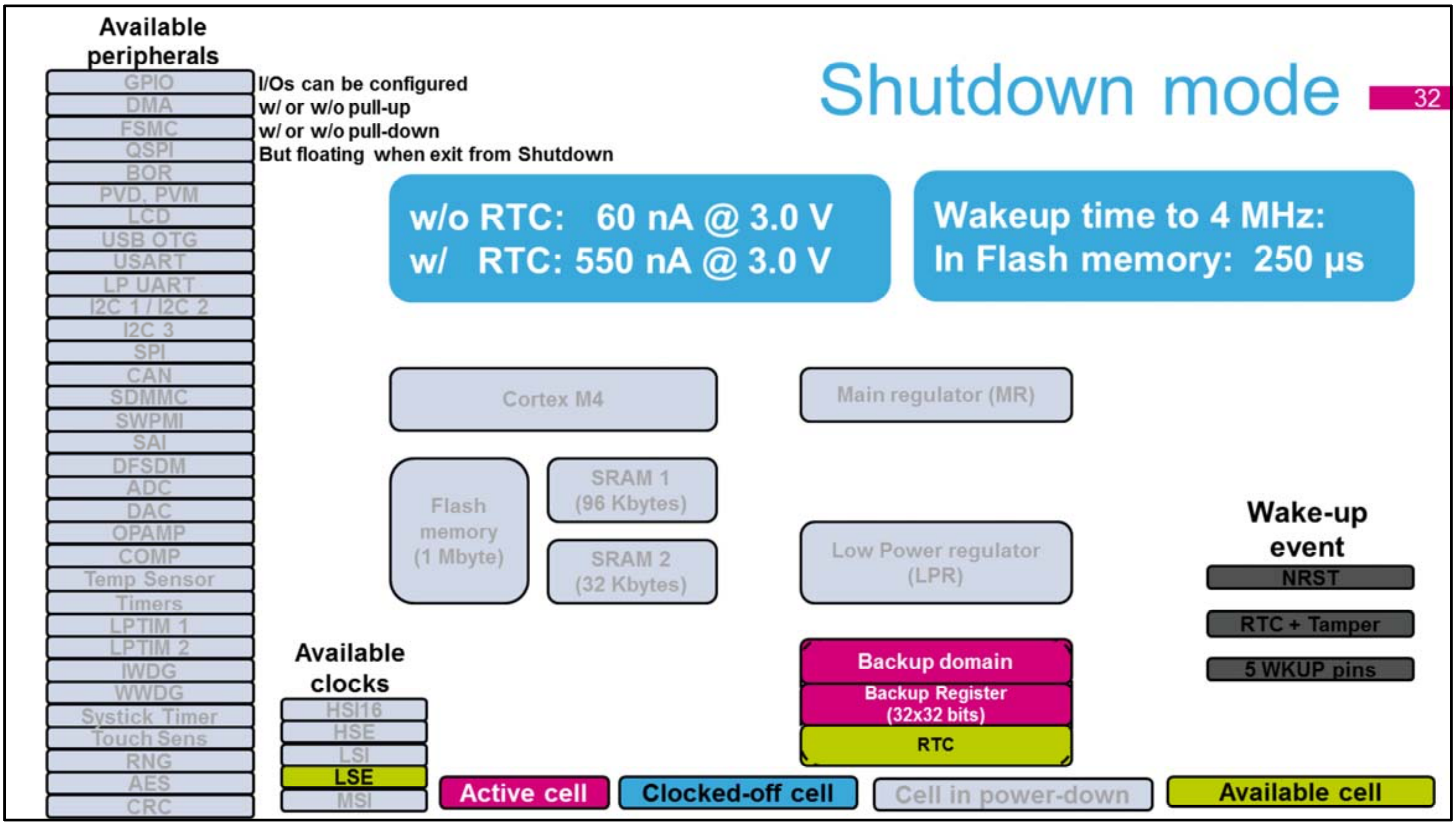
Shutdown mode

Lowest power mode: 30 nA !!

- Similar to Standby but
  - NO power monitoring: no BOR, no switch to VBAT
  - → the product state is not guaranteed if the power supply is lowered below 1.6V
  - NO LSI, no IWDG
  - BOR reset is generated when exiting Shutdown mode
    - → all registers except those in Backup domain are reset.
    - → reset generated on the pad
- 128-byte backup registers
- Wakeup sources: 5 wakeup pins, RTC
- Wakeup clock is MSI 4 MHz.

The shutdown mode is the lowest power mode of the STM32L4, with only 30 nA at 1.8 V.
This mode is similar to Standby mode but without any power monitoring: the brown-out reset is disabled and the switch to VBAT is not supported in Shutdown mode.
Hence the product state is not guaranteed in case the power supply is lowered below 1.6V.
The LSI is not available, and consequently the independent watchdog is also not available. A brown-out reset is generated when the device exits Shutdown mode: all registers are reset except those in the backup domain, and a reset signal is generated on the pad.
The 128-byte backup registers are retained in Shutdown mode.
The wakeup sources are the 5 wakeup pins and the RTC.
When exiting Shutdown mode, the wakeup clock is MSI

at 4 MHz.



Shutdown mode

w/o RTC: 60 nA @ 3.0 V
w/ RTC: 550 nA @ 3.0 V

Wakeup time to 4 MHz:
In Flash memory: 250 µs

Available peripherals

GPIO
DMA
FSMC
QSPI
BOR
PVD, PVM
LCD
USB OTG
USART
LP UART
I2C 1 / I2C 2
I2C 3
SPI
CAN
SDMMC
SWPMI
SAI
DFSDM
ADC
DAC
OPAMP
COMP
Temp Sensor
Timers
LPTIM 1
LPTIM 2
IWDG
WWDG
Systick Timer
Touch Sens
RNG
AES
CRC

I/Os can be configured
w/ or w/o pull-up
w/ or w/o pull-down
But floating when exit from Shutdown

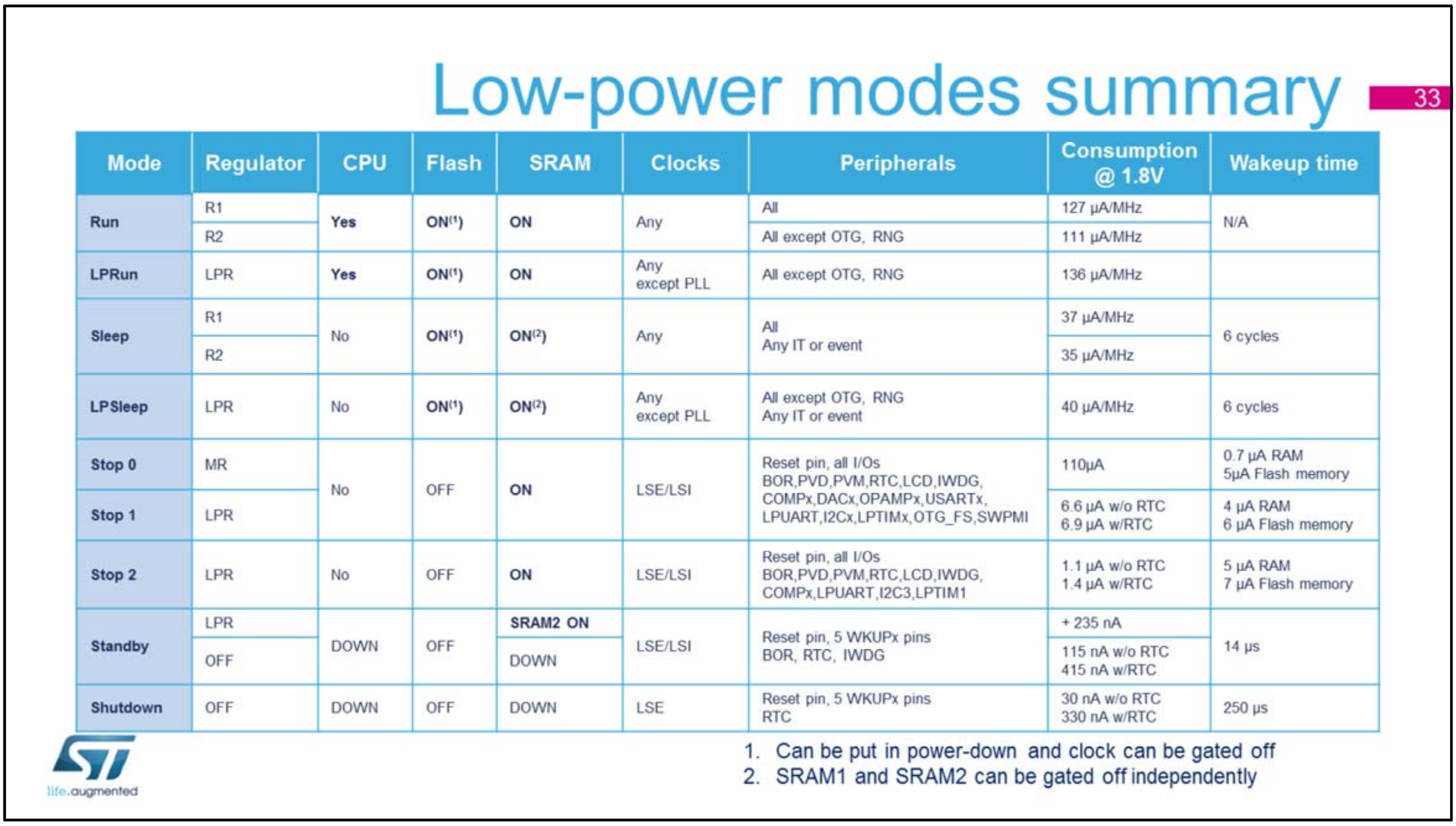
Available clocks

HSI16
HSE
LSI
LSE
MSI

Wake-up event

NRST
RTC + Tamper
5 WKUP pins

In Shutdown mode, the main regulator and the low-power regulator are powered down. The RTC, clocked by the external low-speed oscillator, can be activated.
The brown-out reset is deactivated. Only the external low-speed clock can be enabled.
The wakeup events are the RTC and tamper events, the reset and the 5 wakeup pins.
The Shutdown consumption without RTC is around 60 nA typical at 3 V. The wakeup time is approximately 250 µs.

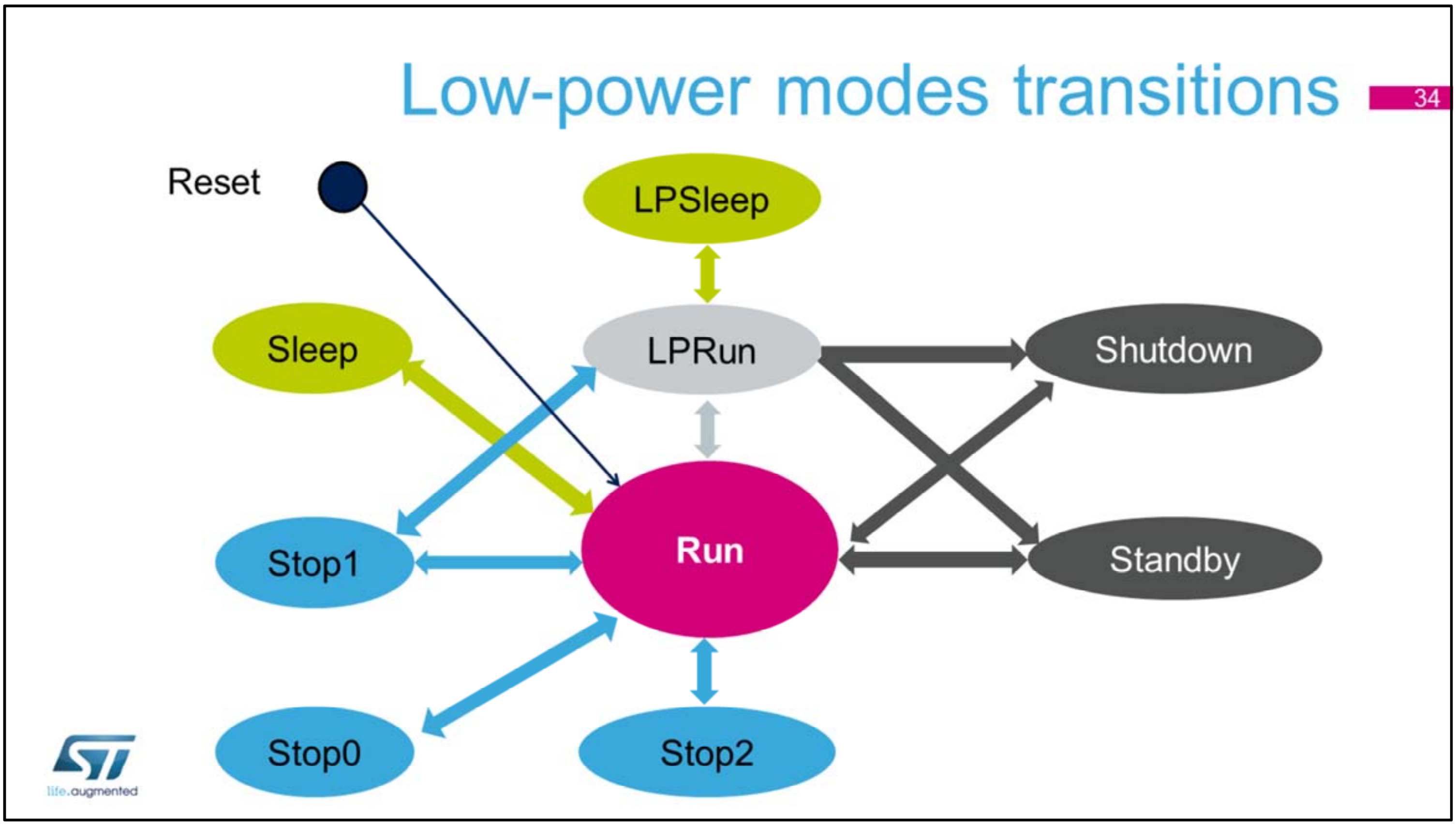


Low-power modes summary

Mode	Regulator	CPU	Flash	SRAM	Clocks	Peripherals	Consumption @ 1.8V	Wakeup time
Run	R1	**Yes**	**ON(1)**	**ON**	Any	All	127 µA/MHz	N/A
	R2					All except OTG, RNG	111 µA/MHz	
LPRun	LPR	**Yes**	**ON(1)**	**ON**	Any except PLL	All except OTG, RNG	136 µA/MHz	
Sleep	R1	No	**ON(1)**	**ON(2)**	Any	All Any IT or event	37 µA/MHz	6 cycles
	R2						35 µA/MHz	
LPSleep	LPR	No	**ON(1)**	**ON(2)**	Any except PLL	All except OTG, RNG Any IT or event	40 µA/MHz	6 cycles
Stop 0	MR	No	OFF	**ON**	LSE/LSI	Reset pin, all I/Os BOR,PVD,PVM,RTC,LCD,IWDG, COMPx,DACx,OPAMPx,USARTx, LPUART,I2Cx,LPTIMx,OTG_FS,SWPMI	110µA	0.7 µA RAM 5µA Flash memory
Stop 1	LPR						6.6 µA w/o RTC 6.9 µA w/RTC	4 µA RAM 6 µA Flash memory
Stop 2	LPR	No	OFF	**ON**	LSE/LSI	Reset pin, all I/Os BOR,PVD,PVM,RTC,LCD,IWDG, COMPx,LPUART,I2C3,LPTIM1	1.1 µA w/o RTC 1.4 µA w/RTC	5 µA RAM 7 µA Flash memory
Standby	LPR	DOWN	OFF	**SRAM2 ON**	LSE/LSI	Reset pin, 5 WKUPx pins BOR, RTC, IWDG	+ 235 nA	14 µs
	OFF			DOWN			115 nA w/o RTC 415 nA w/RTC	
Shutdown	OFF	DOWN	OFF	DOWN	LSE	Reset pin, 5 WKUPx pins RTC	30 nA w/o RTC 330 nA w/RTC	250 µs

1. Can be put in power-down and clock can be gated off
2. SRAM1 and SRAM2 can be gated off independently

Here you can see the summary of all the STM32L4 power modes.



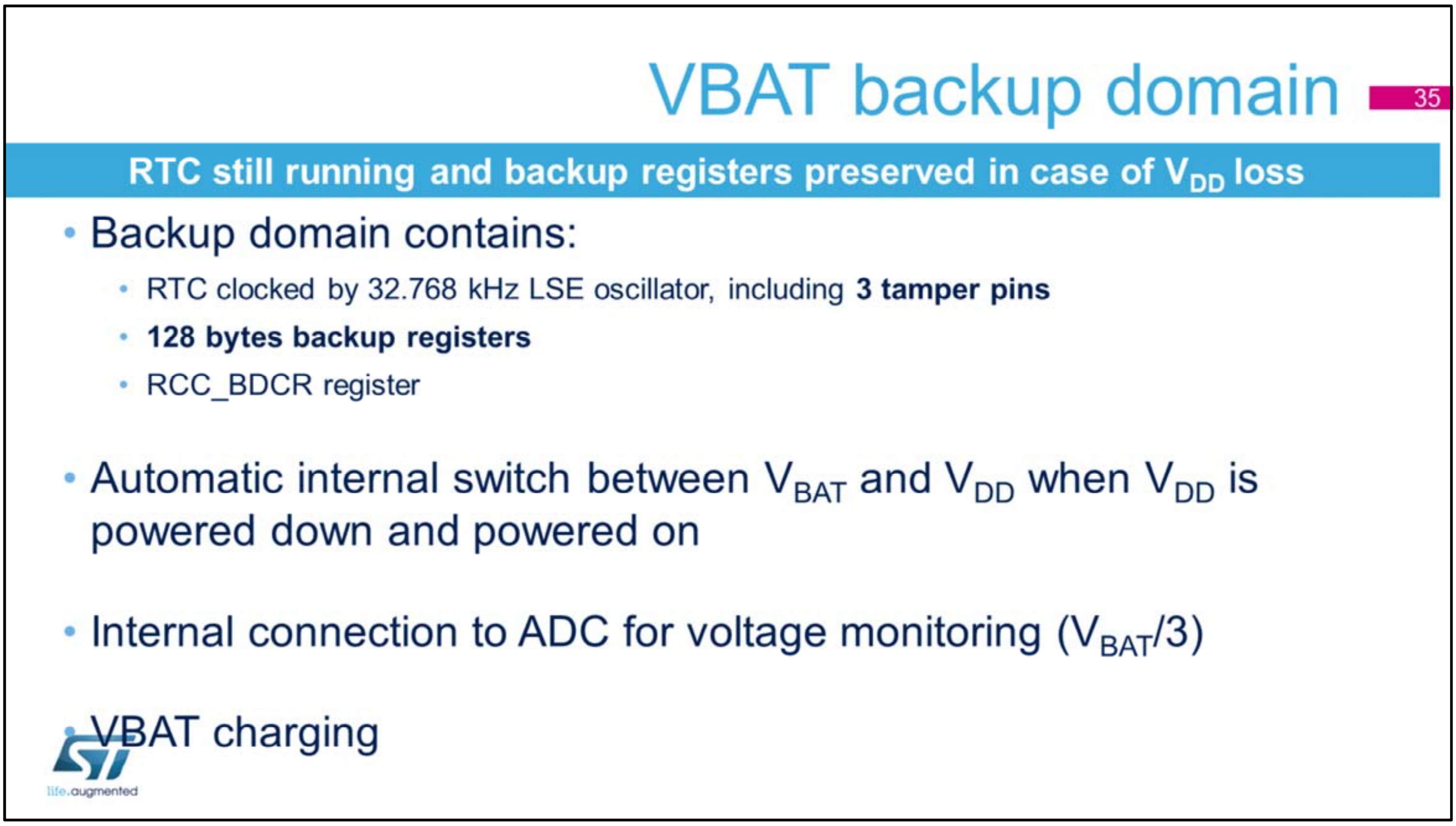
Low-power modes transitions

From Run mode, it is possible to access all low-power modes except Low-power sleep mode. In order to go into Low-power sleep mode, it is required to move first to Low-power run mode and execute a Wait for Interrupt or Wait for Event instruction while the regulator is the low-power regulator. On the other hand, when exiting Low-power sleep mode, the STM32L4 is in Low-power run mode.

When the device is in Low-power run mode, it is possible to go into all low-power modes except Sleep, Stop 0 and Stop 2 modes. Sleep, Stop 0 or Stop 2 modes can only be entered from Run mode.

If the device enters Stop 1 mode from Low-power run mode, it will exit in Low-power run mode.

If the device enters Standby or Shutdown from Low-power run mode, it will exit in Run mode.



VBAT backup domain

RTC still running and backup registers preserved in case of V_{DD} loss

- Backup domain contains:
  - RTC clocked by 32.768 kHz LSE oscillator, including **3 tamper pins**
  - **128 bytes backup registers**
  - RCC_BDCR register
- Automatic internal switch between V_{BAT} and V_{DD} when V_{DD} is powered down and powered on
- Internal connection to ADC for voltage monitoring ($V_{BAT}/3$)
- VBAT charging

The backup domain allows to keep the RTC functional and to preserve the backup registers in case the VDD supply is down, thanks to a backup battery connected to the VBAT pin.

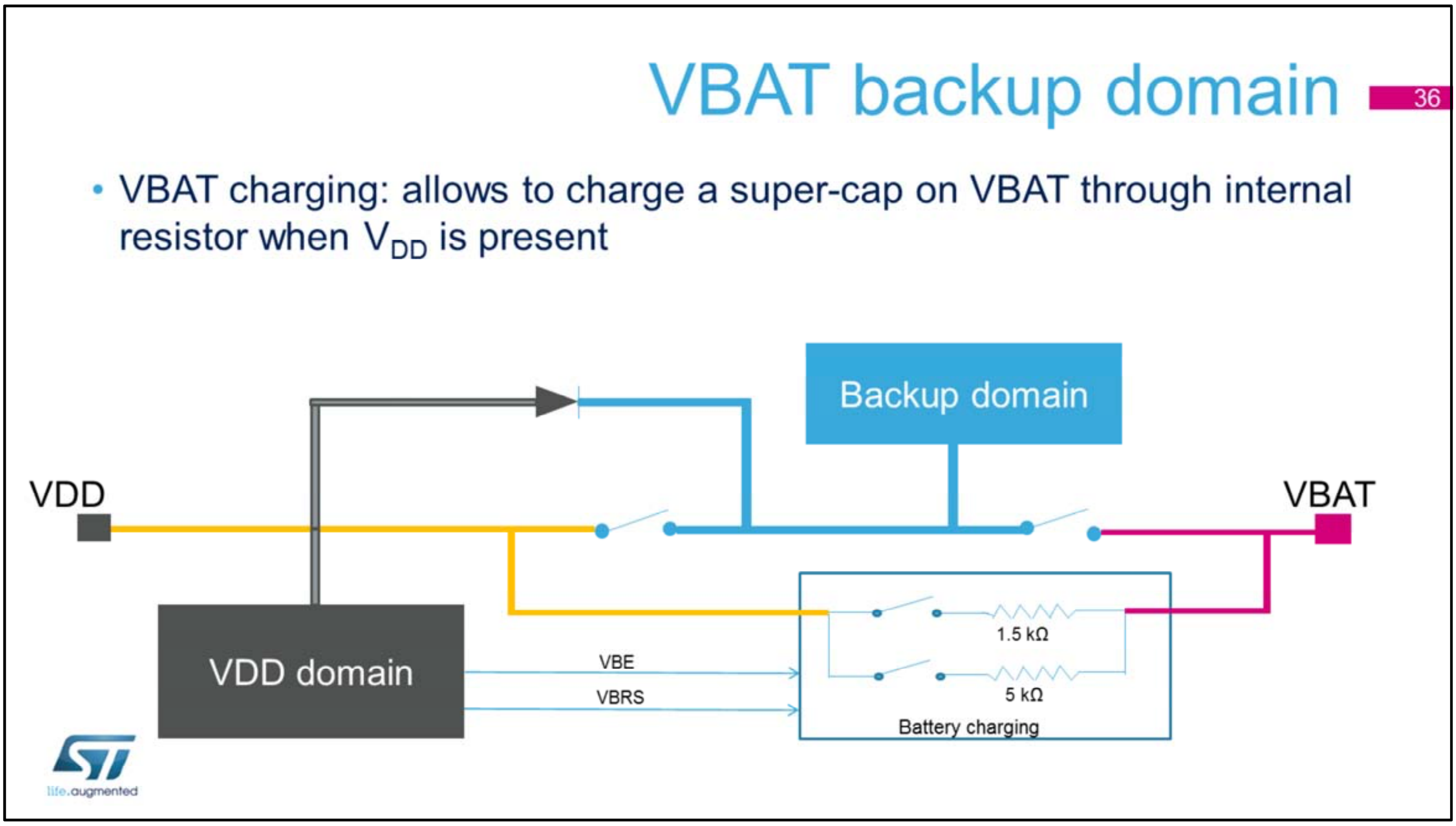
The backup domain contains the RTC clocked by the low-speed external oscillator at 32.768 kHz. 3 tamper pins are functional in VBAT mode, and will erase the 128-byte backup registers also included in the VBAT domain, in case of intrusion detection.

The backup domain also contains the RTC clock control logic.

In case VDD drops below a certain threshold, the backup domain power supply automatically switches to VBAT. When VDD is back to normal, the backup domain power supply automatically switches back to VDD.

The VBAT voltage is internally connected to an ADC input channel in order to monitor the backup battery

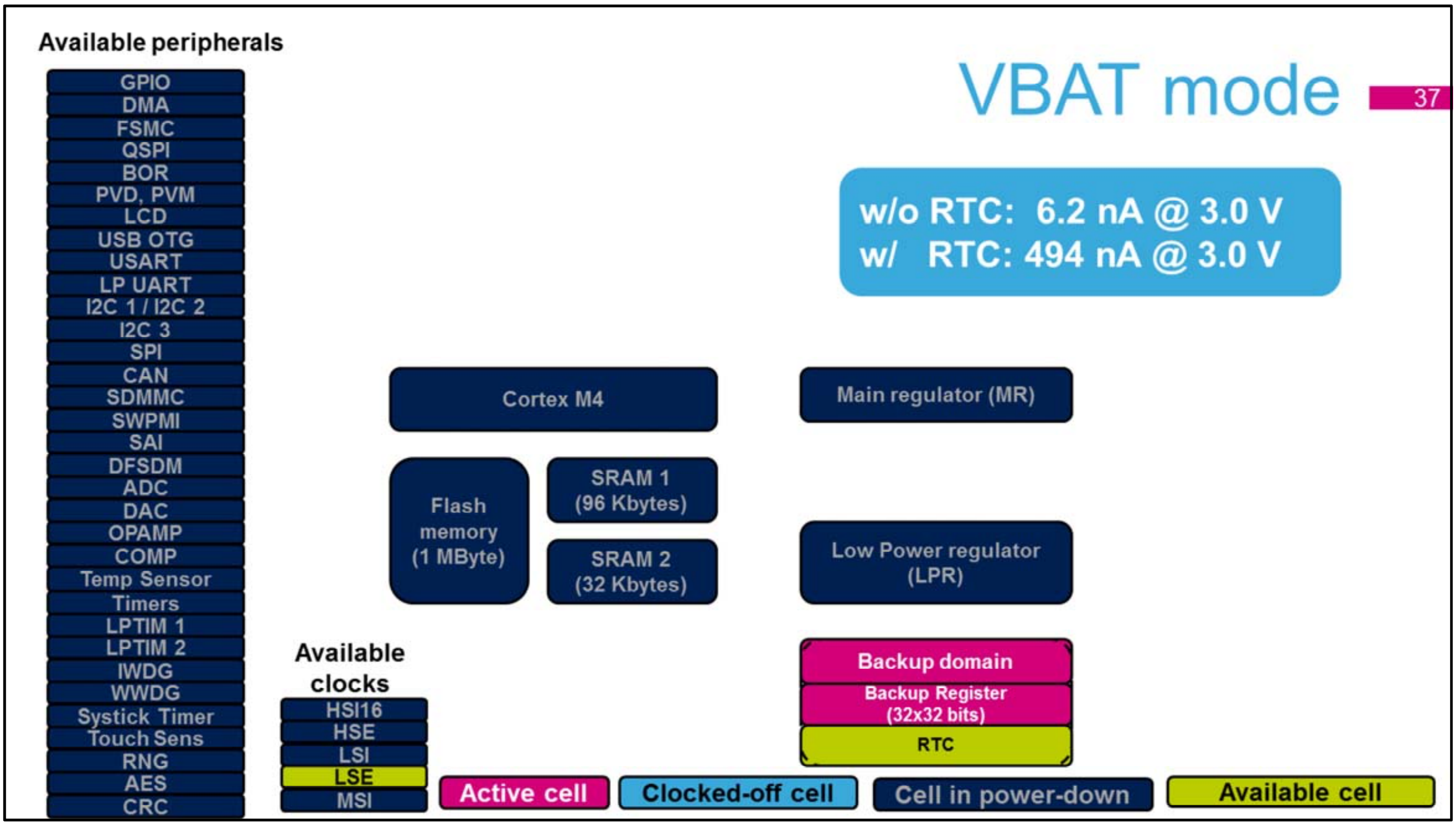
level.
When VDD is present, the battery connected to VBAT can be charged from the VDD supply.



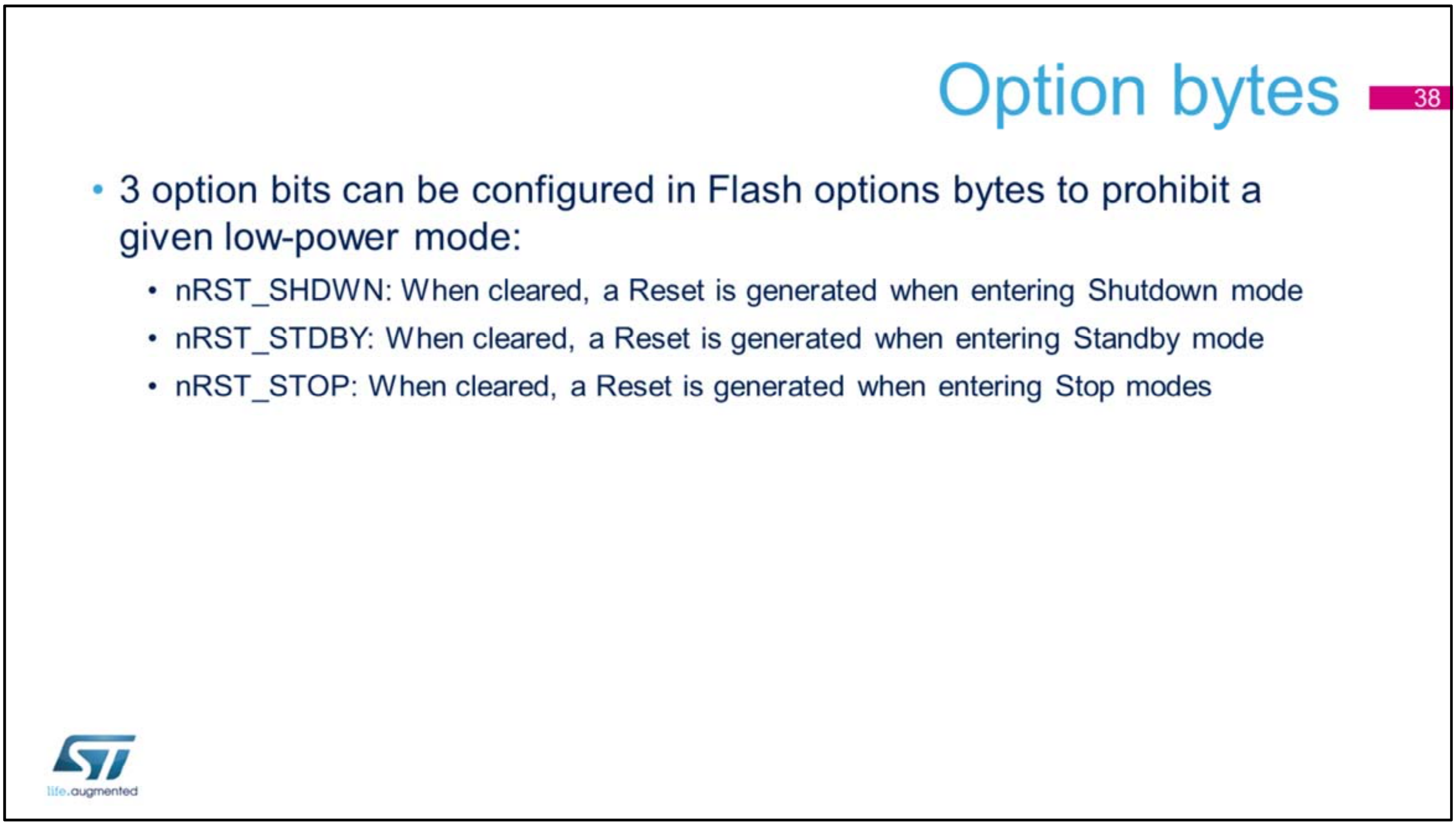
VBAT backup domain

- VBAT charging: allows to charge a super-cap on VBAT through internal resistor when V_{DD} is present

The battery charging feature allows to charge a super-cap connected to VBAT pin through internal resistor when VDD supply is present. The charging is enabled by software and is done either through a 5kΩ or 1.5kΩ resistor depending on software. Battery charging is automatically disabled in VBAT mode.



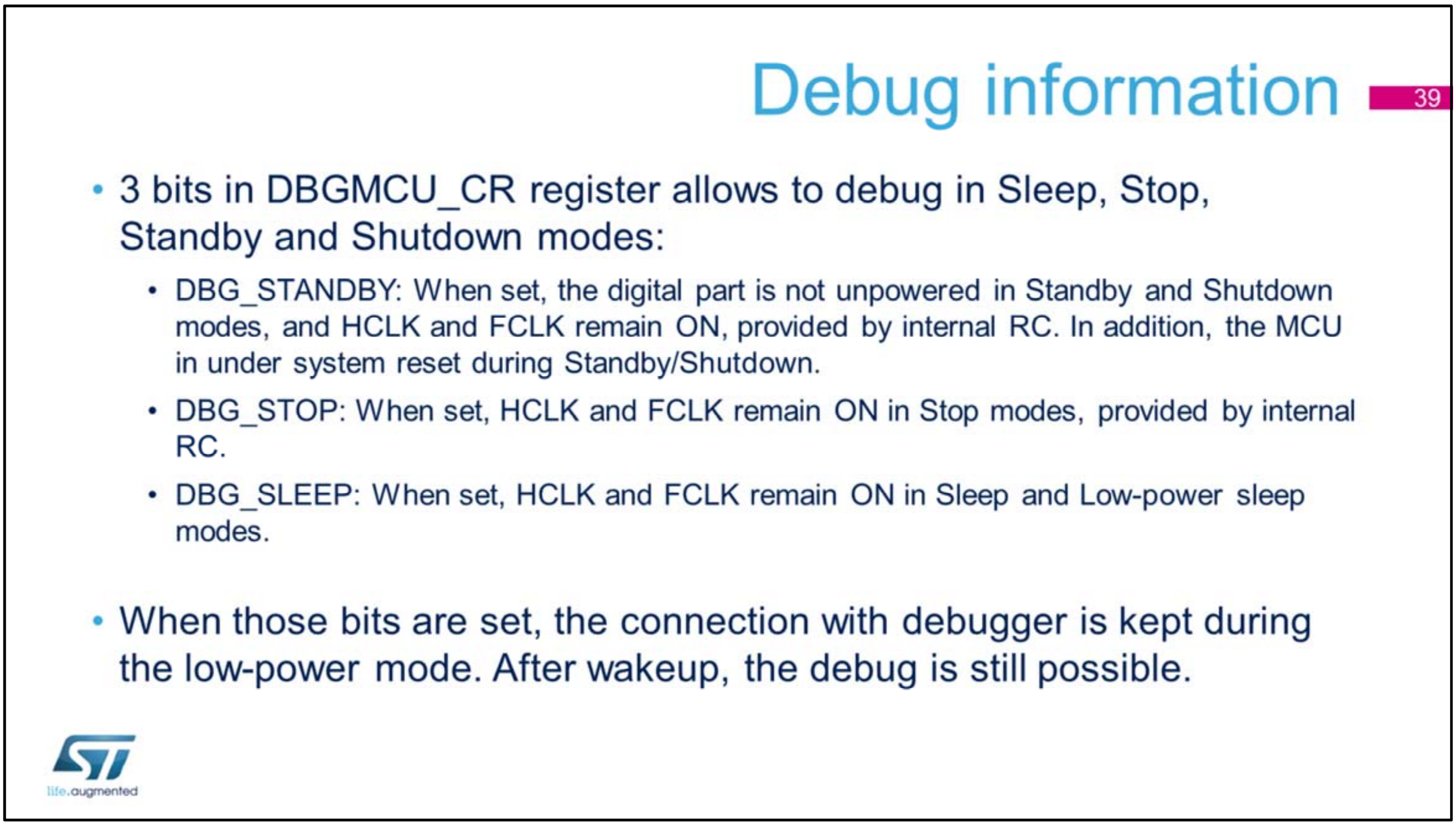
In VBAT mode, the entire MCU is in Power-down mode except the backup domain, including the 128-byte backup registers, RTC and external low-speed clock. The consumption from VBAT pin is approximately 6 nA without the RTC at 3 V, and 500 nA with the RTC.



Option bytes

- 3 option bits can be configured in Flash options bytes to prohibit a given low-power mode:
  - nRST_SHDWN: When cleared, a Reset is generated when entering Shutdown mode
  - nRST_STDBY: When cleared, a Reset is generated when entering Standby mode
  - nRST_STOP: When cleared, a Reset is generated when entering Stop modes

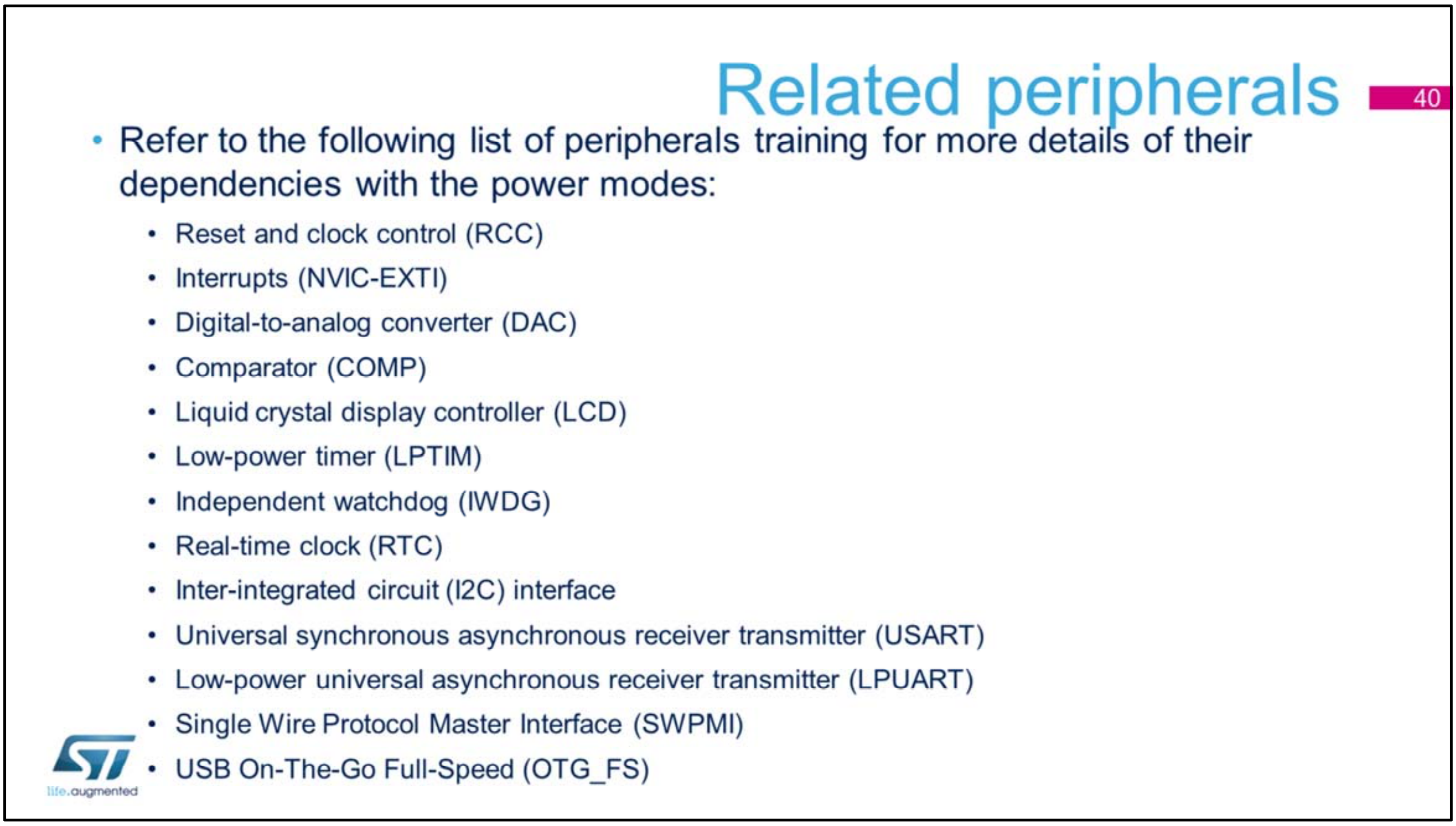
3 bits are available in the Flash option bytes to prohibit a given low-power mode. When cleared, an option bit configures reset generation when entering Shutdown mode. Another bit configures reset generation when entering Standby mode and the last bit configures reset generation when entering Stop modes.



Debug information

- 3 bits in DBGMCU_CR register allows to debug in Sleep, Stop, Standby and Shutdown modes:
  - DBG_STANDBY: When set, the digital part is not unpowered in Standby and Shutdown modes, and HCLK and FCLK remain ON, provided by internal RC. In addition, the MCU in under system reset during Standby/Shutdown.
  - DBG_STOP: When set, HCLK and FCLK remain ON in Stop modes, provided by internal RC.
  - DBG_SLEEP: When set, HCLK and FCLK remain ON in Sleep and Low-power sleep modes.
- When those bits are set, the connection with debugger is kept during the low-power mode. After wakeup, the debug is still possible.

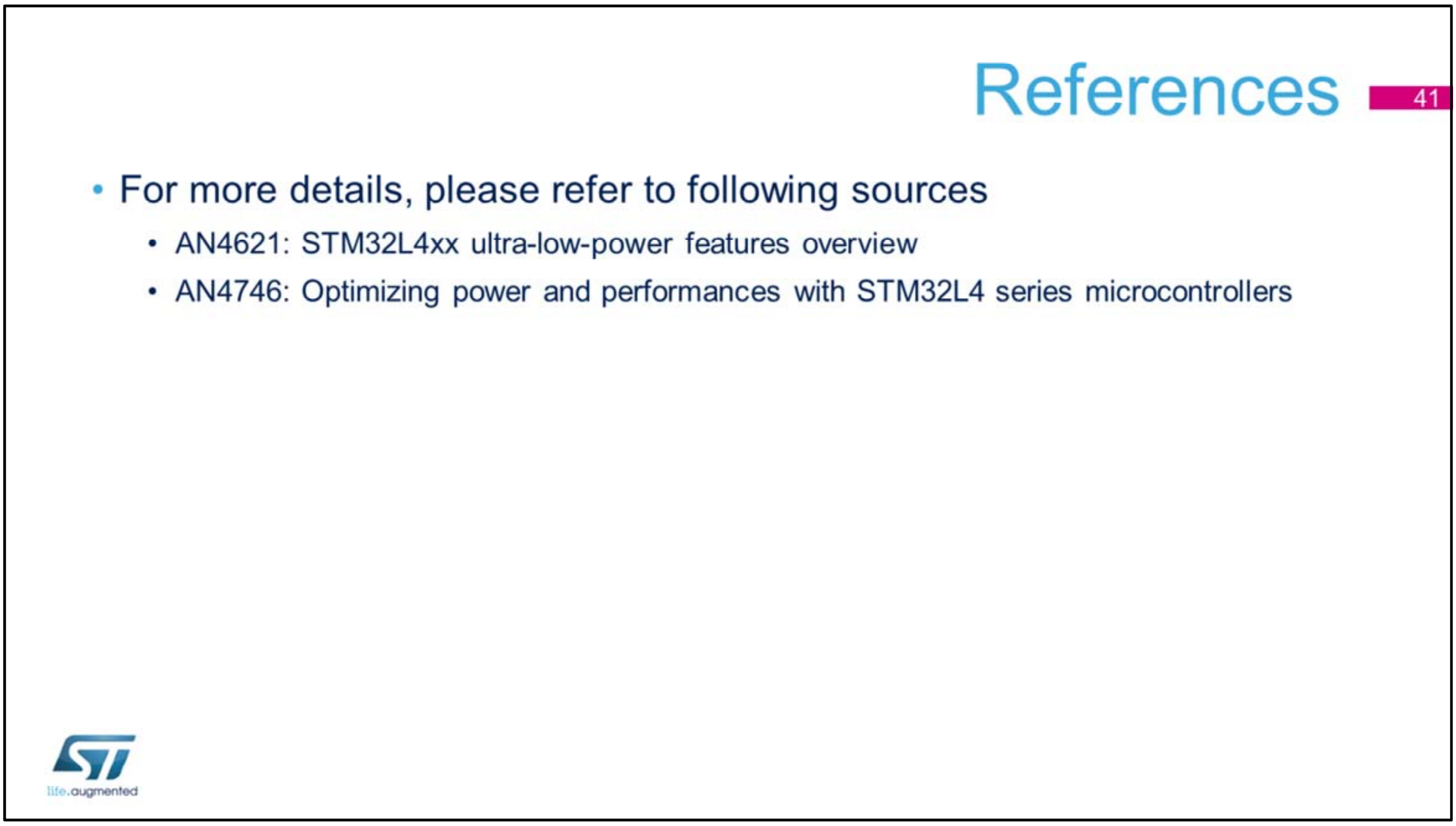
3 bits are available in the Debug Control Register, in order to allow debugging in Sleep, Stop, Standby and Shutdown modes. When the related bit is set, the regulator is kept ON in Standby and Shutdown modes, and the HCLK and FCLK clocks remain ON to keep the debugger active. This maintains the connection with the debugger during the low-power modes, and continues debugging after wakeup. Remember to clear these bits when the MCU is not under debug, because the consumption is higher in all low-power modes when these bits are set, due to the fact they force the clocks and the regulators to remain enabled.



Related peripherals

- Refer to the following list of peripherals training for more details of their dependencies with the power modes:
  - Reset and clock control (RCC)
  - Interrupts (NVIC-EXTI)
  - Digital-to-analog converter (DAC)
  - Comparator (COMP)
  - Liquid crystal display controller (LCD)
  - Low-power timer (LPTIM)
  - Independent watchdog (IWDG)
  - Real-time clock (RTC)
  - Inter-integrated circuit (I2C) interface
  - Universal synchronous asynchronous receiver transmitter (USART)
  - Low-power universal asynchronous receiver transmitter (LPUART)
  - Single Wire Protocol Master Interface (SWPMI)
  - USB On-The-Go Full-Speed (OTG_FS)

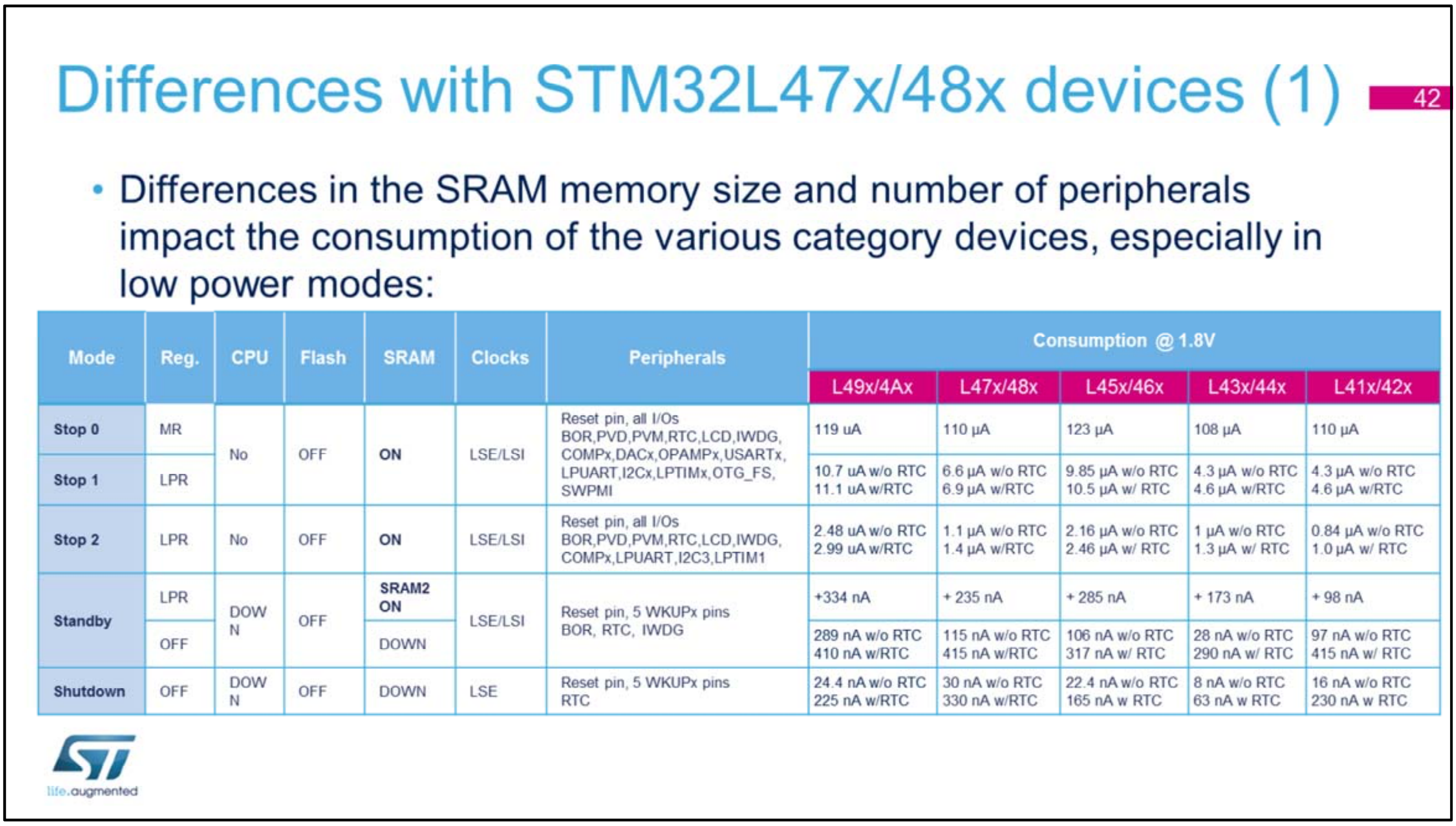
In addition to this training, you can refer to the Reset and Clock Control, Interrupts trainings as well as those for all the peripherals with wakeup from Stop capability.



References

- For more details, please refer to following sources
  - AN4621: STM32L4xx ultra-low-power features overview
  - AN4746: Optimizing power and performances with STM32L4 series microcontrollers

For more details, please refer to application note *STM32L4 ultra-low-power features overview*.



Differences with STM32L47x/48x devices (1)

- Differences in the SRAM memory size and number of peripherals impact the consumption of the various category devices, especially in low power modes:

Mode	Reg.	CPU	Flash	SRAM	Clocks	Peripherals	Consumption @ 1.8V				
							L49x/4Ax	L47x/48x	L45x/46x	L43x/44x	L41x/42x
Stop 0	MR	No	OFF	**ON**	LSE/LSI	Reset pin, all I/Os BOR,PVD,PVM,RTC,LCD,IWDG, COMPx,DACx,OPAMPx,USARTx, LPUART,I2Cx,LPTIMx,OTG_FS, SWPMI	119 uA	110 µA	123 µA	108 µA	110 µA
Stop 1	LPR						10.7 uA w/o RTC 11.1 uA w/RTC	6.6 µA w/o RTC 6.9 µA w/RTC	9.85 µA w/o RTC 10.5 µA w/ RTC	4.3 µA w/o RTC 4.6 µA w/RTC	4.3 µA w/o RTC 4.6 µA w/RTC
Stop 2	LPR	No	OFF	**ON**	LSE/LSI	Reset pin, all I/Os BOR,PVD,PVM,RTC,LCD,IWDG, COMPx,LPUART,I2C3,LPTIM1	2.48 uA w/o RTC 2.99 uA w/RTC	1.1 µA w/o RTC 1.4 µA w/RTC	2.16 µA w/o RTC 2.46 µA w/ RTC	1 µA w/o RTC 1.3 µA w/ RTC	0.84 µA w/o RTC 1.0 µA w/ RTC
Standby	LPR	DOWN	OFF	**SRAM2 ON**	LSE/LSI	Reset pin, 5 WKUPx pins BOR, RTC, IWDG	+334 nA	+ 235 nA	+ 285 nA	+ 173 nA	+ 98 nA
	OFF			DOWN			289 nA w/o RTC 410 nA w/RTC	115 nA w/o RTC 415 nA w/RTC	106 nA w/o RTC 317 nA w/ RTC	28 nA w/o RTC 290 nA w/ RTC	97 nA w/o RTC 415 nA w/ RTC
Shutdown	OFF	DOWN	OFF	DOWN	LSE	Reset pin, 5 WKUPx pins RTC	24.4 nA w/o RTC 225 nA w/RTC	30 nA w/o RTC 330 nA w/RTC	22.4 nA w/o RTC 165 nA w RTC	8 nA w/o RTC 63 nA w RTC	16 nA w/o RTC 230 nA w RTC

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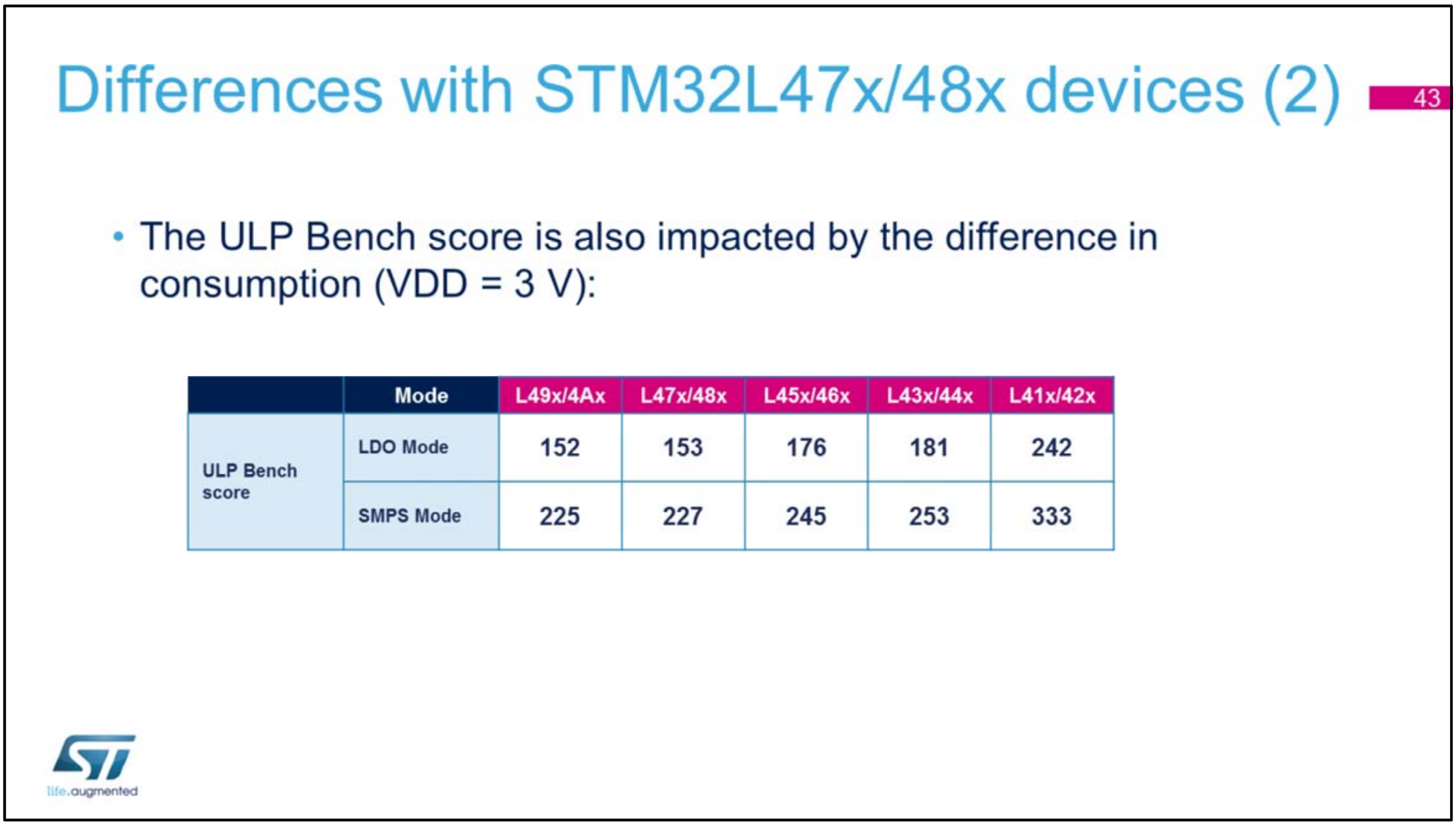
This slide presents the key consumption differences between STM32L4 devices.



Differences with STM32L47x/48x devices (2)

- The ULP Bench score is also impacted by the difference in consumption (VDD = 3 V):

	Mode	L49x/4Ax	L47x/48x	L45x/46x	L43x/44x	L41x/42x
ULP Bench score	**LDO Mode**	152	153	176	181	242
	SMPS Mode	225	227	245	253	333

This slide presents the key differences in ULP Bench scores between STM32L4 devices.