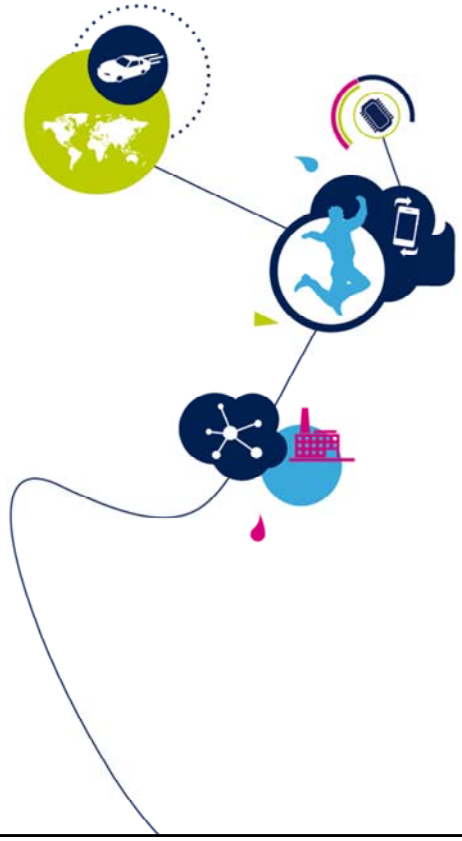
STM32MP1 – HW ARCH

Hardware Architecture
Revision 2.0



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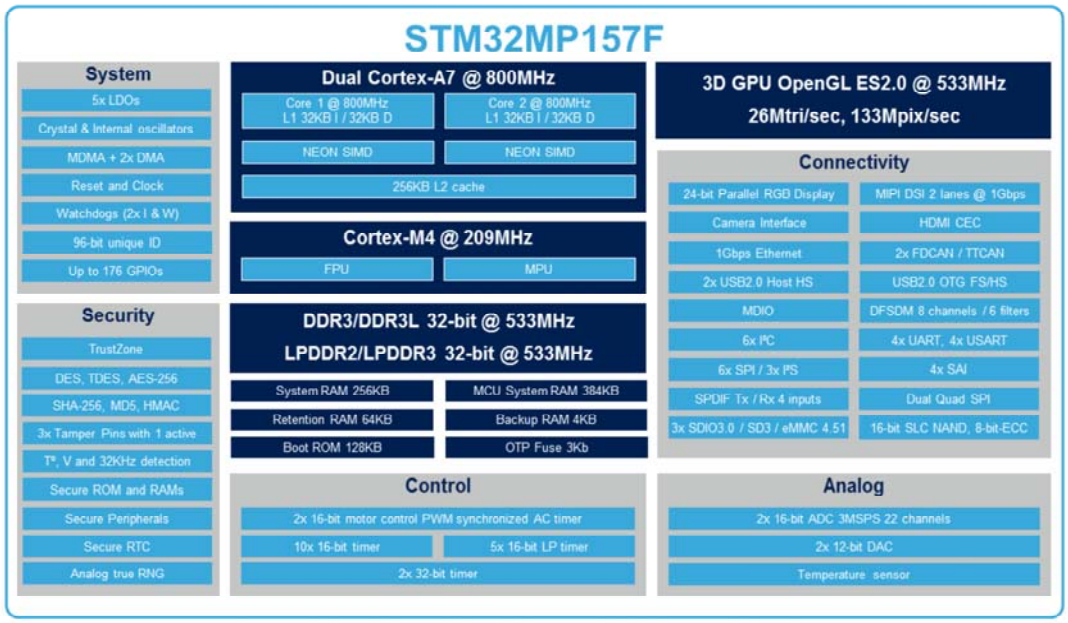
Hello, and welcome to this overview of the hardware architecture of the STM32MP1 series.

STM32MP1 Block Diagram



This block diagram summarizes the key features of the STM32MP157F which is part of the high-end line of the STM32MP1 Series.

The STM32MP157F microprocessor integrates Dual Cortex®-A7 32-bit core with single- and double-precision floating point units, plus the Arm® NEON™ Advanced SIMD instruction set and can run up to 800MHz. Each core has a 32 Kbytes level 1 Instruction Cache and a 32 Kbytes level 1 Data Cache, plus 256 Kbytes of level 2 cache shared between the two cores.

In addition to this powerful application core, it also embeds a Cortex®-M4 32-bit RISC core (with single-precision floating point unit) running at up to 209 MHz.

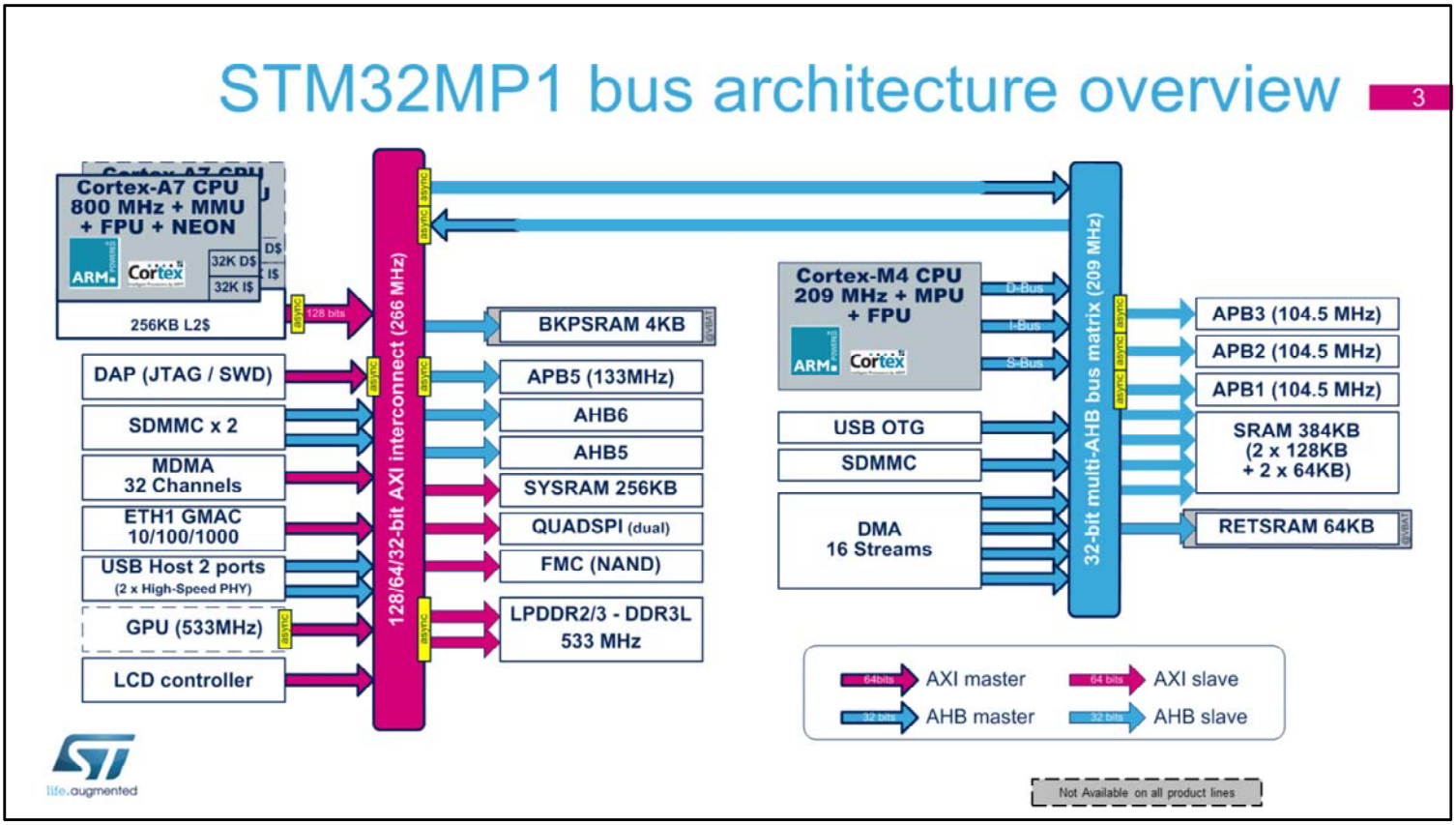
Finally, a powerful 3D GPU is available supporting Open GL ES 2.0 and running at up to 533 MHz.

The internal SRAM memory size is 708 Kbytes with a scattered architecture split into:

- 256 Kbytes of AXI System RAM

- plus 384 Kbytes of AHB MCU Subsystem RAM
- plus 64 Kbytes of AHB MCU subsystem retention RAM in backup domain
- and 4 Kbytes of SRAM in backup domain to keep data in the lowest power modes.

This line also includes up to 37 communication peripherals in addition to an LCD-TFT controller interface which can feed pixel to a parallel or Display Serial Interface (DSI) having two data lanes up to 1 Gbit/s each.
The STM32MP157 line embeds also low-power 16-bit ADCs running at up to 3 Msamples/s, 12-bit DACs, as well as 29 timers.



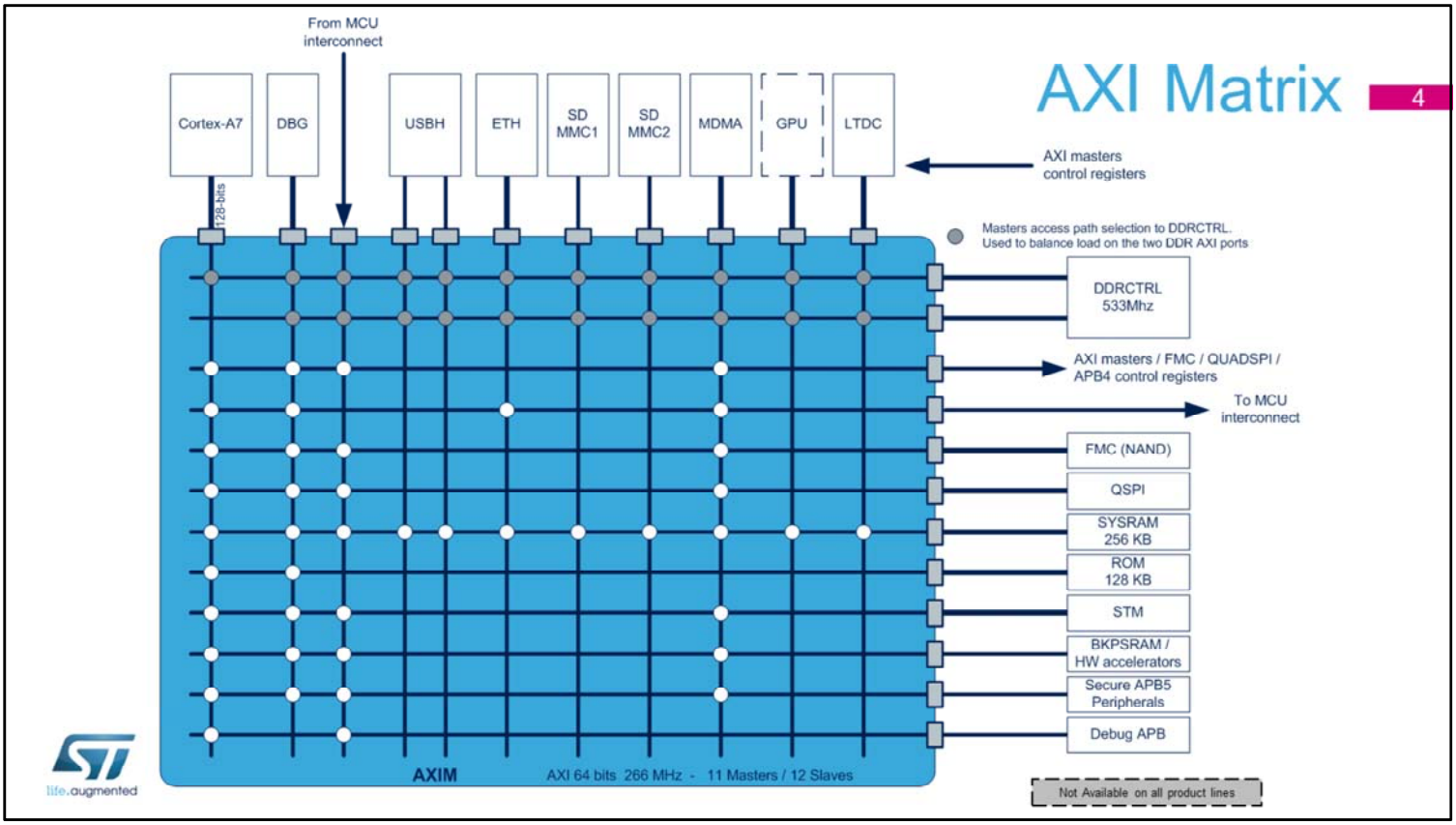
The STM32MP1 bus architecture is split in two interconnect matrix (Arm Cortex-A7 and Arm Cortex-M4) operating in different frequency domains, which can be set in low power modes independently.

- One high-speed Arm CoreLink NIC-400 network interconnect AXI-based performing interconnection between master and slaves on Arm Cortex-A7 side (called MPU-side) , operating at 266 MHz (ck_aclk) and allowing an internal bandwidth up to 2 Gbytes/s between each master and slave. This matrix is optimized for low latency and very high bandwidth master transfers to/from external DDR as well as internal SRAMs. An external DDR memory provides a raw bandwidth up to 4 GBytes/s. Peripherals belonging to the AXI domain are connected to AHB5, AHB6, APB4 (thru AHB6) and APB5 buses.

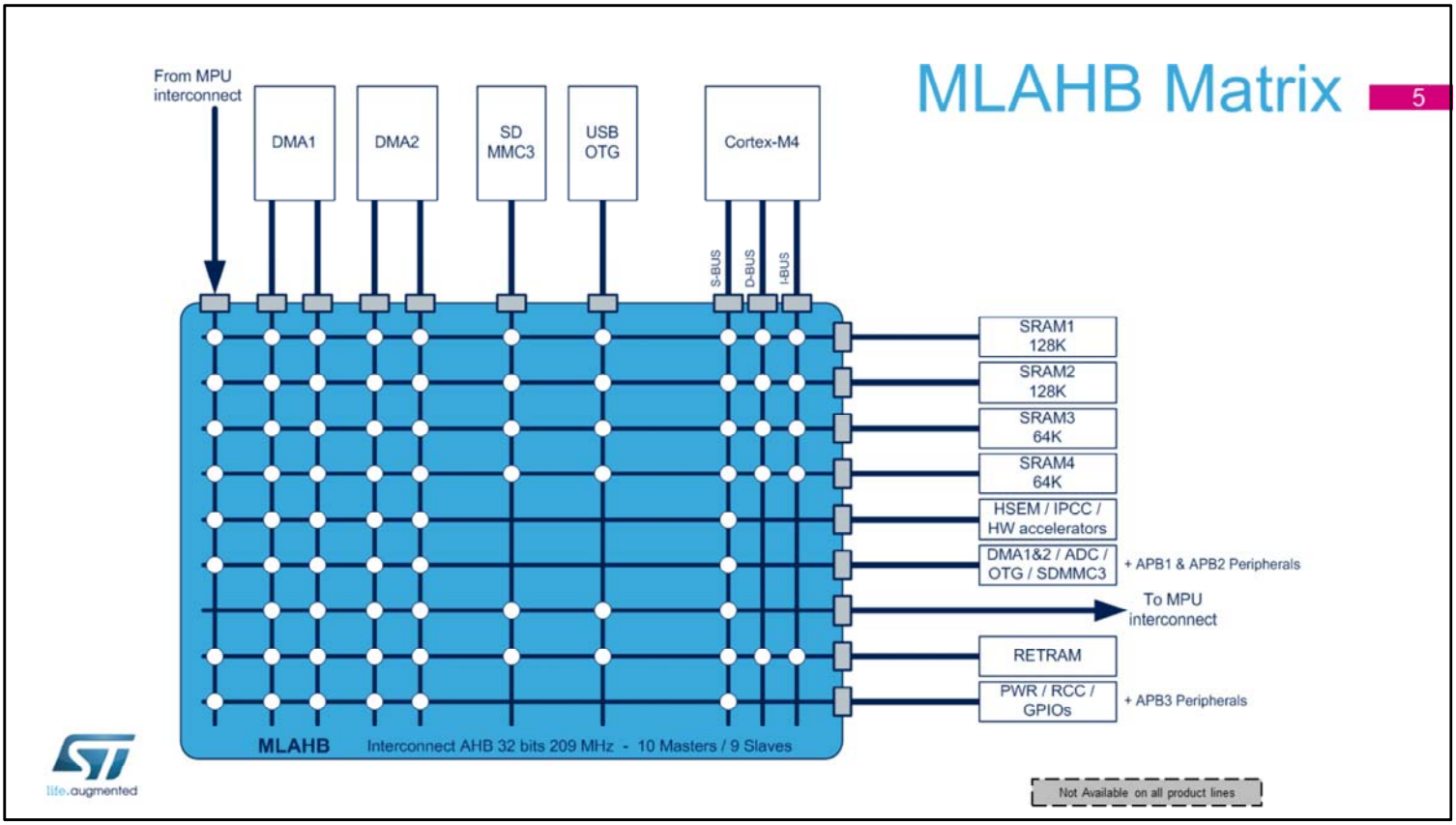
- One multi-layer AHB interconnect (MLAHB) performing interconnection between master and slaves on Arm Cortex-M4 side (called MCU-side) with an architecture inherited from former MCU and operating at 209 MHz (ck_mcu).

AXI interconnect matrix (AXIM) and Multi-layer AHB (ML-AHB) are connected together to enable the sharing of any peripheral by any master.
Blocks with dashed lines are not available on all product lines.

Security is not shown in this overview.



The AXI Matrix is enabling the interconnection between up to 11 masters and 12 slaves peripherals.



AHB Matrix is enabling the interconnection between up to 10 masters and 9 slaves peripherals.

Memories Summary

	Memory	Type	Size	TrustZone Access Control	Cortex-A7 access	Cortex-M4 access
Embedded memories	BOOTROM	ROM	128 KB	●	●	
	SRAM	SRAM	384 KB		●	●
	SYSRAM	SRAM	256 KB	●	●	●
	RETRAM	SRAM (On VBAT)	64 KB	●	●	●
	BKPSRAM	SRAM (On VBAT)	4 KB	●	●	●
External memories	DDR SDRAM	DDR3, DDR3L, LPDDR2, LPDDR3	Up to 1 GB	●	●	
	SDMMC	SD-Card, *e*•MMC			●	● *(SDMMC3 only)*
	QUADSPI	SPI Flash	Up to 512 MB (1) Up to 4 GB (2)		●	●
	FMC NOR	NOR Flash, SRAM	Up to 256 MB		●	●
	FMC NAND	NAND Flash	Up to 256 MB		●	●

(1) Memory-mapped mode
(2) Indirect-mode

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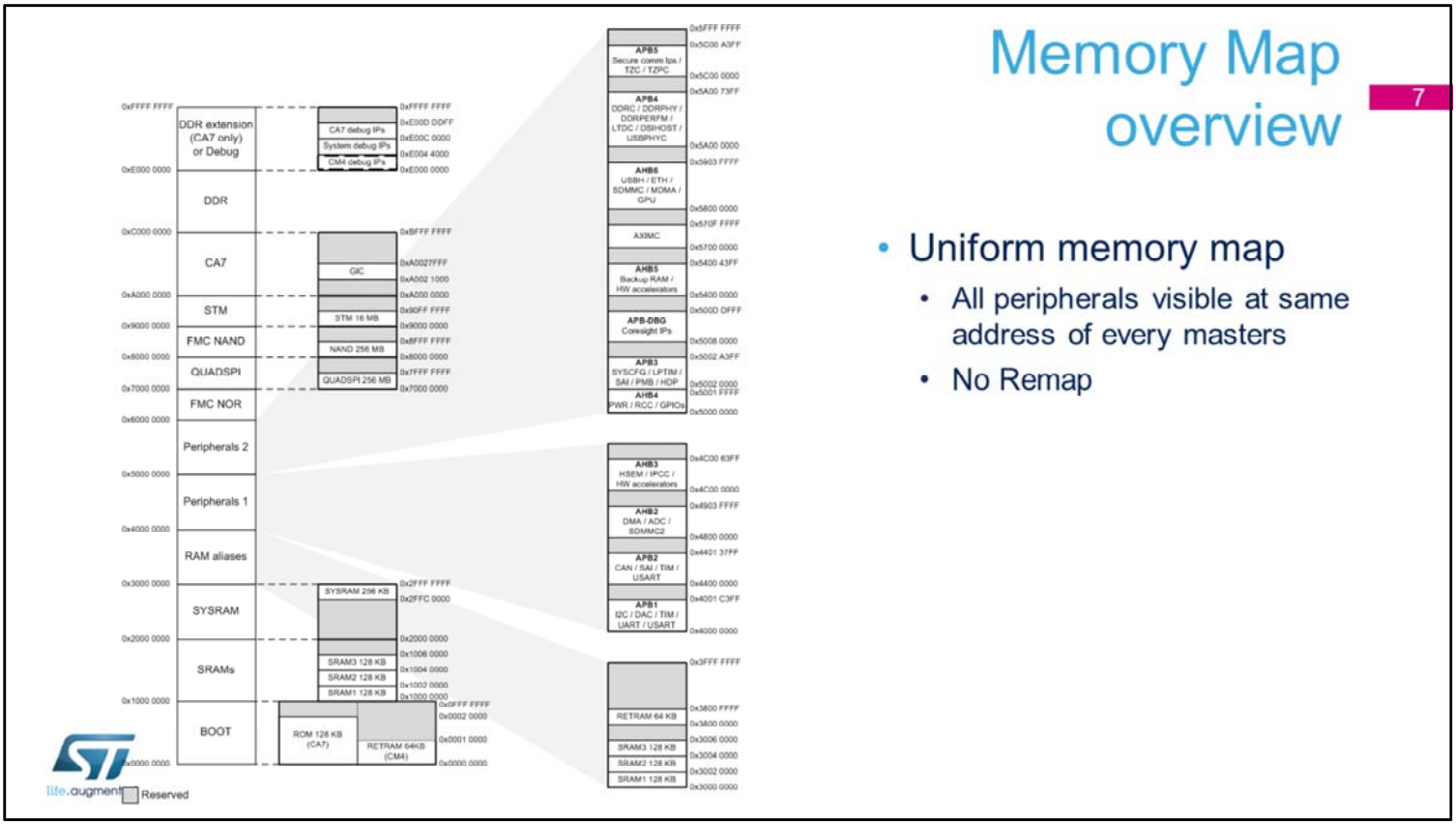
Some memories are dedicated to Cortex-A7 core access (e.g. BootROM, DDR), and benefit from the optional access control using the Arm TrustZone technology.



The memory map addressed by any masters is the same, all peripherals are visible at the same address, simplifying the development and debug.
There is no dynamic memory remapping, only part of the MCU SRAM and RETRAM memories are aliased on two locations to allow Cortex-M4 access optimizations.

Reset and Clocking (RCC)

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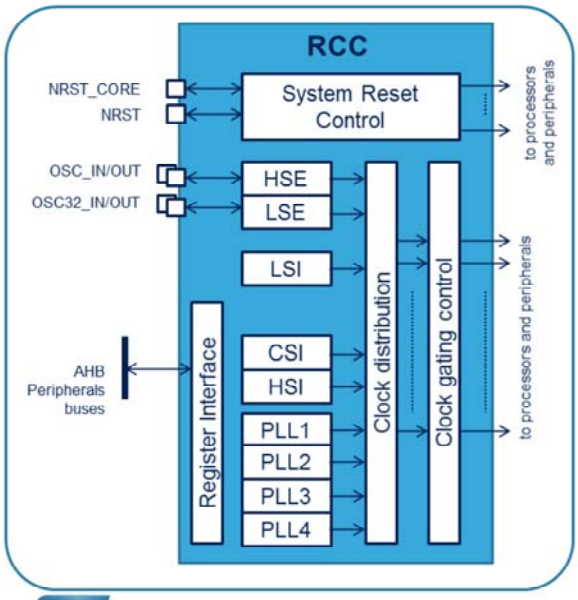

- The Reset and Clock Controller (RCC) manages:
  - The generation of all the clocks,
    - 4xPLLs, RC oscillators, Crystal oscillators…
  - The gating of all the clocks
    - Possibility to enable/disable clocks for each peripheral
  - The control of all the system and peripheral resets.

Application benefits

- High flexibility regarding the clock sources to meet consumption and accuracy requirements.
- Safe and flexible reset management

The reset and clock controller (RCC) manages the system reset and the peripherals clock generation. STM32MP15x microprocessor embeds 3 internal oscillators, 2 oscillators for an external crystal or resonator, and 4 phase-locked loops (PLL) managed by the RCC.
Outside the RCC, there is also one dedicated PLL for the High-Speed USB. For STM32MP15x lines with a Display Serial Interface (DSI), one additional PLL is dedicated to the clocking of this interface.

Many peripherals have their own clock, independent of the system clock to allow maximum flexibility.
The RCC provides high flexibility in the choice of the clock sources. This enables the system designer to meet both power consumption and accuracy requirements.
The numerous independent peripheral clocks allow a

designer to adjust the system power consumption without impacting the communication baud rates, and also keep some peripherals active in low-power mode.

Power Supplies

Name	Typical or Range	Description
VDD	**1.7V – 3.6V**	Power supply input for I/Os
VDD_ANA		Power supply input for system analog like RCC, PWR. To be connected to VDD
*VDD_DSI***		Power supply input for DSI regulator. To be connected to VDD
VDD_PLL		Power supply input for PLLs. To be connected to VDD
VDD_CORE	**1.2V**	Power supply input for Digital Core domain
VDDA	**1.7V – 3.6V**	Analog Power supply input for ADCs, DACs and voltage reference buffers
VDDQ_DDR	**1.2V / 1.35V / 1.5V***	Power supply input for DDR Physical Interface (PHY) and IOs
VDD3V3_USBHS/FS	**3.3V**	Power supply input for USB Physical Interface (PHY) and IOs
Internally generated Power Supplies		
VDDA1V8_REG	**1.8V**	Analog Power Supply input or output, used internally for USB Physical Interface (PHY)
*VDDA1V8_DSI***		Analog Power supply input for DSI Physical Interface (PHY), to be connected to VDDA1V8_REG
VDDA1V2_DSI_REG**	**1.2V**	Analog Power supply output, used internally for DSI PLL
*VDDA1V2_DSI_PHY***		Analog Power supply input for DSI Physical Interface (PHY), to be connected to VDDA1V2_DSI_REG
VDDA1V1_REG	**1.1V**	Analog Power supply output for USB Physical Interface (PHY)

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(*) LPDDR2/LPDDR3, DDR3L and DDR3 respectively
(**) only on STM32MP157 line

The STM32MP15x microprocessor requires various dedicated power supplies to work.

- VDD has a wide range and is mostly used to supply the IOs.
- VDDCORE is the main supply for the internal logic.
- VDDA is used for the analog parts of the chip.
- VDDQ_DDR is the IO voltage for the DDR interface. This voltage depends on the selected memory type and is 1.2V for LPDDR2 or LPDDR3, 1.35V for DDR3L and 1.5V for DDR3 memories.
- VDD3V3_USBHS and USB3V3_USBFS are used to supply the embedded USB physical interface for respectively high-speed and full-speed ports.

The STM32MP15x also embeds some internal regulators to supply the USB and DSI physical interfaces.

Power Controller (PWR)

Cortex-M4 or -A7 mode	Description	Wakeup
CRun	CPU Active ➔ CPU, CPU-sub system bus matrix(s), CPU enabled peripheral clock(s) active.	-
CSleep	CPU Sleep ➔ CPU clock stopped, CPU-sub system bus matrix(s), CPU sleep enabled peripheral clock(s) active.	Any CPU Interrupt
CStop	CPU Deepsleep ➔ CPU, CPU-sub system bus matrix(s), CPU peripheral clock(s) stopped.	Depend on System mode

System mode	Description	Wakeup
Run	Clocks are active and forwarded to the system	-
Stop / Lp-Stop	Clocks are stopped. Some platform supplies are powered down (Lp-Stop). Some peripherals could request clock while in Stop / Lp-Stop	RTC/TAMP, EXTI, some peripherals, WKUP pins
LpLv-Stop	Clocks are stopped. Some platform supplies are powered down. Core voltage could be reduced	RTC/TAMP, EXTI, WKUP pins
Standby	Most platform supplies are powered down. Core supply is powered down. Backup domain may be active	RTC/TAMP, WKUP pins
Off	All Platform, Core and IOs supplies are powered down. Backup domain may be active	RTC/TAMP event could request PMIC to restore power supplies

The Core entering low power mode is controlled by software. When one Core enters CStop mode, the domain and system operating mode depend on the other Core mode.
Lp-Stop system mode could be used to control external supplies to reduce the system power.
LpLv-Stop system mode could be used to control external supplies as well as reducing the VDDCORE voltage to reduce the system power.
External power supplies are controlled using dedicated PWR_ON or PWR_LP signals in addition to some external software settings when an external Power Management IC (PMIC) is used.

Peripherals (1)

Timers	Advanced	16 bits	2
	General purpose	16 bits	8
		32 bits	2
	Basic	16 bits	2
	LP Timer	16 bits	5
	M4 Systick	24 bits	1
	A7 Timers	64 bits	4 (Secure, Non-Secure, Virtual, Hypervisor)
	RTC/AWU		1 (Securable)
	Watchdog		3 (Independent, Independent Secure, Window)
Communication Peripherals	SPI		6 (1 Securable)
		having I2S	3
	I2C (with SMB/PMB support)		6 (2 securable)
	USART (Smartcard, SPI, IrDA, LIN) + UART (IrDA, LIN)		4 + 4 (including 1 Securable USART)
	SAI		4 (up to 8 audio channels), with I²S master/slave, PCM input, SPDIF-TX
	USB	EHCI/OHCI Host	2 ports
			embedded HS PHY with BCD
		OTG HS	Yes, Embedded FS or HS PHY with BCD
		Embedded PHYs	3 (2 x High-Speed + 1 x Full-Speed)
	SPDIFRX		4 inputs
	FDCAN		2 (1 x TT-FDCAN), Clock Calibration, 10 Kbytes shared buffer
	CEC (HDMI Consumer Electronics Control)		1
	Including the following securable		1 x USART, 1 x SPI, 2 x I2C on Securable GPIOs

Boot Source

Boot Source

- All Peripherals Input/Output (when existing) are mapped through GPIO alternate functions

Not Available on all product lines or packages

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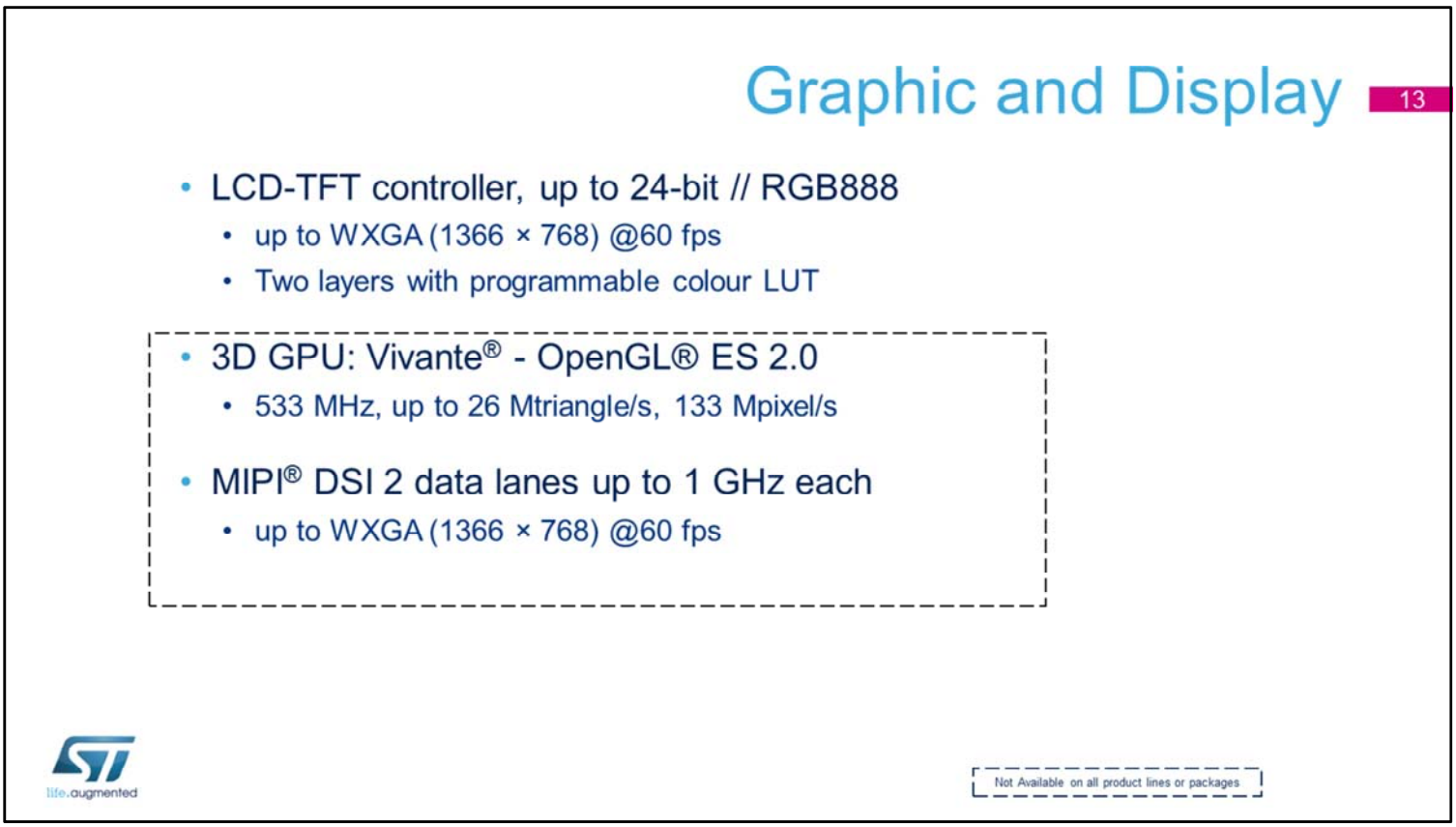
Peripherals with IOs are mapped on GPIO alternate functions (AFMUX).
Some peripherals are managed by BOOTROM and can be used as system control or program download during the initialization phase.
UART and USB are used to setup the system and/or download code into the external Flash memory.
Note that FDCAN is not available on STM32MP151 line.

Peripherals (2)

SDMMC (SD, SDIO, eMMC)		3 (8 + 8 + 4 bits), eMMC or SD	Boot Source
QuadSPI		Yes (dual-quad)	Boot Source
FMC	Parallel Address/Data 8/16-bits	4 x CS, up to 4 x 64MBytes	
	Parallel AD-Mux 8/16-bits	4 x CS, up to 4 x 64MBytes	
	NAND 8/16-bits	Yes, 1 x CS, SLC, BCH4/8	Boot Source
Gigabit Ethernet		MII, RMII, GMII, RGMII with PTP and EEE	
DMA		3 instances (1 Securable) , 48 physical channels in total	
Cryptography		DES, TDES, AES-256, dual instances (Secure and non-Secure)	
Hash		SHA-256, MD5, HMAC, dual instances (Secure and non-Secure)	
Random number generator		True-RNG, dual instances (Secure and non-secure)	
Fuses (One Time Programming)		3072 effective bits (Secure, >1500 bits available to user)	
Digital Camera Interface	bus width	8, 10, 12 or 14-bits	
GPIOs with interrupt (total count)		98, 148 or 176 depending on package	
	Securable GPIOs	8	
	Wakeup pins	4 or 6 depending on package	
	Tamper pins (Active tamper)	2 or 3 (1) depending on package	
DFSDM		8 input channels with 6 filters	
16 bit synchronized ADC		2	
	ADC channels in total	17 or 22 depending on package	
12 bit DAC		2	
Internal ADC/DAC VREF generation		1.5V, 1.8V, 2.048V, 2.5V or VREF+ input	
	VREF+ input pin	Yes	

Not Available on all product lines or packages

SDMMC can be a boot source by using either SD-Card (SDMMC1) or eMMC (SDMMC2) memory cards.
QUADSPI bank1 can be a boot source for Serial-NOR or Serial-NAND Flash memories.
FMC could be a boot source for SLC parallel-NAND Flash memories.
Cryptography is not available on STM32MP15xA devices.
Securable GPIOs are only available on STM32MP15xxAA (LFBGA448 18x18) and STM32MP15xxAC (TFBGA361 12x12) devices.



The LCD controller can provide up to WXGA @60fps (63Mpixels/s). Higher resolution are possible with reduced frame rate assuming the pixel clock remains in the allowed range.
A 3D GPU is available on STM32MP157 line and can process up to 26 Mtriangles/s or 133 Mpixels/s.
A Display Serial Interface (MIPI DSI) is available on STM32MP157 line and can provide up to WXGA @60fps (63Mpixels/s). Higher resolution are possible with reduced frame rate assuming the LTDC pixel clock and the data lane rate remain in the allowed range.

OTP Fuses

- OTP Fuses are One Time Programming memory
  - Initial bits are '0' and are irreversibly programmed to '1'
  - Incremental programing of bits in a 32-bit word is possible
- Handled thru BSEC controller IP
  - Programming, reading, status and locking handled by BSEC
  - Lock mechanism to avoid read and/or program (32-bits granularity)
- OTP Content
  - Product configuration and Trimming values set by ST during production
  - Secrets and unique identification numbers set by ST during production
  - Device configuration set by OEM (e.g. MAC address, boot source, security mode, etc...)
  - Secrets set by OEM (e.g. for secure boot)
  - Up to 1184 bits available for other OEM purposes

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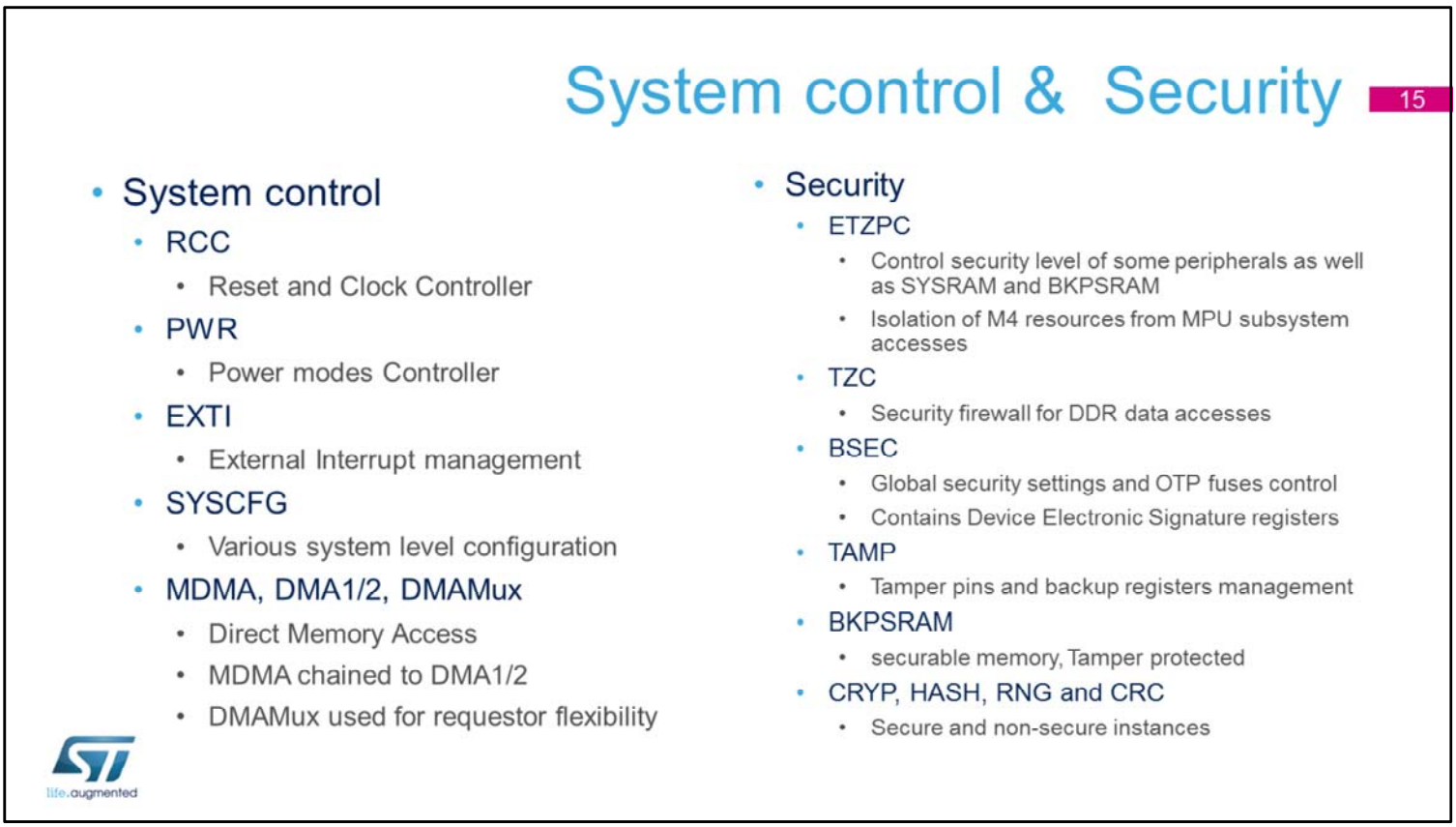
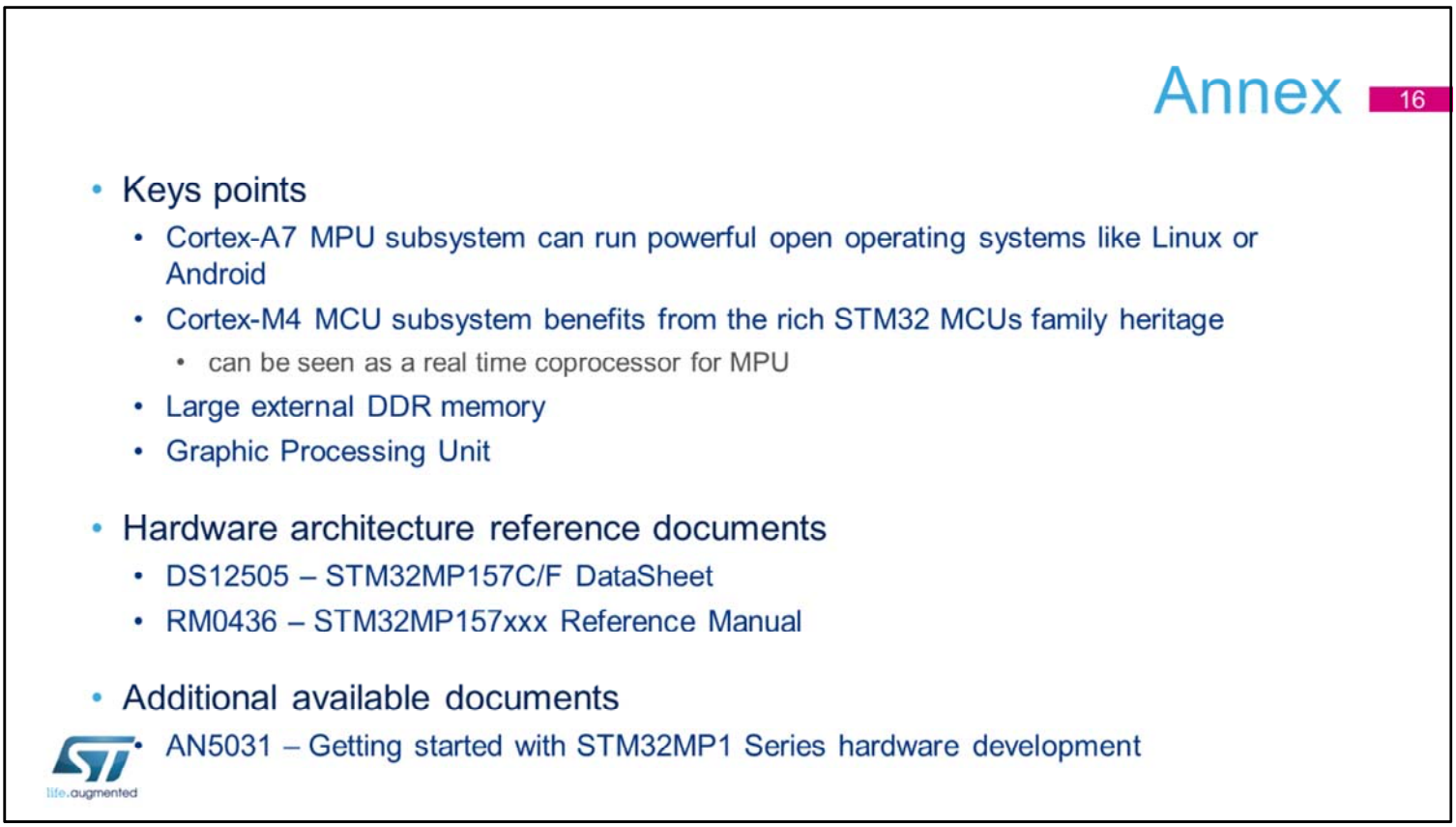
OTP fuses are memory fields which could be programmed once and then cannot be altered anymore.
The BSEC IP manages the control of the OTP fuses, including reading, programming and secure accesses.
The OTP content includes product configuration and unique numbers.
The OTP could contains OEM information such as the MAC address, secret keys or any relevant data.
Up to 1184 bits are fully available for OEM various purposes.



Various blocks are managing the transversal system control. The major ones are the Reset and Clock Controller (RCC), the power manager (PWR) which controls the system power modes.
Security is controlled by Trustzone inside the Cortex-A7 core as well as various blocks. The Enhanced TrustZone Protection Controller (ETZPC) defines which peripherals are secure or not, isolated or not.
The TrustZone Address Space Controller for DDR (TZC) blocks unwanted access to DDR data.



The main points to be noted from this presentation are:

- The STM32MP15x embeds a Cortex-A7 core able to run powerful operating systems like Linux or Android.
- The STM32MP15x embed as well a Cortex-M4 core able to run real time tasks or act as a coprocessor to reduce the Cortex-A7 load or power.
- The STM32MP15x always need an external DDR memory to run the operating system.
- The STM32MP157 Line includes a GPU which provides rich graphic capabilities for operating system.