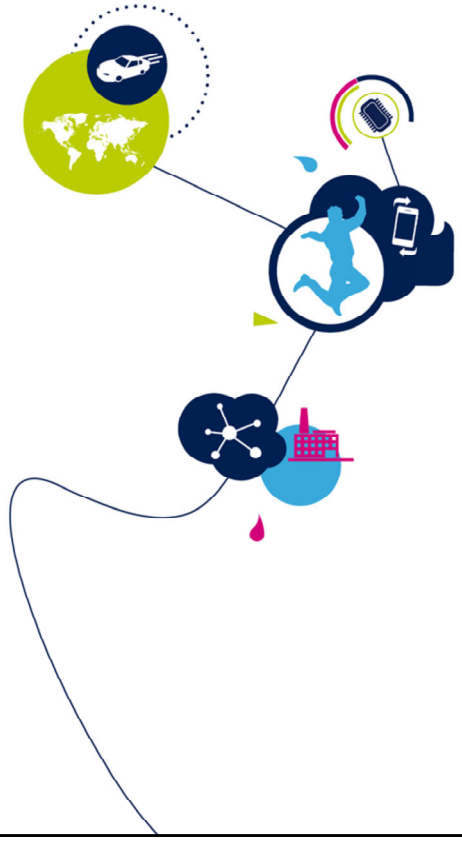
STM32WB- PWR

Power Controller

Revision 1.0



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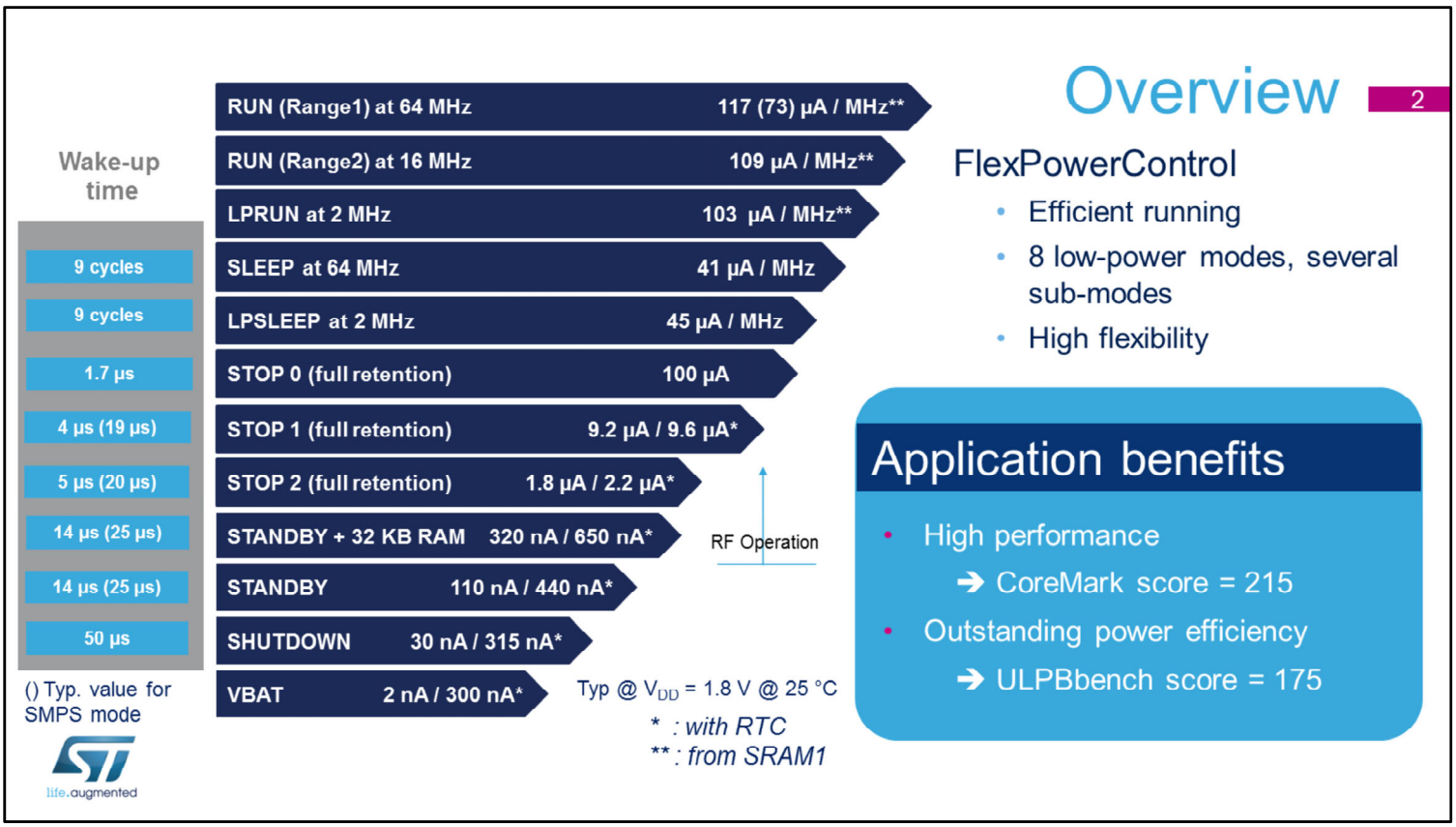
Hello, and welcome to this presentation of the STM32WB power controller. Power management functions and all power modes will also be covered in this presentation.



STM32WB devices feature FlexPowerControl, which increases flexibility in power mode management and further reduces the overall application consumption. Run mode can support a system clock running at up to 64 MHz, with only 117 µA/MHz.

STM32WB devices support 8 main low-power modes: Low-power run, Sleep, Low-power sleep, Stop 0, Stop 1, Stop 2, STANDBY with RAM retention, Standby and Shutdown SHUTDOWN modes. Each mode can be configured in many ways, providing several additional sub-modes. Note that for RF operation, the system cannot go bellow Standby with RAM retention mode as a minimum set of contexts needs to be maintained.

In addition, STM32WB devices support a battery backup domain, called VBAT.

The high flexibility in power management provides both high performance with a CoreMark score equal to 215, together with outstanding power efficiency, demonstrated by the

ULPBench score equal to 175.

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Key features

- 8 low-power modes with fast wakeup
  - Down to 30 nA with I/O wake-up
  - Down to 320 nA with 32 KB RAM retained
  - Wake-up from high number of peripherals
- Down to 77 µA/MHz in Run mode from Flash memory
- VBAT Battery backup mode with RTC and backup registers
- Flexible power distribution

Application benefits

- High flexibility to lower power consumption depending on active peripherals, required performance and needed wakeup sources
- Increased battery life
- Autonomous radio operation
- BOM cost-saving by removing external shifters and components

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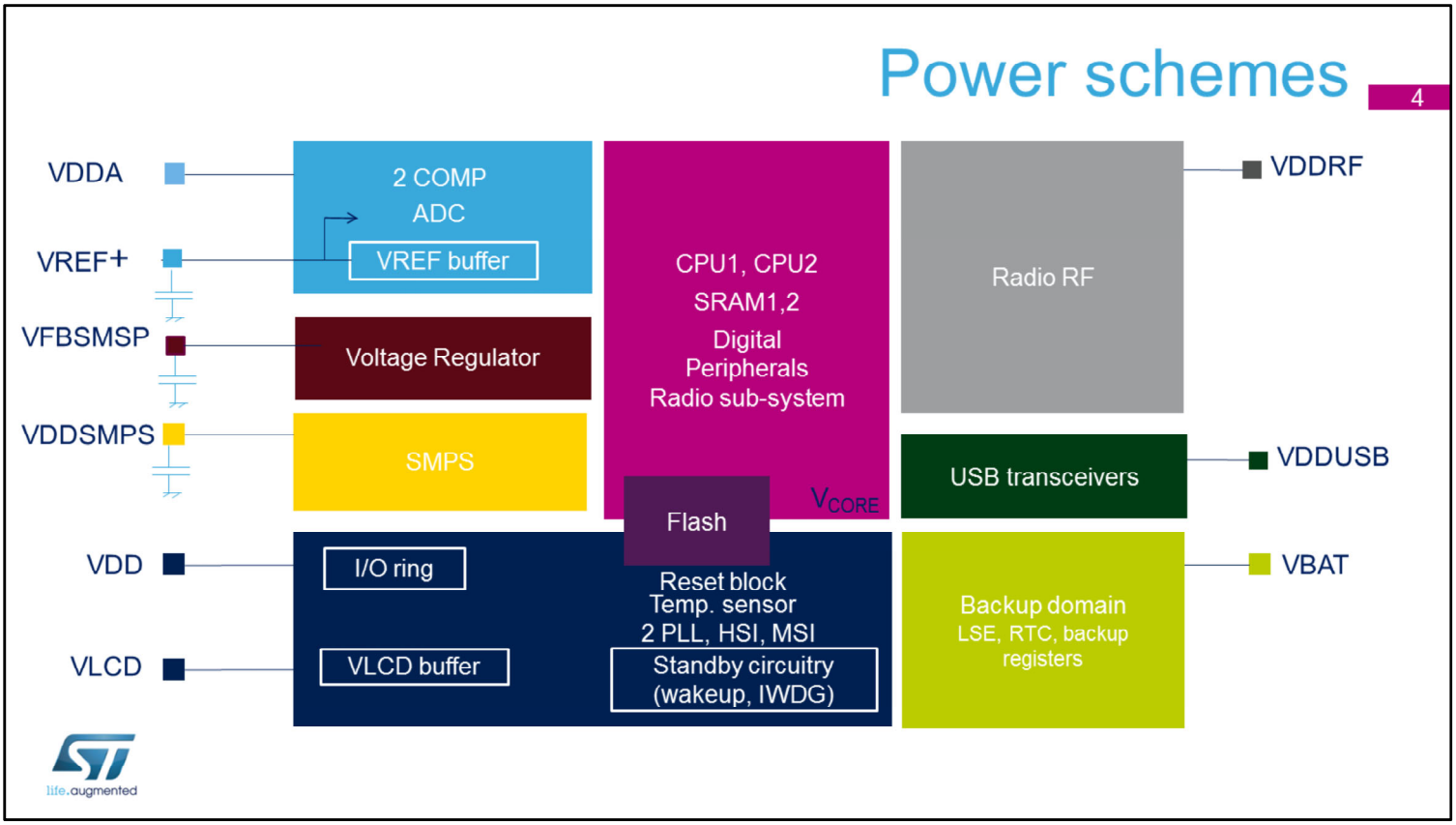
The STM32WB has several key features related to power management:
Several low-power modes, down to 30nA while it is still possible to wake up the MCU with an event on an I/O. For only 3200 nA, 32 Kbytes of SRAM can be retained. A large number of peripherals can wake up from the various low-power modes.
Dynamic consumption is down to 77 µA/MHz, executing from Flash memory.
A battery backup domain, called VBAT, including the RTC and certain backup registers.
Several power supplies are independent, allowing to reduce MCU power consumption while some peripherals are supplied at higher voltages.
Thanks to the large number of power modes, STM32WB devices offer high flexibility to minimize the power consumption and adjust it depending on active peripherals, required performance and needed wake-up sources.



STM32WB devices have several independent power supplies, which can be set at different voltages or tied together.

The main power supply is V_{DD}, supplying all I/Os, the reset block, temperature sensor and all internal clock sources. In addition, it supplies the Standby circuitry which includes the wakeup logic and independent watchdog as well as the Radio. V_{DD} is monitored by the BORS circuitry.

V_{DDSMPS} supplies the Switch Mode Power Supply step-down converter. Its output V_{FBSMPS} supplies the CPU with most of the digital peripherals and the SRAMs. The Flash memory is supplied by both V_{FBSMPS} and V_{DD}.

STM32WB features several independent supplies for peripherals: V_{DDA} for the analog peripherals, V_{DDUSB} for the USB transceiver, V_{DDRF} for the Radio.

V_{LCD} for LCD drivers, can be generated internally or come from an external supply.

The internal Reference Voltage used by analog block can be

output on VREF+ pin to supply external circuitry for the application.
A backup battery can be connected to the VBAT pin to supply the backup domain.

Improving Power Efficiently

- The SMPS is used to step down the V_{DD} supply.
- The SMPS supplies the digital core and Radio LDOs (typ.: 1.4 V)
- The SMPS mode is used when the V_{DD} supply is above the BOR[1..4] threshold.
  - Below this threshold, Bypass mode is used. Switching on the fly is supported.
  - Switch OFF is performed by HW mechanism, switching it ON should be resumed by SW.
- The SMPS will follow the device operating modes
  - Will only be ON in Run, Low-power Run, Sleep, Low-power Sleep and Stop0 modes.
  - In Stop1, 2, Standby and Shutdown modes the SMPS is automatically in Open mode.
    - When waking up it is automatically resume the mode that was used before entering.

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The SMPS supplies the digital core and radio LDOs.
The SMPS supports switching on the fly. When the VDD supply drops below 2.1 V, it automatically switches to Bypass mode.
The SMPS operating mode (on and off) will follow the device modes.
To remove any noise from the SMPS during ADC conversions, software may switch on the fly the SMPS mode.

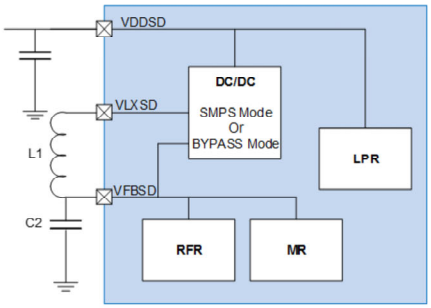
Supply configurations

Flexible selection between performance and cost

- Performance with SMPS
  - By adding an external capacitor and coil the SMPS is used to lower power consumption.
- Low cost using only LDOs.
  - By short cutting the SMPS inputs, the LDOs are directly supplied from V_{DD}. Saving the cost for a capacitor and coil to the expense of increasing the overall power consumption.

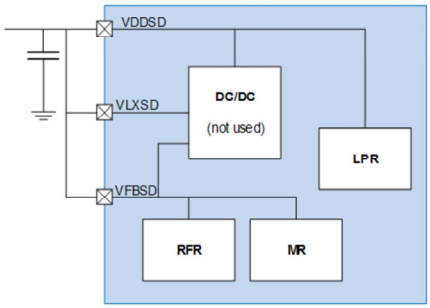
Full Vdd range [1.62..3.6V]
High efficiency SMPS (>85%)
Automatic Bypass mode when Vdd goes bellow 1.96V.

SMPS configuration



Or

LDO configuration



Full Vdd range [1.62..3.6V]
Low BOM
Low noise

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The STM32WB supply configuration is to be selected by hardware.
For the best power performance, use the SMPS configuration.
For the lowest cost, the LDO configuration can be used.

Power schemes

Optimized power and performance thanks to independent power supplies

- V_{DD} , V_{DDSMPS} and V_{DDRF} from 1.71 to 3.6 V (down to 1.6 V at power-down)
- V_{FBSMPS} from 1.4 to 3.6 V (≥1.7 V for Tx = 5.5 dBm)
- V_{DDA} from 1.62 to 3.6 V
  - 1.62 V min. when ADCs or COMPs are used
  - 2.4 V min. when VREFBUF is used
- V_{LCD} voltage for LCD from 2.5 to 3.6V, can be supplied externally or internally generated (up to 3.6V if V_{DD} > 2.0 V)
- V_{DDUSB} from 3 to 3.6 V for USB transceivers
- V_{BAT} from 1.55 to 3.6 V including the RTC and 80-byte backup registers

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The main power supply V_{DD} ensures full-featured operation in all power modes from 1.71 up to 3.6 V, allowing to be supplied by an external 1.8 V (+-5%) regulator. Device functionality is guaranteed down to 1.61 V, the minimum voltage after which a brown-out reset is generated.
RF operation is allowed in the full voltage range from 1.71 to 3.6 V.
Other independent supplies are provided to allow peripherals to operate at a different voltage.
The V_{DDSMPS} is connected to the same supply as V_{DD}.
The analog power supply V_{DDA} can be connected to any voltage other than V_{DD}. When the analog-to-digital converters or comparators are used, the V_{DDA} voltage must be greater than 1.624 V. When the voltage reference buffer is used, V_{DDA} must be greater than 2.4 V.
The LCD Voltage can be generated internally or provided externally.
The USB power supply V_{DDUSB} can be connected to any

voltage other than V_{DD}. When the USB is used, V_{DDUSB} must be greater than 3 V. Note that three IOs of Port A[13 to 11], are supplied by V_{DDUSB} independently from V_{DD}.
A backup domain is supplied by VBAT, which must be greater than 1.55 V. The backup domain contains the RTC, the 32.768-kHz LSE external oscillator and the 80-byte backup registers.

Voltage supply supervision (1/2)

Supply supervision enabling dynamic power management

- Supply voltage monitoring is provided on:
  - V_{DD} via POR/PDR, BOR (reset/switching on the fly), and PVD (threshold interrupt on AIEC).
  - V_{DDA} via PVM (threshold interrupt on AIEC)
  - V_{DDUSB} via PVM (threshold interrupt on AIEC)
  - V_{BAT} via ADC
  - V_{BKUP} monitors either V_{BAT} or V_{DD} (reset)
  - V_{FBSMPS} SMPS regulated supply, via level detector (reset).

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The power supply supervisor allows dynamic power supply management.
STM32WB devices embed power management on main V_{DD}, analog V_{DDA}, V_{BAT} supply input, Switch Mode Power Supply V_{FBSMPS}, and USB interface V_{DDUSB} supply lines.
The main V_{DD} supervision allows reset management and voltage detection via the power voltage detector (PVD) when V_{DD} crosses the selected threshold. The PVD can be enabled in all modes except Standby modes. Seven thresholds can be selected by software. The Brown-out level can be used to provide switching on the fly of the SMPS when V_{DD} drops below the threshold level.
On the analog V_{DDA} supply, a supervision circuit selected via PVM detects when V_{DDA} crosses a threshold. The PVM can be enabled in all modes except Standby modes.
On the V_{BAT} supply, a supervision circuit selected via PVM detects when V_{BAT} crosses a threshold.
On the SMPS V_{FBSMPS} supply, a supervision circuit will reset

the core when the supply is too low (<1.4 V).
On the USB interface V_{DDUSB} supply, ADC performs measurements to verify that the USB interface supply is present. The USB supply measurement can only be enabled in Run mode.

Power supply supervisor (2/2)

Safe and ultra-low-power reset management

- Brown-out reset is always enabled in all modes except Shutdown mode
  - 5 thresholds selected by option byte **BOR_LEV[2:0],** from V_{BOR0} = 1.7 V to V_{BORH4} = 2.95 V.
  - BOR1 to BOR4 can, according with option byte:
    - Ensure reset as soon as MCU drops below selected threshold, regardless of the VDD slope.
    - Or Automatically switch the SMPS in BYPASS mode if V_{DD} goes bellow the threshold.
  - BOR0 (1.7 V) is always active except in Shutdown mode. BOR0 consumption in included in all datasheet figures.
- Power voltage detector active in all modes except Standby and Shutdown
  - 7 thresholds, selectable by software

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The power supply supervisor guarantees a safe and ultra-low power reset management.
STM32WB devices embed an ultra-low-power brown-out reset (BOR) which is always enabled in all power modes except Shutdown mode. The BOR ensures reset generation as soon as the V_{DD} drops below the selected threshold, regardless of the V_{DD} slope. Five thresholds from 1.7 to 2.95 V are selected by option byte programmed in Flash memory.
A power voltage detector can generate an interrupt when V_{DD} crosses the selected threshold. The PVD can be enabled in all modes except Standby and Shutdown modes. Seven thresholds can be selected by software. In addition, an external pin can be used to compare voltages.
The BOR consumption with the 1.7 V threshold is included in the datasheet.

Peripheral voltage monitor

Supervising Power supply

- Peripheral Voltage Monitor for V_{DDA}, V_{DDUSB} = comparator vs. selected threshold, with wakeup capability from Stop modes.

PWM	Power supply	PVM threshold
PVM1	V_{DDUSB}	VPVM1: 1.22 V
PVM3	V_{DDA}	VPVM3: 1.65 V

- By default, independent power supplies are electrically isolated and the peripherals/IO powered by them are not available. The power isolation must be removed by SW.

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The STM32W MCU embeds four Peripheral Voltage Monitors to detect if the independent supply is present or not. These comparators have wake-up from Stop mode capability. The PVM1 compares the V_{DDUSB} voltage with the 1.22 V threshold. The PVM3 compares the VDDA voltage with the 1.65 V threshold, intended for the comparators and analog-to-digital converters. The PVM2 and PVM4 are reserved.

To guarantee any of the supply sequences on the application, power isolation has been implemented and is active by default. It is the role of software to enable the needed supplies by removing the power isolation.

Independent voltage reference supplies for analog performance

- VREF+: reference voltage for ADC
  - It can be provided either by an external reference voltage or by the internal voltage reference buffer.
  - VREF+ pin, and thus the internal voltage reference, is not available on the 48-pin package. On this package, this pin is double-bonded with V_{DDA} which can be connected to an external reference or V_{DD}. The internal voltage reference buffer is not available and must be kept disabled.
- The application SW can decide to place the SMPS in Bypass mode when performing ADC conversion to reduce noise. SMPS mode change can be done on the fly.

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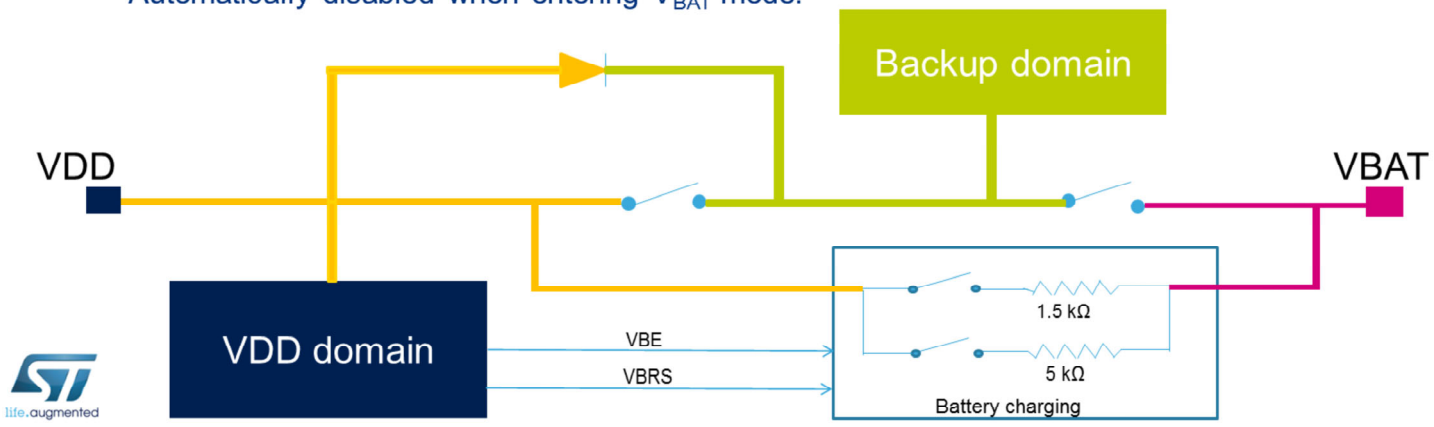
The ADC and DAC voltage references can be provided either by an external supply voltage or by the internal reference buffer. This allows improvement of the converters performance by providing an isolated and independent reference voltage. The VREF+ pin and thus the internal voltage reference, is not available on the 48-pin package. In this package, the VREF+ is double-bonded with VDDA and the internal voltage buffer must be kept disabled. The voltage reference can be provided through the VDDA pin in this package.
The application software can decide to place the SMPS in Bypass mode when performing ADC conversion to reduce noise.

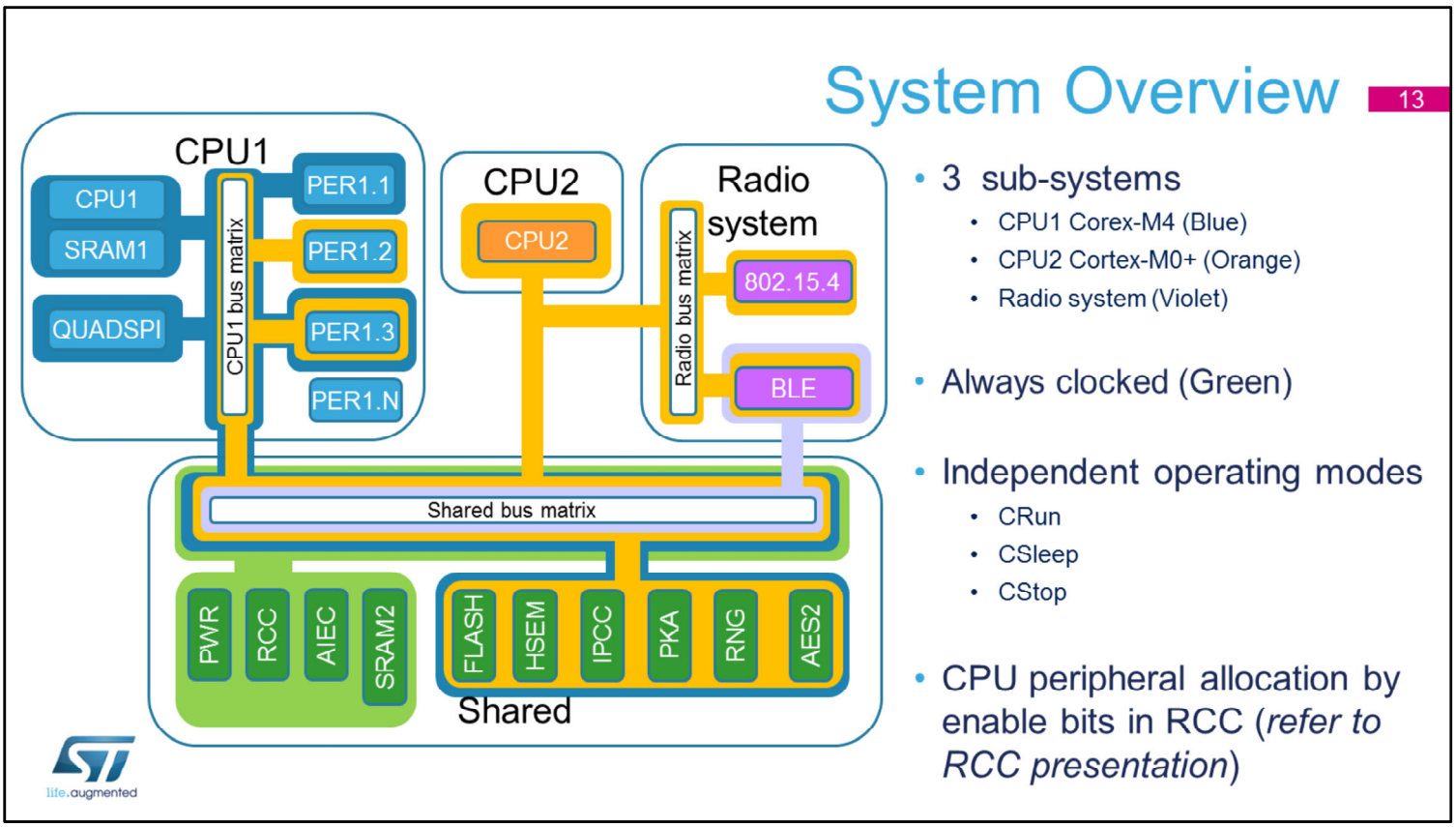
V_{BAT} battery charging

Time Keeper operation

- A backup battery connected to V_{BAT} can be charged from V_{DD}.
  - Enabled by application Software
  - Selection between 2 charging resistor values (5 kOhm, 1.5 kOhm)
  - Automatically disabled when entering V_{BAT} mode.



The battery charging feature allows to charge a super-cap connected to VBAT pin through internal resistor when V_{DD} supply is present. The charging is enabled by software and is done either through a 5 kOhm or 1.5 kOhm resistor depending on software. Battery charging is automatically disabled in VBAT mode.



The STM32WB system contains three sub-systems. The CPU1 Cortex-M4, the CPU2 Cortex-M0+, and the Radio sub-system. Each of the three sub-systems can operate independently being in one of its operating modes CRun, CSleep, or CStop. Peripherals will only be clocked when the associated sub-system is in CRun mode, or CSleep when enabled in Sleep mode. The system resources such as RCC, PWR, AIEC and SRAM2, connected on the Shared bus will always be clocked when the system is in Run mode. The other peripherals on the Shared bus may be enabled to operate with CPU1 and/or CPU2. The SRAM1 and QSPI peripherals on the CPU1 bus matrix can only be associated with the CPU1 processor. The other CPU1 bus matrix peripherals may be enabled to operate with CPU1 and/or CPU2. The Radio system bus matrix can only be associated with the CPU2 processor. The Radio system BLE peripheral may operate when both CPUs are in CSleep and CStop mode, in this case only the system resources on the Shared

bus are clocked.

CPU sharing Power modes

Automatic Power mode management

- Each CPU can decide independently which low-power mode to use (STOP0, STOP1, STOP2, STANDBY, or SHUTDOWN).
- Each CPU can decide which IT source or RTC, RF (CPU2 only), GPIO signal, will wake it up.
- When both CPUs enter WFI (or WFE) the HW mechanism executes the compatible request. It select the highest low-power mode compatible with the two CPU requirements.
- One CPU can wake up without the need to wake up the other one.
  - When the STM32WB wakes up from StopX modes, according the Interruption source, only the CPU registered for this IT source is restarted, the other one stays in WFI (or WFE) with its clock stopped.
  - When the STM32WB wakes up from STANDBY modes, according with the source, only the CPU registered for this source is restarted, the other one stays under Reset mode.

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Each CPU can decide independently which low-power mode to use (Stop 0, Stop 1, Stop 2, Standby, or Shutdown).
Each CPU can decide which IT source or RTC, RF (CPU2 only), GPIO signal, will wake it up.
When both CPUs enter WFI (or WFE), the hardware mechanism executes the compatible request. It selects the highest low-power mode compatible with the requirements for both CPUs.
One CPU can wake up without the need to wake up the other one if not required.
When the STM32WB wakes up from Stop x modes, according with the Interruption source, only the CPU registered for this IT source is restarted, the other one stays in WFI (or WFE) with its clock stopped.
When the STM32WB wakes up from Standby modes, in accordance with the source, only the CPU registered for this source is restarted, the other one stays under Reset mode.
Run mode (Run Range 1, Run Range 2 and Low Power

Run) and Frequency selection changes are centralized on one of the CPUs to avoid conflicting configurations. This includes selection of the System clocks as well as LP enable and Voltage Range and Flash Memory configurations.

Radio power modes

Automatic Power mode management

- The Radio can autonomously enter and exit low-power modes.
- The Radio low-power timer will wake it up.
- When both CPUs and the Radio are all in CStop mode, the system will enter Stop, Standby or Shutdown mode as selected by the CPUs.
- The Radio can wake up from Stop and Standby modes without the need of the CPUs.

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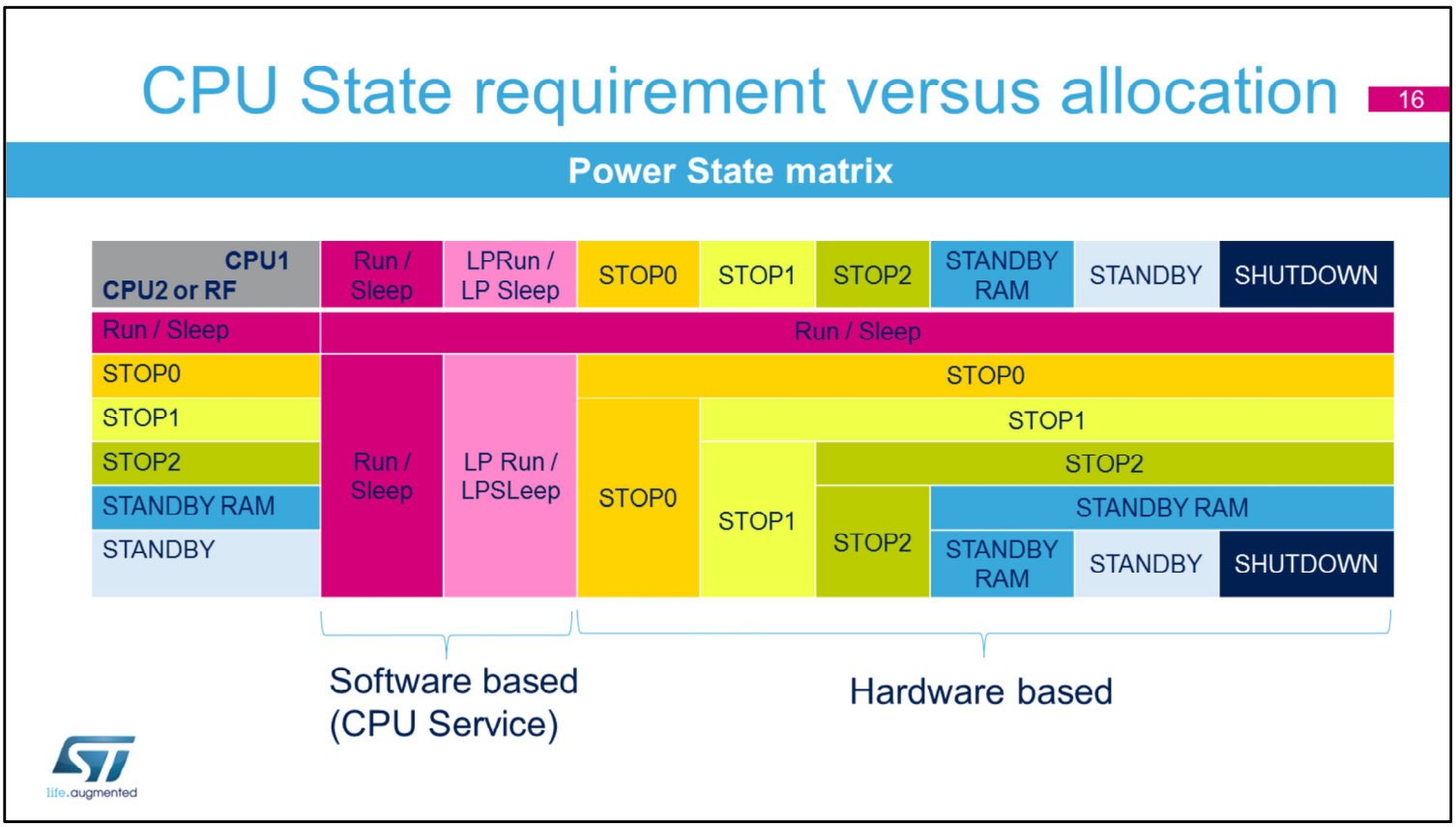
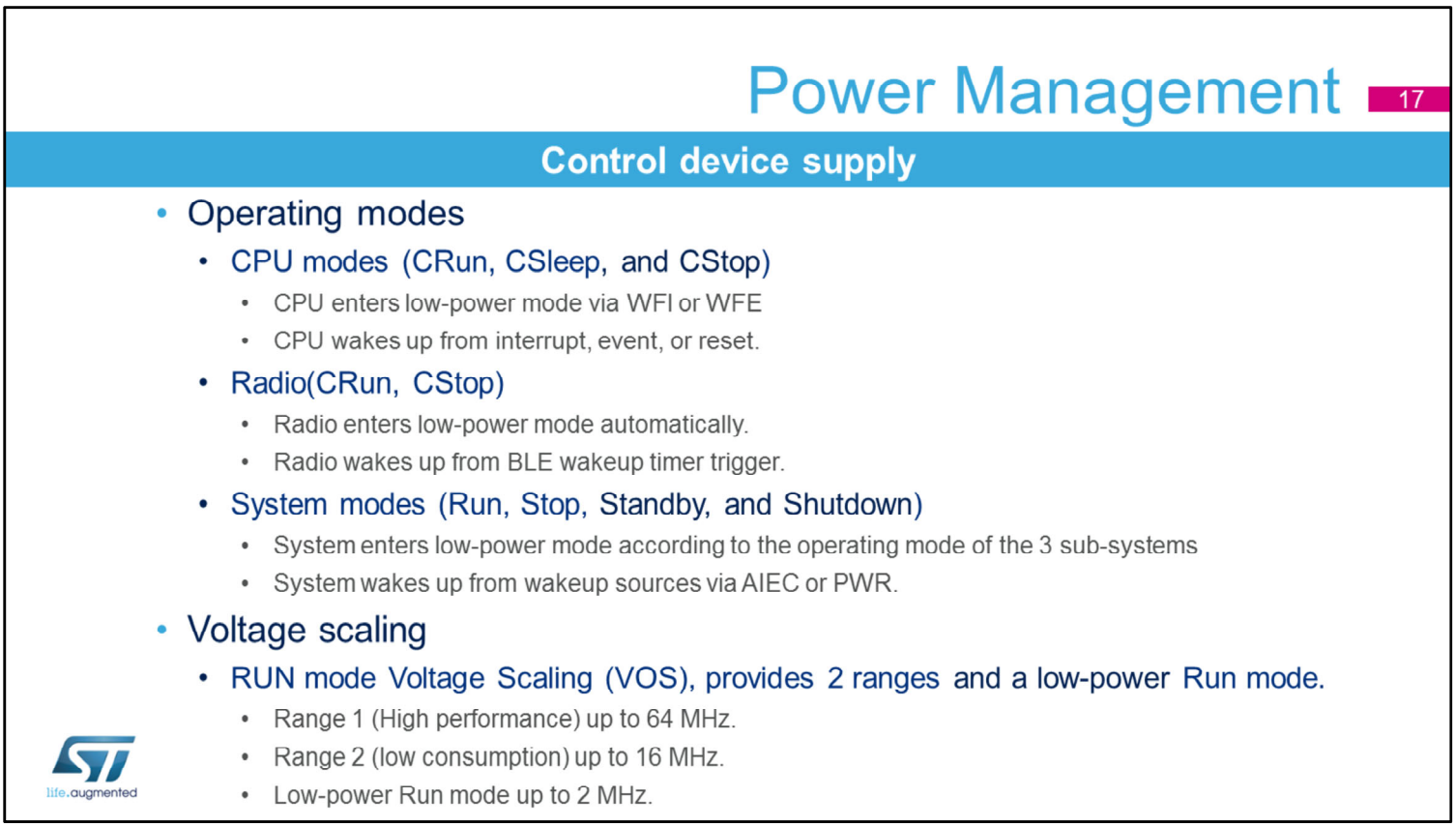
Each Radio sub-system operates autonomously and will enter and exit low-power modes on its own.
The Radio low-power timer is the wakeup source for the Radio sub-system.
When both CPUs and the Radio sub-system are in CStop mode, the system will enter the low-power mode as selected by the CPUs.

CPU State requirement versus allocation



According to the requirements of the CPU1, CPU2 and RF systems, the PWR Hardware mechanism manages how the STM32WB reaches a given state. That is to say, when CPU1 allows Standby mode and CPU2 allows only Stop2 mode, the system enters Stop2 mode.
Note that only the CPUs can place the system in LP Run or LP Sleep modes. The Radio does not support Shutdown mode and must be disabled prior to entering Shutdown mode.



Power management allows to control the device power supply based on system operating mode. The system operating mode depends on the individual CPUs and Radio operating modes. The system is in Run mode whenever one of the 3 sub-systems is in CRun or CSleep mode. The system enters Stop or Standby modes when all three sub-systems are in CStop mode.
In system Run mode, the device power supply can be scaled according to the required performance: Up to 64 MHz in Range 1, 16 MHz in range 2, and only up to 2 MHz in low-power Run mode.

CPU entering CStop

- When a CPU enters Cstop mode
  - the CPU clock domain may be clocked when the other CPU is in CRun or CSleep mode and has allocated peripherals.
  - the System may
    - stay in Run mode when the other domain CPU or the Radio system stay in CRun or Csleep mode, or a wakeup source remains active
    - enter Stop mode
    - enter Standby mode when allowed by both CPUs.
- The system operating mode depends on both CPUs and the Radio system.

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A CPU enters the CStop mode when executing a Wait for Interrupt (WFI) or Wait for Event (WFE) with the DEEPSLEEP bit set. The system state also depends on the operating modes of the other CPU and the radio system. The CPU1 bus matrix clock is only stopped when the other CPU has no allocated peripherals on the CPU1 clock domain or the other CPU is also in CStop mode. The system may only enter Stop or Standby mode when both the other CPU and the radio system are in CStop mode. The system only enters Standby mode when allowed by both CPUs.

CPU wakeup from CStop

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- To determine the system low-power mode when the CPU wakes up from CStop mode, flags are provided.
- Each CPU has its own set of flags
  - CxSTOPF
    - System has woken up from STOP mode
      - Wakeup interrupt to the CPU will be pending in AIEC or peripheral
  - CxSBF
    - System has woken up from STANDBY mode
      - CPU start from reset, there is no wakeup interrupt pending in the AIEC.
- The flags of both CPUs must be checked to determine the system operating mode.

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When a CPU wakes up from its CStop mode, it has to know from which mode the domains and system have woken up. For this, the CPU has a few dedicated flag bits SBF_D1, SBF_D2, SBF and STOPF. These bits inform the CPU about the state of the system, and which parts (clock, peripherals) may need to be reinitialized.

Wakeup system mode detection

System mode	C1SBF	C1STOPF	C2SBF	C2STOPF	CPU1 wakeup
Run	0	0	x	x	Wakeup from Run
	0	1	0	0	Wakeup from Stop, but system is already in Run due to CPU2.
	1	0	0	0	Wakeup from Standby, but system is already in Run due to CPU2.
	1	1	0	0	Wakeup from Stop, preceded by Standby, but system is already in Run.
Stop	0	1	x	1	Wakeup from Stop. (CPU2 is still in CStop)
	1	1	0	1	Wakeup from Stop, preceded by Standby. (CPU2 is still in CStop)
Standby	1	0	1	0	Wakeup from Standby. (CPU2 is still in CStop)

For example, if CPU1 has selected to enter Stop mode:
- but when it wake up, it reads C1STOPF=0, it means it never entered in System STOP, and so there is no need to re-initialize some peripherals (PLL..),
- if it reads C1STOPF=1 and C2STOPF=0, it means that it has entered System STOP but that CPU2 has woken up the system in the mean time (and has probably re-initiated some peripherals)

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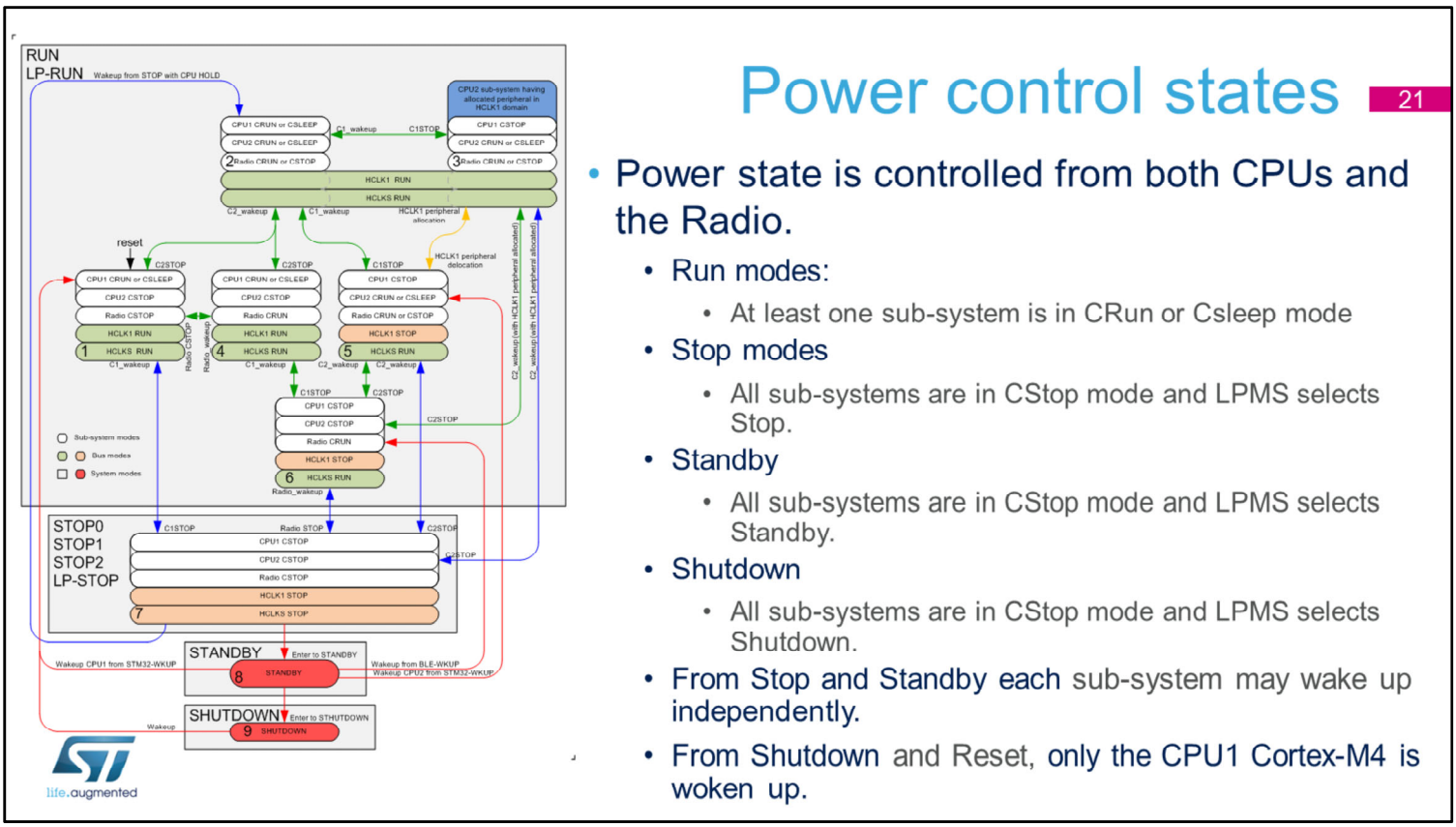
These CxSBT (Standby) and CxSTOPF (Stop) flags have to be tested by the CPU software when waking up from Stop or Standby modes. They enable the CPU1 application to selectively reprogram its context (RAM, Peripherals and Clocks).



Power control states

- Power state is controlled from both CPUs and the Radio.
  - Run modes:
    - At least one sub-system is in CRun or Csleep mode
  - Stop modes
    - All sub-systems are in CStop mode and LPMS selects Stop.
  - Standby
    - All sub-systems are in CStop mode and LPMS selects Standby.
  - Shutdown
    - All sub-systems are in CStop mode and LPMS selects Shutdown.
  - From Stop and Standby each sub-system may wake up independently.
  - From Shutdown and Reset, only the CPU1 Cortex-M4 is woken up.

This figure gives the complete overview of the power modes in relation to the CPUs and Radio operating modes. Whenever a sub-system is in CRun or CSleep mode, the system is in Run mode. Low-power Stop, Standby and Shutdown modes are only entered when all three sub-systems are in CStop mode. The low-power mode is selected by the Low-Power Mode Select (LPMS) bits. Each CPU has its own Low-Power Mode select bits and the system enters the highest consuming low power mode selected. From Stop and Standby modes, each sub-system can be awakened independently by its own enabled wakeup sources. From Shutdown mode and Reset, only the CPU1 Cortex-M4 is awakened. It is up to the Cortex-M4 application software to wake up the CPU1 Cortex-M0+ and the Radio sub-system.

Run and Low-power run modes

Flexibility between required performance and consumption

- Each peripheral clock can be configured to be ON or OFF
  - After reset, all peripheral clocks are OFF, except the Flash interface clock
  - SRAM1 and SRAM2 clocks are always ON in Run mode
- When running from SRAM1 (CPU1 Only) or SRAM2; in Low-power run:
  - Flash memory can be put in Power-down mode (if none of the CPUs are using it)
  - Flash memory clock can be switched off
  - Interrupt vectors must also be re-mapped to SRAM

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Each peripheral clock can be configured to be ON or OFF in Run and Low-power run modes. By default, all peripherals clocks are OFF, except the Flash interface clock. The SRAM1 and SRAM2 clocks are always ON in Run mode. When running from SRAM1 or SRAM2 (in Low-power run mode), the Flash memory can be put in Power-down mode thanks to software, and the Flash clock can be switched off. The Flash memory must not be accessed when it is switched off, consequently interrupts must be mapped in SRAM, using the CPU Vector Table Offset Register.

PWR interrupts

Interrupt event	Description	Availability
WKUP[5:1]	External wakeup to GPIO Wakeup pins.	Run, Stop and Standby
PVDO	Programmable Voltage detection via AIEC	Run and Stop
PVMO[3,1]	Peripheral Voltage monitoring via AIEC	Run and Stop
CPU2 Hold	CPU1 wakeup to re-initialize system before releasing CPU2	Stop and Standby
Critical Radio Phase	End of critical Radio phase.	Run
BLE activity	End of BLE Radio activity.	Run
802.15.4 activity	End of 802.15.4 Radio activity.	Run

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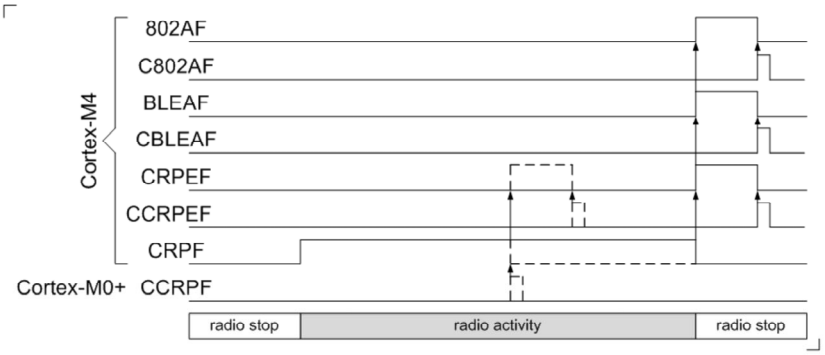
Here is a summary of the PWR control related interrupts.

Real-time radio information

Interrupts generated by the radio sub-system

- The Application can get real-time radio information from the PWR
  - Radio critical phase active with critical phase end interrupt (PWR_EXTSCR.CRPF, PWR_SR1.CRPEF)
  - Radio BLE activity end interrupt (PWR_SR1.BLEAF)
  - Radio IEE802.15.4 activity end interrupt (PWR_SR1.802AF)



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Radio activity flags and interrupts are available to the Cortex-M4 and may be used to control the radio's real-time operation, i.e. to prevent Flash memory operations from being executed during the radio's critical phase.

Run and Low-Power run modes

Flexibility between required performance and consumption

Voltage range	CPU	HCLK1 HCLK2	MSI	HSI	PLL
Range 1	CPU1 CPU2	64 MHz max 32 MHz max	48 MHz range	16 MHz	64 MHz VCO max = 344 MHz
Range 2	CPU1 CPU2	16 MHz max 16 MHz max	24 MHz range	16 MHz	16 MHz VCO max = 128 MHz
Low-power run	CPU1 CPU2	2 MHz max 2 MHz max	2 MHz range	Allowed	Not allowed

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The Run mode, thanks to voltage scaling, and the Low-power run modes offer flexibility between required performance and consumption.
In Run mode range 1, the system clock is limited to 64 MHz and the internal and external oscillators and the PLL can be used. In Run mode range 2, the system clock is limited to 16 MHz and the internal and external oscillators as well as the PLL can be used, but must be limited to 16 MHz. In Low-power run mode, the system clock must be limited to 2 MHz.

Sleep and Low-power sleep modes

All peripherals available and fastest wakeup time

- Core is stopped, each peripheral clock can be gated ON or OFF
- Entered by executing WFI (Wait For Interrupt) or WFE (Wait For Event)
- Two mechanisms to enter this mode:
  - Sleep Now: MCU enters Sleep mode as soon as WFI/WFE instruction are executed
  - Sleep on Exit: MCU enters Sleep mode as soon as it exits the lowest priority ISR
    - The stack is not popped before entering Sleep mode, it will not be pushed when the next interrupt occurs, saving running time.
  - Controlled by Cortex System Control Register [SLEEPONEXIT]

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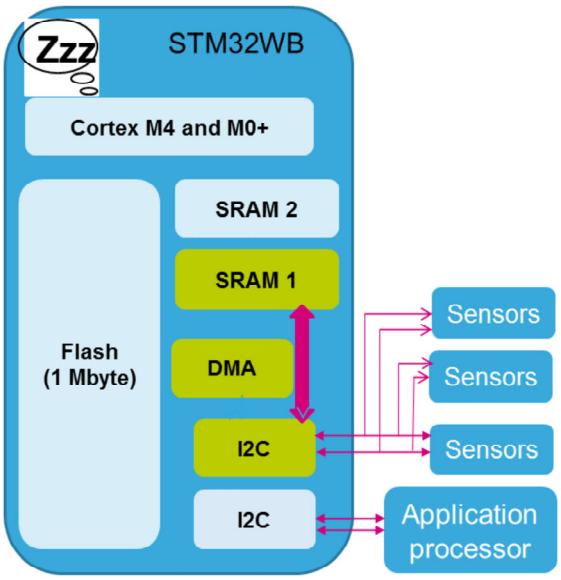
Sleep and Low-power sleep modes allows all peripherals to be used and features the fastest wakeup time.
In these modes, the CPU is stopped and each peripheral clock can be configured by software to be gated ON or OFF during the Sleep and Low-power sleep modes.
These modes are entered by executing the assembler instruction Wait for Interrupt (WFI) or Wait for Event (WFE).
When executed in Low-power run mode, the device enters Low-power sleep mode.
Depending on the SLEEPONEXIT bit configuration in the Cortex M4 System Control Register, the MCU enters Sleep mode as soon as the instruction is executed, or as soon as it exits the lowest priority Interrupt Sub Routine. This last configuration allows you to save time and consumption by saving the need to pop and push the stack.

Batch Acquisition Mode (BAM)

Optimized mode for transferring data with communication peripherals, while the rest of the device is in low-power mode.

1. Only the needed communication peripheral + 1 DMA + 1 SRAM are configured with clock enabled in Sleep mode
2. When both CPU are in Sleep mode, the Flash memory is put in Power-down mode and Flash memory clock is gated off during Sleep mode
3. Enter either Sleep or Low-power sleep mode
   - Note that the I2C clock can be at 16 MHz even in Low-power sleep mode, allowing 1 MHz Fast-mode Plus support. U(S)ART/LPUART clock can also be HSI.



Batch Acquisition Mode is an optimized mode for transferring data.
Only the needed communication peripheral + 1 DMA + SRAM1 or SRAM2 are configured with clock enable in Sleep mode.
Flash memory is put in Power-down mode and the Flash memory clock is gated off during Sleep mode.
Then it can enter either Sleep or Low-power sleep mode.
Note that the I2C clock can be at 16 MHz even in Low-power sleep mode, allowing support for 1-MHz Fast-mode Plus.
The USART and LPUART clocks can also be based on the high-speed internal oscillator. Typical applications are sensor hubs.

Stop modes

Lowest power modes with full retention

- All memory and all peripheral registers are retained
- All high-speed clocks are stopped
  - Except the HSI used as kernel clock for peripherals capable of operating in Stop mode.
- LSE (32.768 kHz external oscillator) and LSI (32 kHz internal oscillator) can be enabled
- Several peripherals can be active and wake up from Stop modes
- System clock at wakeup can be HSI or MSI up to 48 MHz (1 µs wakeup time on RAM, 5 µs on Flash memory, add +10 µs when SMPS is used)
- Stop 2 consumption is lower, Stop 1 and 0 supports more active peripherals

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STM32WB devices features three Stop modes: Stop 0, Stop 1, and Stop 2, which are the lowest power modes with full retention and fast wakeup time to Run mode at maximum 48 MHz.
The contents of SRAMs and all peripherals registers are preserved in all Stop modes.
All high-speed clocks are stopped, except the ones used as kernel clock for peripherals capable of operating in Stop modes.
The 32.768 kHz external oscillator and 32 kHz internal oscillator can be enabled.
Several peripherals can be active and wake up from Stop mode.
System clock on wake-up can be the internal high-speed and multi-speed oscillators up to 48 MHz, with only a 1 µs wakeup time from SRAM or 5 µs from Flash memory; add +10 µs when SMPS is used.
Stop 2 consumption is lower than Stop 1 and 0, but supports

less active wakeup peripherals.

Stop mode comparison

Voltage range	Stop 0	Stop 1	Stop 2
Consumption	25 °C, 3 V		
	100µA	9.2 µA w/o RTC	1.8 µA w/o RTC
Wakeup time to 32 MHz (1)	1.7 µs in Flash memory 2 µs in RAM	4.7 µs in Flash memory 3.4 µs in RAM	5.1 µs in Flash memory 5 µs in RAM
Wakeup clock	MSI configurable up to 48 MHz or HSI at 16 MHz		
Regulator	Main regulator	Low power regulator	
Peripherals	RF IP, RTC, I/Os, BOR, PVD, PVM, IWDG		
	USB (suspend, ADP) 2 LP TIMERs 1 LP UART (Start, address match or byte reception) UART (Start, address match or byte reception) 2 I2C (address match)		1 LP TIMER (LPTIM1) 1 LP UART (Start, address match or byte reception) 1 I2C (I2C3) (address match)

(1) Add 10µs typical for wakeup time when using SMPS mode

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When comparing Stop modes:
Stop 0 mode has the highest consumption as it keeps the Main Regulator ON.
Stop 1 mode consumption is higher than Stop 2 mode consumption, but the wakeup time is shorter and the number of active peripherals is higher.
It is possible to wake up from Stop 0 or 1 mode with the USB Resume from Suspend event or with Attach Detection, but it is not supported in Stop 2 mode.

The I2C address recognition is functional in both Stop modes, and can generate a wakeup event in case of an address match. Only 1 I2C is supported in Stop2 versus 2 I2Cs in other Stop modes.
The UART byte reception is functional in both Stop modes and can generate a wakeup event in case of Start detection or Byte reception or Address match event. Only the low-power UART is supported in Stop2 mode. In other Stop

modes, all UARTs and the low-power UART can generate a wakeup event.
When clocked by the internal or external low-speed oscillator, or when clocked by an external pin, the low-power timer can wake up the MCU with all its events. In Stop 0 and Stop 1 modes, both low-power timers are supported whereas only LPTIM1 is supported in Stop 2 mode.

Stop hold mode

Allows the CPU1 to re-initialize the clock system.

- When waking up from Stop modes, the clock system is reset.
- The Stop Hold function allows the CPU1 to re-initialize the clock system.
  - A wake-up interrupt to the CPU2 holds the CPU2 and issues a wake-up hold interrupt to the CPU1.
  - The CPU1 after having re-initialized the clock system removes the hold on the CPU2.

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To allow the CPU1 to re-initialize the clock system when exiting from Stop modes, the Stop hold function holds the CPU2 until the CPU1 has re-initialized the system. To ensure this, a wake-up from Stop mode interrupt holds the CPU2 and wakes up the CPU1 with a wake-up hold interrupt. Once the CPU1 has re-initialized the system, it releases the CPU2 hold.

Standby mode

Lowest power mode with SRAM2 retention, switch to V_{BAT} and I/O control

- RTC and 80-byte backup registers always retained.
- Possibility to retain 32 Kbytes of SRAM2a
- Wakeup sources:
  - Radio IP (wakeup CPU2 only)
  - RTC (both CPU)
  - 5 wakeup pins: the polarity of each of the 5 wakeup pins is configurable (both CPU)
- Ultra Low Power BOR0 always ON: safe reset regardless of V_{DD} slope.
- Configurable pull-up or pull-down or none for each I/O

  PWR_PUCRx / PWR_PDCRx registers (x = A,B,…H), applied when APC is set in PWR_CR3 register

  => Allows to control external component inputs state
- Wakeup clock is HSI at 16 MHz.

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The Standby mode is the lowest power mode in which 32 Kbytes of SRAM2 can be retained, the automatic switch from V_{DD} to V_{BAT} is supported and the I/Os level can be configured by independent pull-up and pull-down circuitry. By default, the voltage regulators are in Power down mode and the SRAMs and the peripherals registers are lost. The 80-byte backup registers are always retained.

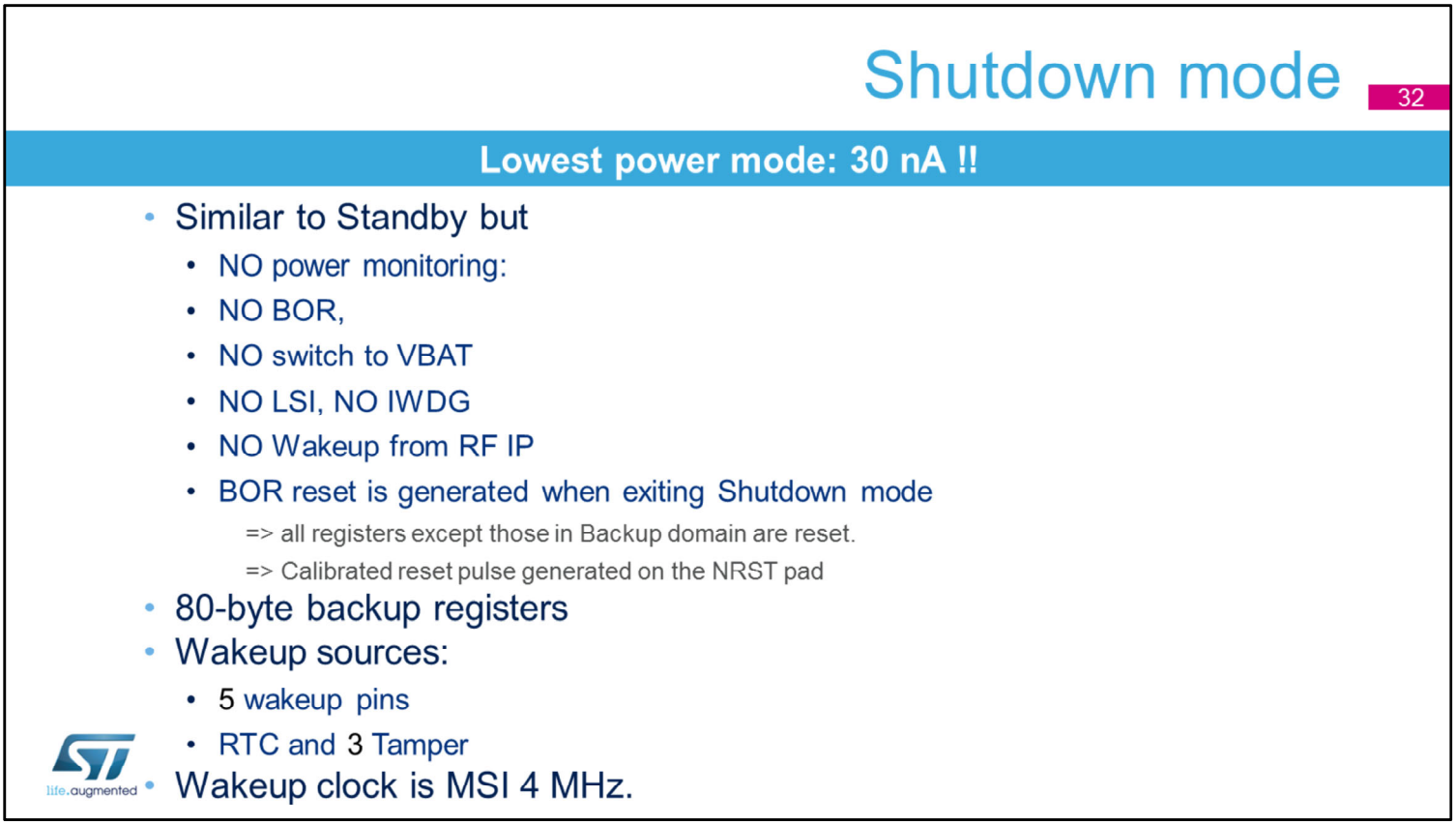
The ultra-low-power brown-out reset is always ON to ensure a safe reset regardless of the V_{DD} slope.

Each I/O can be configured with or without a pull-up or pull-down, which is applied and released thanks to the APC control bit. This allows control of the inputs state of external components even during Standby mode.

The Radio IP can wake up the CPU2.

Five wakeup pins are available to wake up both CPUs from Standby mode. The polarity of each of the five wakeup pins is configurable.

The wakeup clock is HSI with a frequency of 16MHz.



Shutdown mode is the lowest power mode of the STM32WB, with only 30 nA at 1.8 V.
This mode is similar to Standby mode but without any power monitoring: the brown-out reset is disabled and the switch to V_{BAT} is not supported in Shutdown mode.
The LSI is not available, and consequently the independent watchdog is also not available. A brown-out reset is generated when the device exits Shutdown mode: all registers are reset except those in the backup domain, and a reset signal is generated on the pad.
The 80-byte backup registers are retained in Shutdown mode.
The wakeup sources are the 5 wakeup pins and the RTC.
When exiting Shutdown mode, the wakeup clock is MSI at 4 MHz.

VBAT mode

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RTC still running and backup registers preserved in case of V_{DD} loss

- Backup domain contains:
  - RTC clocked by 32.768 kHz LSE oscillator
  - 3 tamper detection pins with time-stamping to detect intrusion
  - 80 bytes backup registers
- If V_{BAT} goes below the V_{BKUP} threshold, the backup domain is reset
- Automatic internal switch between V_{BAT} and V_{DD} when V_{DD} is powered down and powered up.

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The backup domain allows us to keep the RTC functional and to preserve the backup registers in case the V_{DD} supply is down, thanks to a backup battery connected to the VBAT pin.
The backup domain contains the RTC clocked by the low-speed external oscillator at 32.768 kHz. Three tamper pins are functional in VBAT mode, and will erase the 80-byte backup registers also included in the VBAT domain, in case of intrusion detection.
The backup domain also contains the RTC clock control logic.
In case V_{DD} drops below a certain threshold, the backup domain power supply automatically switches to V_{BAT}. When V_{DD} is back to normal, the backup domain power supply automatically switches back to V_{DD} .
The V_{BAT} voltage is internally connected to an ADC input channel in order to monitor the backup battery level.
When V_{DD} is present, the battery connected to V_{BAT} can be

charged from the V_{DD} supply.

Power modes summary

Mode	Regulator	RF	CPU	Flash	SRAM	Clocks	Peripherals
Run	R1	YES	**Yes**	**ON**	**ON**	Any	All
	R2	no					All except USB, RNG, RF
LPRun	LPR	no	**Yes**	**ON**(1)	**ON**	Any except PLL	All except USB, RNG, RF
Sleep	R1	YES	No	**ON**	**ON**(2)	Any	All Any IT or event
	R2	no					
LPSleep	LPR	no	No	**ON**(1)	**ON**(2)	Any except PLL	All except USB, RNG, RF Any IT or event
Stop 0	R1/R2	YES	No	OFF	**ON**	LSE/LSI	Reset pin, all I/Os BOR,PVD,PVM,RTC,IWDG, USARTx, LPUART,I2Cx,LPTIMx, USB
Stop 1	LPR	YES	No	OFF	**ON**	LSE/LSI	Reset pin, all I/Os BOR,PVD,PVM,RTC,IWDG, USARTx, LPUART,I2Cx,LPTIMx, USB
Stop 2	LPR	YES	No	OFF	**ON**	LSE/LSI	Reset pin, all I/Os BOR,PVD,PVM,RTC,LCD,IWDG, LPUART,I2C3,LPTIM1
Standby + RAM	LPR	YES	DOWN	OFF	**SRAM2a**	LSE/LSI	RF IP, Reset pin, 5 WKUPx pins BOR, RTC, IWDG
Standby	OFF	no			**DOWN**		
Shutdown	OFF	no	DOWN	OFF	**DOWN**	LSE	Reset pin, 5 WKUPx pins, RF RTC

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Here you can see the summary of all the STM32WB power modes.

Option bytes

Avoiding entering unwanted low power modes

- 3 option bits can be configured in Flash options bytes to prohibit a given low-power mode:
  - nRST_SHDWN: When cleared, a reset is generated when entering Shutdown mode
  - nRST_STDBY: When cleared, a reset is generated when entering Standby mode
  - nRST_STOP: When cleared, a reset is generated when entering any Stop modes

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Three bits are available in the Flash option bytes to prohibit a given low-power mode. When cleared, an option bit configures reset generation when entering Shutdown mode. Another bit configures reset generation when entering Standby mode and the last bit configures reset generation when entering Stop 1 or Stop 2 modes.
One bit is used to configure the behavior of the BORHx threshold, either as a reset (as in STM32L4 family) or to automatically switch the SMPS into Bypass mode. Note that switching back to SMPS mode when VDD increases depends on the application.

Low-power debug information

Keeping the debugger alive while in Low Power modes

- 3 bits in DBGMCU_CR register allows to debug in Sleep, Stop, Standby and Shutdown modes:
  - DBG_SLEEP: When set, HCLK and FCLK remain ON in Sleep and Low-power sleep modes.
  - DBG_STOP: When set, HCLK and FCLK remain ON in Stop modes, provided by internal RC.
  - DBG_STANDBY: When set, the digital part is not unpowered in Standby and Shutdown modes, and HCLK and FCLK remain ON, provided by internal RC. In addition, the MCU in under system reset during Standby/Shutdown.
- When those bits are set, the connection with the debugger is kept during the low-power mode. After wake-up, the debug is still possible.

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Three bits are also available in the Debug Control Register for debugging in Sleep, Stop, Standby and Shutdown modes. When the related bit is set, the regulator is kept ON in Standby and Shutdown modes, and the HCLK and FCLK clocks remain ON to keep the debugger active. This maintains the connection with the debugger during the low-power modes, and continues debugging after wake-up. Remember to clear these bits when the MCU is not under debug, because the consumption is higher in all low-power modes when these bits are set, due to the fact they force the clocks and the regulators to remain enabled.

Related peripherals

- Refer to the following list of peripherals training for more details of their dependencies with the power modes:
  - Reset and clock control (RCC)
  - Interrupts (NVIC AIEC)
  - Comparator (COMP)
  - Liquid crystal display controller (LCD)
  - Low-power timer (LPTIM)
  - Independent watchdog (IWDG)
  - Real-time clock (RTC)
  - Inter-integrated circuit (I2C) interface
  - Universal synchronous asynchronous receiver transmitter (USART)
  - Low-power universal asynchronous receiver transmitter (LPUART)
  - USB Full-Speed (USB_FS)

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In addition to this training, you can refer to the Reset and Clock Control, Interrupts trainings as well as those for all the peripherals with wakeup from Stop and Standby capability.