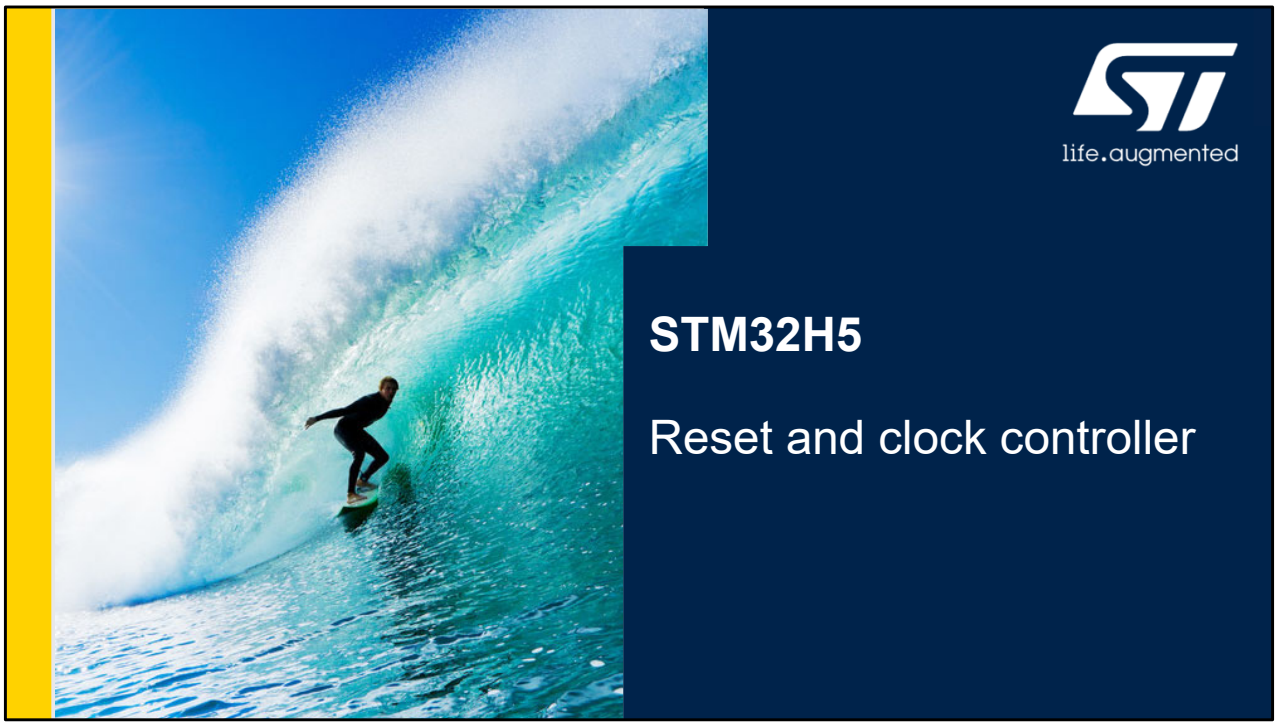

Hello, and welcome to this presentation of the STM32H5 reset and clock controller (or RCC).

Key features

Four internal clock sources

- High-speed internal 64 MHz RC oscillator (HSI)
- Low-power internal RC oscillator clock (CSI)
- Low-speed internal 32 kHz RC oscillator (LSI)
- High-speed internal 48 MHz RC oscillator (HSI48)

Two external oscillators

- High-speed external 4 to 50 MHz oscillator (HSE) with clock security system
- Low-speed external 32.768 kHz oscillator (LSE) with clock security system

Three PLL(1),each with 3 independent outputs

Two PLL(2), each with 2 independent outputs

(1) For STM32H562/573/563
(2) For STM32H503

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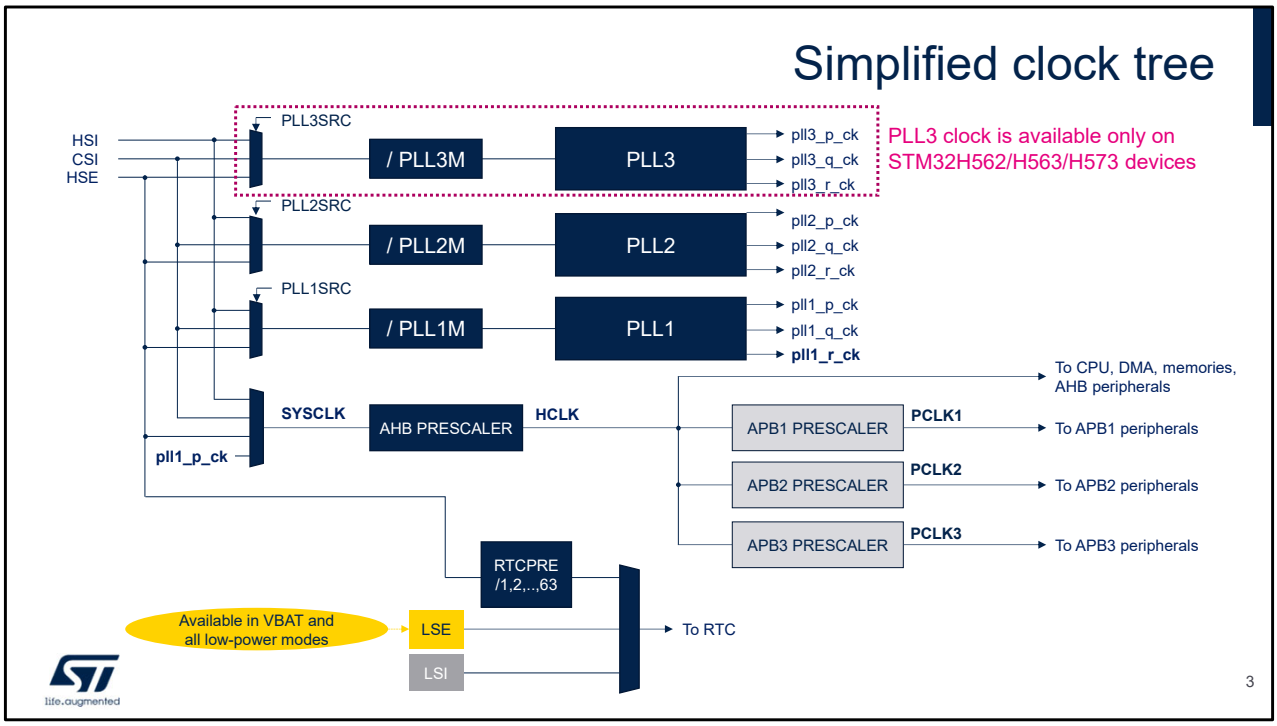
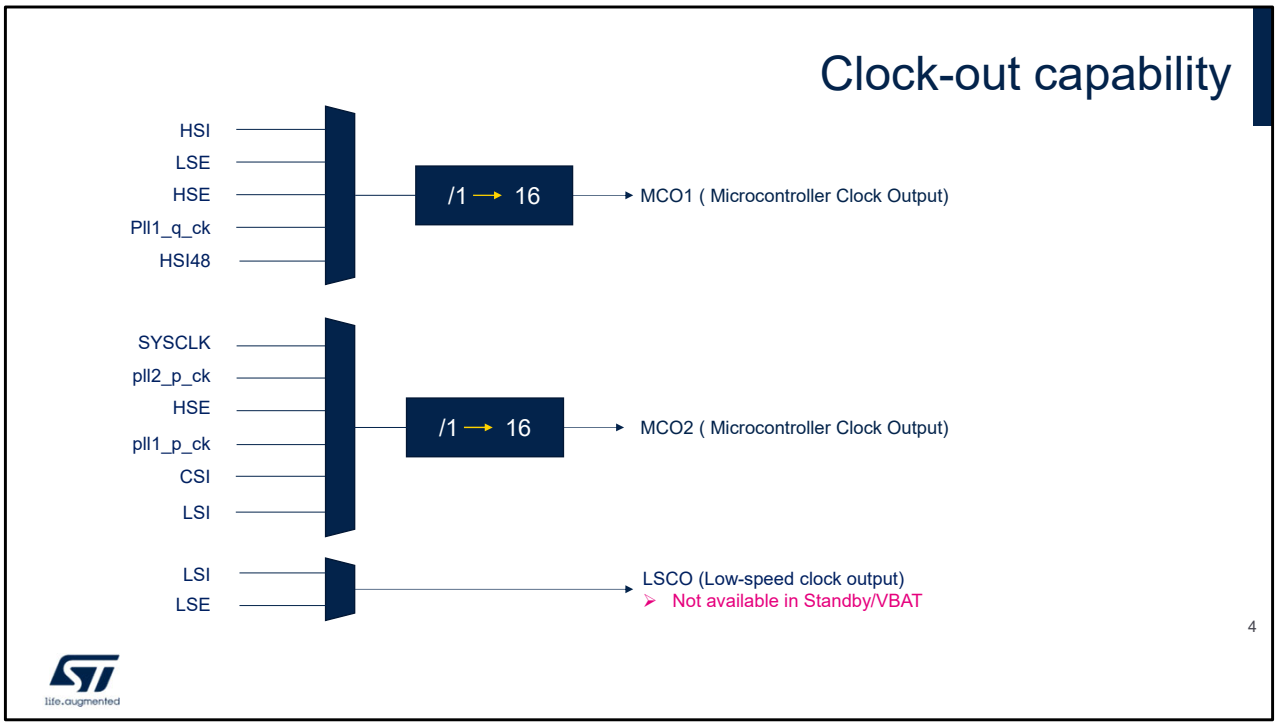
The STM32H5 reset and clock controller manages the system and peripheral clocks.
STM32H5 microcontrollers embed 4 internal oscillators, 2 oscillators for an external crystal or resonator.
Regarding the phase-locked loops (or PLLs), the STM32H56X and STM32H57X integrate three PLLs, while the STM32H503 only integrates two PLLs.
Many peripherals have their own clock, independent of the system clock.
The RCC also manages the various resets present in the device.
The STM32H5 RCC provides high flexibility in the choice of clock sources, allowing the system designer to meet both power consumption and accuracy requirements.

The numerous independent peripheral clocks allow a designer to adjust the system power consumption without impacting the communication baud rates and, also to keep some peripherals active in low-power modes.

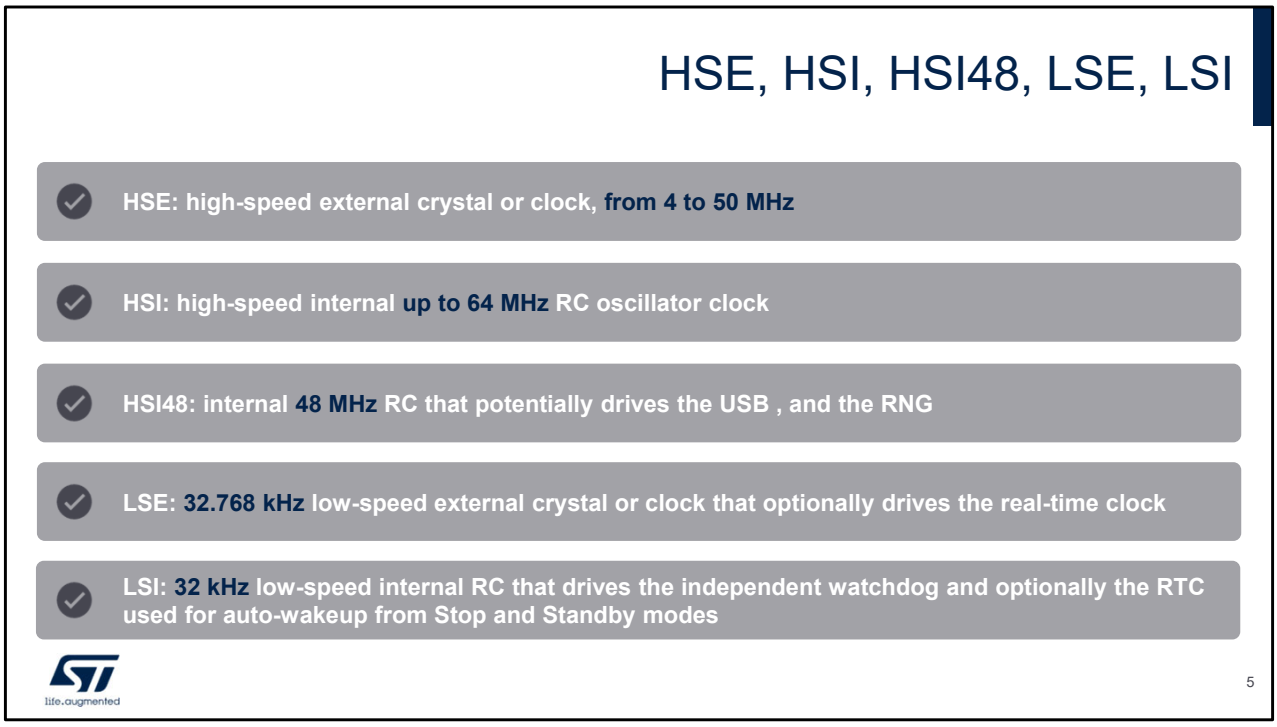


The system clock can be derived from the high-speed internal 64 MHz RC oscillator (HSI), from the high-speed external 4 to 50 MHz oscillator (HSE), from the low-power oscillator (CSI) or from the pll1_p_ck output of the PLL1.
The AHB clock, called HCLK, is derived by dividing the system clock by a programmable prescaler.
The APB clocks, called PCLK1, PCLK2 and PCLK3, are generated by dividing the AHB clock by programmable prescalers.
The RTC clock is generated by the low-speed external 32.768 kHz oscillator (LSE), the low-speed internal 32 kHz RC oscillator (LSI), or the HSE divided by a value in range 1 to 32. This selection cannot be modified without resetting the Backup domain.

The LSE can remain enabled in all low-power modes and in VBAT mode.
The LSI can remain enabled in all modes except in VBAT modes.



Various clocks can be output on I/O pads.
Two microcontroller clock output pins (MCO), MCO1 and MCO2, are available.
A clock source can be selected for each output.
The low-speed clock output feature enables the external output of the LSI or LSE clock, which is driven onto the Low-speed output clock or LSCO pad.
This output remains available in Stop modes but not in Standby and VBAT modes.



This slide describes the features of five oscillators.
- The high-speed external oscillator provides a safe crystal system clock.
The HSE supports a 4 to 50 MHz external crystal or ceramic resonator, as well as an external source in bypass mode.
A clock security system automatically detects an HSE failure. In this case a Non-Maskable Interrupt is generated, and a break input can be sent to the timers in order to put critical applications such as motor control in a safe state.
When an HSE failure is detected, the system clock is automatically switched to an internal oscillator: either HSI or CSI, so that the application software does not stop in the case of crystal failure.

- The high-speed internal oscillator is a 64 MHz RC oscillator which provides fast wakeup times. The HSI is trimmed during production testing and can also be user-trimmed to take into account temperature and voltage variations.
The HSI can be automatically awoken when exiting any Stop mode in order to make it available for peripherals when it is not used as the system clock.
The HSI is used as system clock source after startup from reset, configured at 32 MHz.
- The HSI48 is generated from an internal 48-MHz RC oscillator.
48 MHz is a canonical frequency for a USB module.
HSI48 can also be used as the reference clock for the RNG.
The HSI48 is associated with a special Clock Recovery System (CRS) circuitry that dynamically adjusts the frequency according to the receipt of a USB Start of Frame packet or the LSE or an external signal.
- The Low Speed Internal (LSI) oscillator is the unique clock of the independent watchdog and can be the clock of the RTC. It can be kept running in all Stop and Standby modes. The clock frequency is 32 kHz.

HSI electrical characteristics

Parameter	Condition	Min	Typ	Max	Unit
Frequency	VDD=3.3 V, TJ=30 °C	63.7(1)	64	64.3(1)	MHz
User Trimming step	Trimming is not a multiple of 32(2)	-	0.24	0.32	%
	Trimming is 128, 256 and 384(2)	−5.2	−1.8	-	
	Trimming is 64, 192, 320 and 488 (2)	−1.4	−0.8	-	
	Other trimming are a multiple of 32(2) (not including multiple of 64 and 128	−0.6	−0.25	-	
Startup time	-	-	1.4	2	µs
Stabilization time	At 1 % of target frequency	-	4	8	
	At 5 % of target frequency	-	-	4	
Power consumption	-	-	300	450	µA

(1) Calibrated during manufacturing tests
(2) Trimming value of HSICAL[8:0]

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This table summarizes the features of the HSI oscillator.
The values come from the STM32H5xx data sheets.
Minimum, typical and maximum frequencies are indicated for operation at 30-degree Celsius.
Startup time and stabilization times are also indicated.
Note that the HSI has a faster startup time than the HSE crystal oscillator.
Finally, the table provides the typical and maximum consumption of the HSI, knowing that the HSI can be switched off using the HSION bit.

High-Speed Internal (HSI) clock

1% accuracy, High speed, and fast wakeup time

- The HSI is used as default system clock source after startup from reset, configured at 32 MHz
  - After reset or exit from standby HSI is set to 32MHz
- HSI @64MHz (also 8,16,32MHz), factory- and user-trimmed
- HSI can be selected as
  - Wakeup clock from STOP mode
  - Backup clock for Clock Security System (CSS)
- Can be automatically started when exiting STOP mode
- Can remain activated during STOP mode to avoid the start-up penalty
- Some peripherals can enable the HSI during STOP when they need a kernel clock to detect wakeup event conditions
  - Kernel clock request capability

Parameters	Values (Typical)
Start-up time	1.4 µs
Consumption	300 µA

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The high-speed internal oscillator (HSI) is a 64 MHz RC oscillator which provides fast wakeup times. The HSI is trimmed during production testing and can also be user-trimmed.
A dedicated divider can generate a 32, 16 or 8 MHz clock. The HSI can be selected as a clock at wakeup from system Stop, and as the backup clock if an HSE failure is detected by the Clock Security System.
The HSI can remain powered when the system goes to STOP mode in order to speed up the wakeup time. Certain peripherals such as the I2Cs and U(S)ART/LPUART can request the activation of the HSI in system Stop mode in order to generate wakeup events. The HSI is enabled by the peripheral only for the wakeup

sequence detection and remains disabled outside of this wakeup sequence.

Low Power Internal (CSI) clock

Low-power and fast wakeup time

- CSI @4MHz , factory- and user-trimmed
- CSI can be selected as Wakeup clock from STOP mode
- Can be automatically started when exiting STOP mode
- Can remain activated during STOP mode to avoid the start-up penalty
- Some peripherals can enable the CSI during STOP when they need a kernel clock to detect wakeup event conditions
  - Kernel clock request capability

Parameters	Values (Typical)
Start-up time	1 µs
Consumption	23 µA

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The low-power internal oscillator (CSI) is a 4 MHz RC oscillator which provides fast wakeup times.
The CSI is trimmed during production testing and can also be user trimmed. The CSI can be selected as a clock at wakeup from system Stop.
The CSI can remain powered when the system goes to Stop mode in order the speed-up the wakeup time. Certain peripherals such as the I2Cs and U(S)ART/LPUART can request the activation of the CSI in system STOP mode in order to generate wakeup events. The CSI is enabled by the peripheral only for the wakeup sequence detection and remains disabled outside of this wakeup sequence.

CSI electrical characteristics

Parameter	Condition	Min	Typ	Max	Unit
Frequency	VDD=3.3 V, TJ=30 °C	3.96(1)	4	4.04(1)	MHz
User Trimming step	Trimming is not a multiple of 16	-	0.40	0.75	%
	Trimming is a multiple of 32	−4.75	−2.75	0.75	
	Other trimming are a multiple of 16 (not including multiple of 32)	−0.43	−0.0	0.75	
Startup time	-	-	1	2	µs
Stabilization time	-	-	-	4	Cycle
Power consumption	-	-	23	30	µA

(1) Calibrated during manufacturing tests

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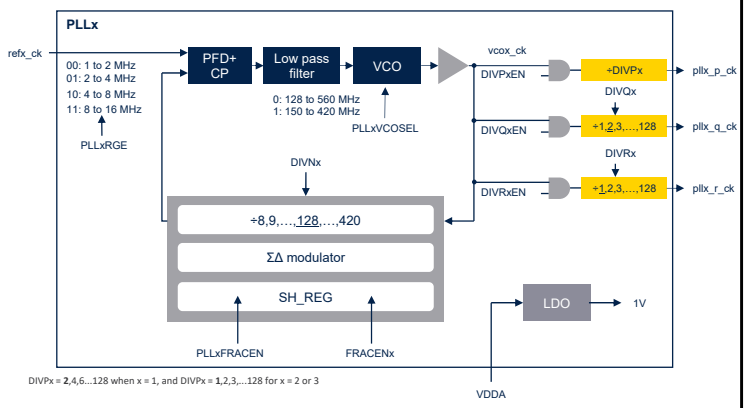
This table summarizes the features of the CSI oscillator.
Minimum, typical and maximum frequency values are indicated for operation at 30 degrees Celsius.
Note the power consumption, more than 10% lower than the one of HSI.

PLLs

- Three PLL(1)
  - Main PLL for the CPU and certain peripherals
  - Others PLLs for peripheral's kernel clock
- A VCO supporting two modes:
  - A wide-range
  - A low-range used for instance in audio application cases
- Input frequency
  - 2 to 16 MHz for the VCO in wide-range mode
  - 1 to 2 MHz for the VCO in low-range mode
- 13-bit fractional multiplication factor
  - Programmable on the fly
- 3 outputs per PLL
  - with a VCO divider range from 1 to 128



(1) Only or STM32H562/573/563

For STM32H562/H563/H573 devices, three PLLs integrated in the RCC are completely independent. Only two PLLs are available for STM32H503 devices
They offer the following features:
A VCO supporting two modes: a wide-range and a low-range used for instance in audio application cases
- the input frequency is between 2 and 16 MHz for the VCO in wide-range mode
- the input frequency is between 1 to 2 MHz for the VCO in low-range mode.
The PLLs also provides 3 different outputs which are all derived from the VCO output via post-dividers (DIVP, DIVQ and DIVR).
In addition, it is possible to change the values of the post-

divider without disabling the PLLs.
The application just needs to disable the corresponding post-divider.
The 13-bit sigma-delta (ΣΔ) modulator fine-tunes the VCO frequency in steps of 11 to 0.3 ppm.
The sigma-delta modulator can be updated on-the-fly, without generating frequency overshoots on PLL outputs.

CLOCK FREQUENCIES

Voltage range	SYSCLK	CSI	HSI	HSI48	HSE	PLL outputs
VOS0	250 MHz	4 MHz	Allowed	Allowed	50 MHz	150 to 420 MHz
VOS1	200 MHz	4 MHz	Allowed	Allowed	50 MHz	150 to 420 MHz
VOS2	150 MHz	4 MHz	Allowed	Allowed	50 MHz	150 to 420 MHz
VOS3	100 MHz	4 MHz	Allowed	Allowed	50 MHz	150 to 420 MHz

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This table indicates the maximum frequencies according to the voltage scaling ranges.
In voltage range 0, the maximum performance is obtained: 250-MHz system clock.
In voltage range 1 and 2, the maximum system frequency is respectively 200 and 150 MHz.
In voltage range 3, the maximum frequency is 100 MHz.
In all cases, the PLL output, before being divided, can be maximum 420 MHz.

LSE

- LSE 32.768 kHz with 3 drive/power levels
  - Medium-low drive
  - Medium-high drive
  - High drive
- Available in all power modes and in VBAT mode

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The LSE clock is generated from a 32.768 kHz crystal or ceramic resonator. It has the advantage to provide a low-power, highly accurate clock source to the real-time clock (RTC) for clock/calendar or other timing functions.
The LSE also offers a programmable driving capability, which can be used to modulate the amplifier driving capability. Three modes are available: medium-low drive, medium-high drive and highest drive.
In case of an analog clock (low swing), the LSEBYP and LSEON bits must be set to 1.
In case of a digital clock, the LSEBYP and the LSEEXT bits must be set to 1 followed by setting the LSEON bit to 1.
The peripherals that can be clocked by the LSE are the

USARTs, the UARTs, the low-power UART1, the RTC, the RNG, the HDMI CEC, the Cortex system timer and the DAC1.

CSS on LSE

- Available in VBAT mode
- Detects clock missing or over frequency, switch to LSI is not automatic
- CSS detection signal is connected to tamper 3 line
  - Interrupt is the TAMP interrupt
  - Caution: In the case of CSS detection, secrets protected by tamper (including SRAM2) cannot be accessed until tamper flag is cleared by software

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A clock security system monitors for failure of the LSE oscillator. It detects a missing clock or over frequency.
The CSS on LSE works in all modes including VBAT. It is also functional during system reset, excluding power-on reset.
The CSS on LSE failure is connected to a tamper event. In the case of a failure, the application can switch the RTC clock to the LSI. This is not automatic.
The tamper flag must be cleared prior to accessing the secrets protected by this tamper.

Thank you

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Thank you for having attended this presentation.
For more details, please refer to application note AN2867, which is an oscillator design guide for STM8S, STM8A and STM32 microcontrollers.