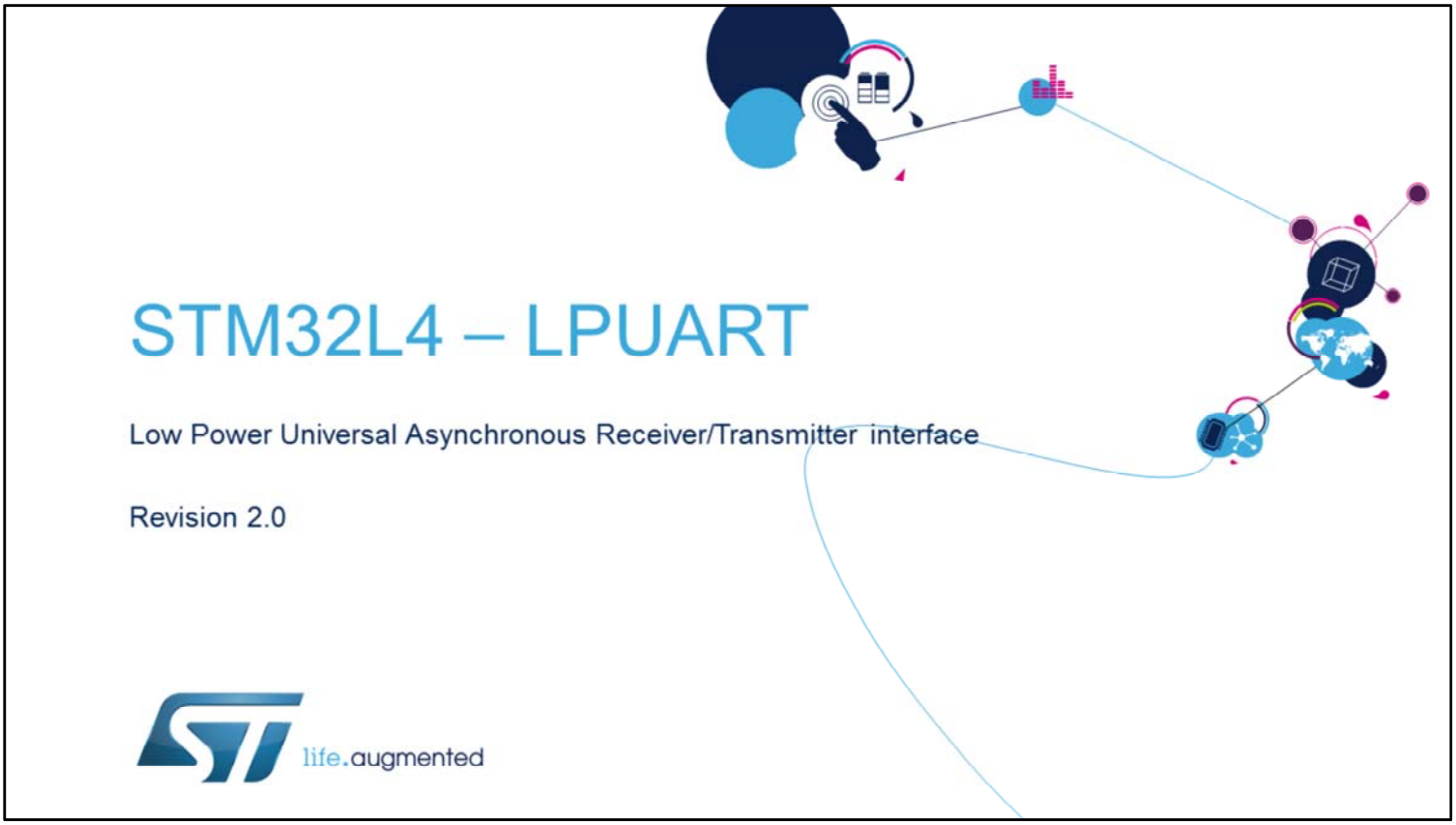
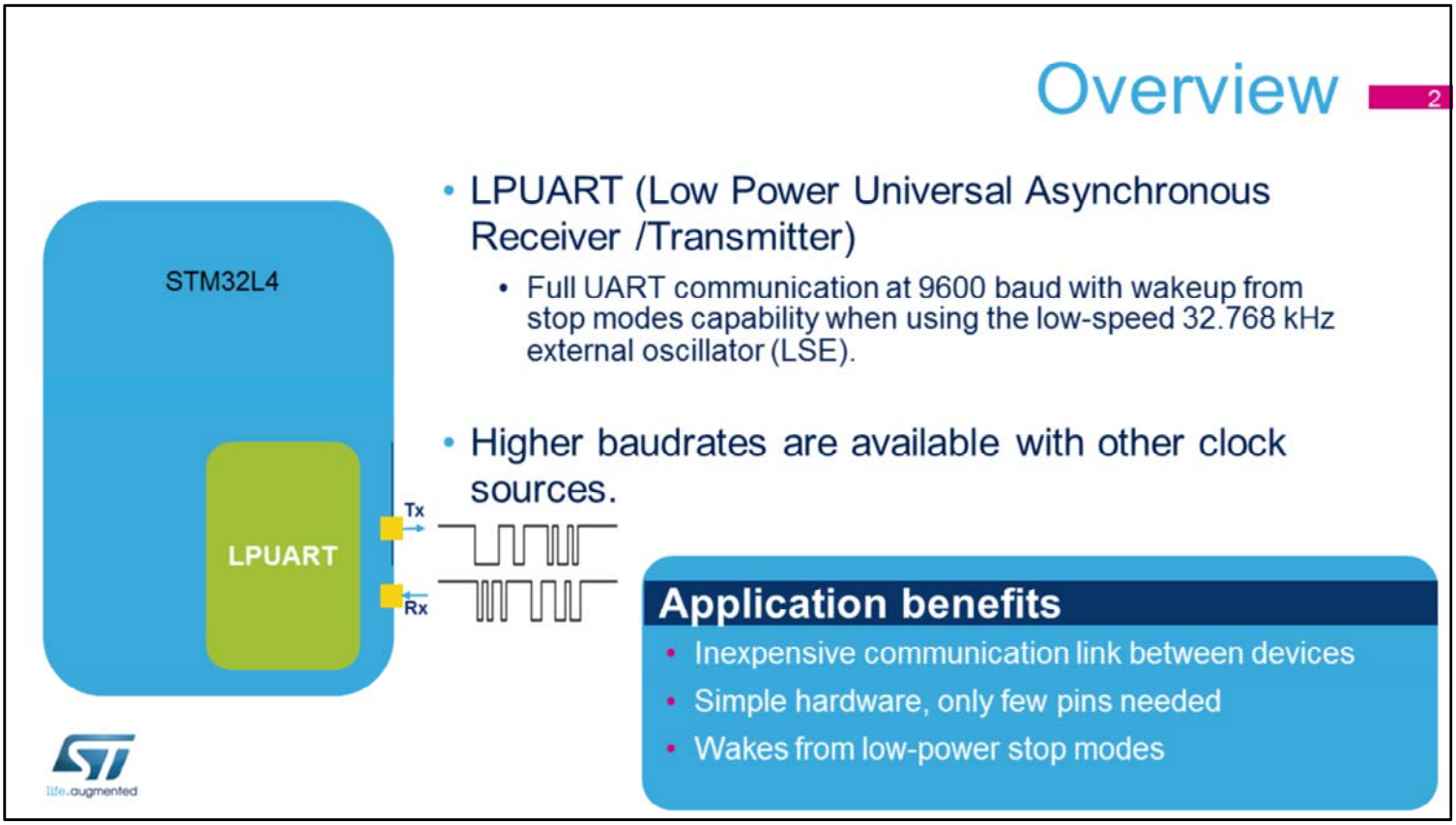


Hello, and welcome to this presentation of the STM32 Low Power Universal Asynchronous Receiver/Transmitter interface. It covers the main features of this interface, which is widely used for serial communications.



The **L**ow **P**ower **U**niversal **S**ynchronous **A**synchronous **R**eceiver provides full UART communications at 9600 baud when the LPUART is clocked using a low-speed external 32.768 kHz oscillator (LSE).
Higher baudrates can be reached when it is clocked by clock sources different from the LSE clock.
Applications can benefit from the easy and inexpensive connection between devices, requiring only a few pins. In addition, the LPUART peripheral is functional in low-power modes.

Key features

3

- Fully programmable serial interface
  - Data can be 7, 8 or 9 bits
  - Even, odd and no-parity
  - 1 or 2 stop bits
  - Programmable data order with MSB or LSB first
  - Programmable signal polarity for transmission and reception.
  - Programmable baudrate generator
- Supports RS-232 and RS-485 hardware flow control

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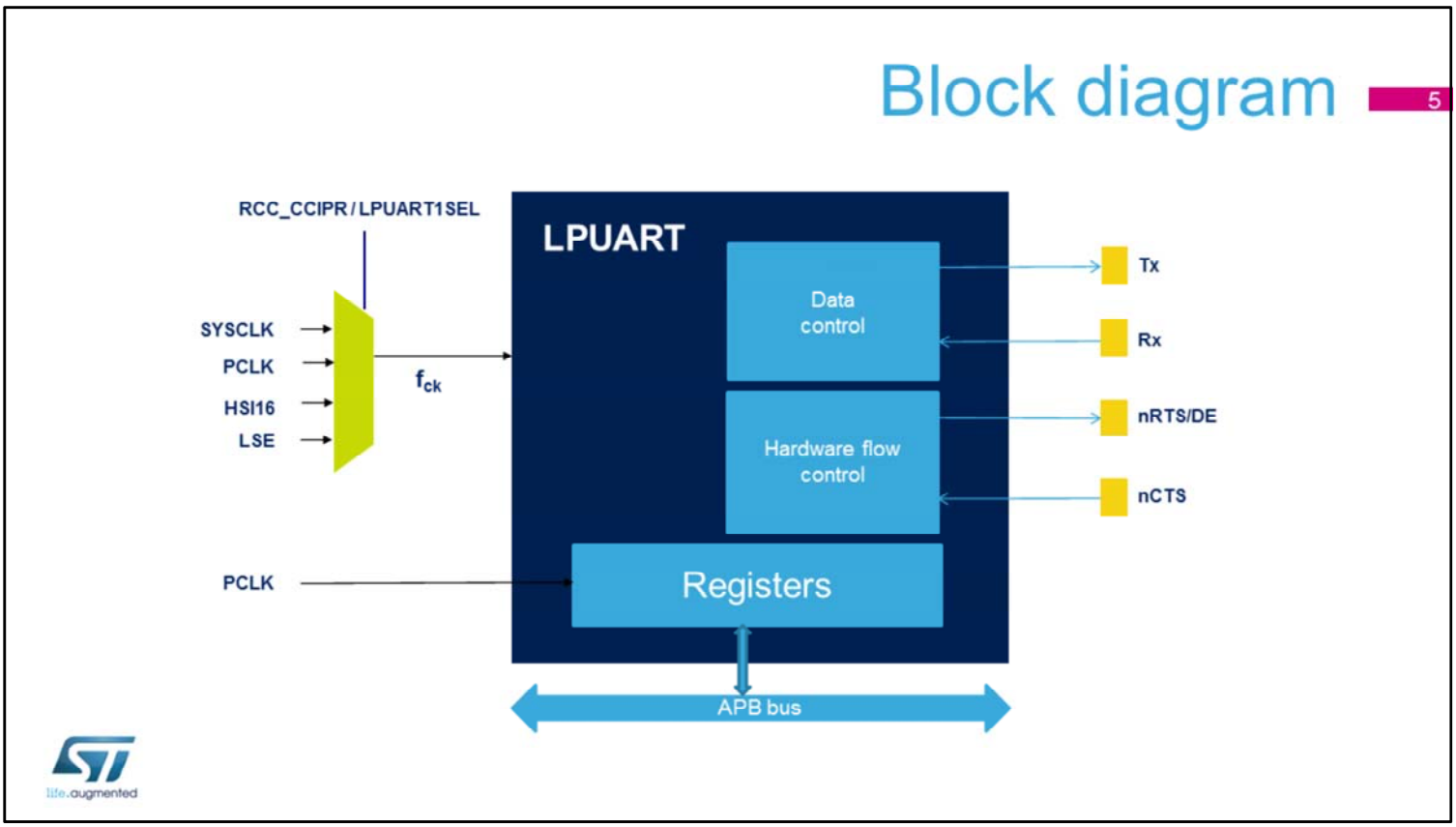
The LPUART is a fully programmable serial interface with configurable features such as data length, parity that is automatically generated and checked, number of stop bits, data order, signal polarity for transmission and reception, and baudrate generator.
It supports RS-232 and RS-485 hardware flow control options.

Key features (continued)

4

- Dual clock domain allowing:
  - UART driven wakeup from stop modes
  - Convenient baudrate programming independent of PCLK
- Multiprocessor communication
- Single-wire half-duplex communication

The LPUART supports dual clock domains allowing for wake up from stop modes and baudrate programming independent of the peripheral clock.
The multi-processor mode allows the USART to remain idle when not addressed.
In addition to full duplex communication, it also supports single-wire half-duplex mode.

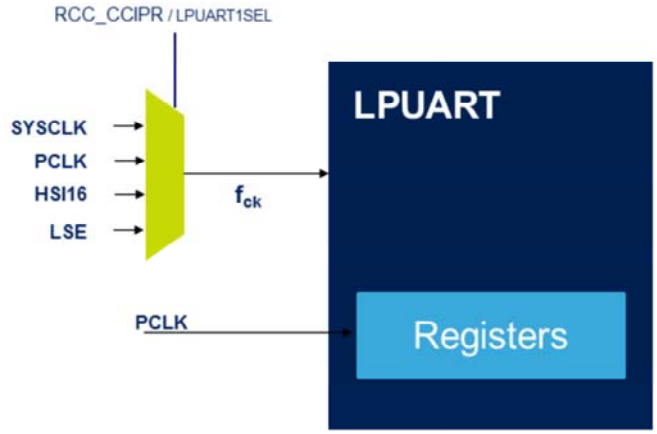


Here is the LPUART block diagram. The LPUART clock “fck” can be selected from among the System clock, APB clock, high-speed internal 16 MHz RC oscillator (**HSI16**) or the low-speed external 32.768 KHz crystal oscillator (LSE).
Tx and Rx are used for data transmission and reception. nCTS and nRTS are used for RS-232 hardware flow control.
The Driver Enable (DE) signal, which is available on the same I/O as nRTS, is used in RS-485 mode.

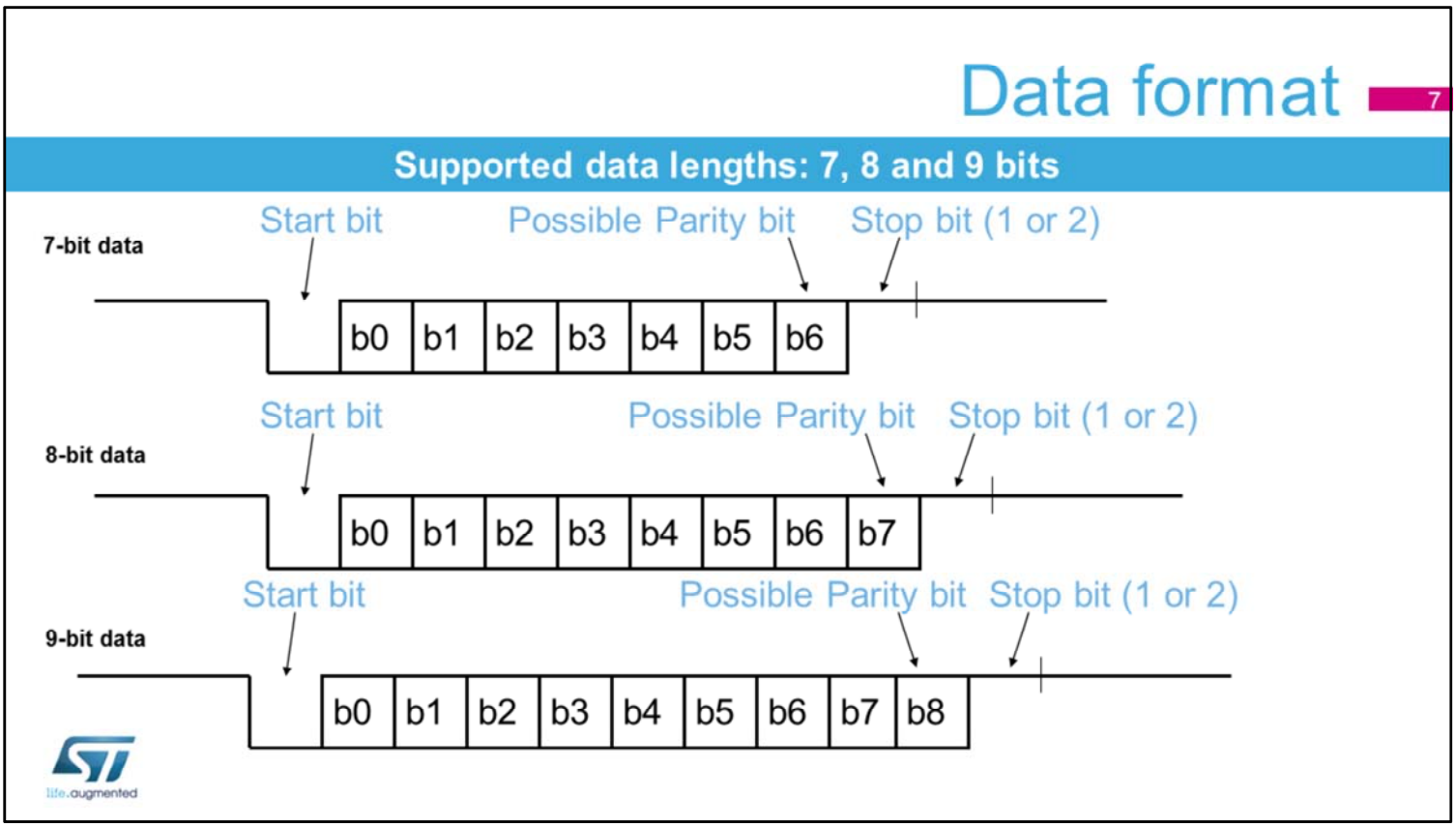
Dual clock domain

Baud rate programming independent from the PCLK reprogramming

- Flexible clocking scheme through selectable clock sources
  - PCLK (default)
  - HSI16 clock
  - LSE clock
  - System clock (SYSCLK)
- Max baudrate is:
  - 9600 baud when fck is LSE 32.768 KHz
  - 26 Mbaud when fck is 80MHz

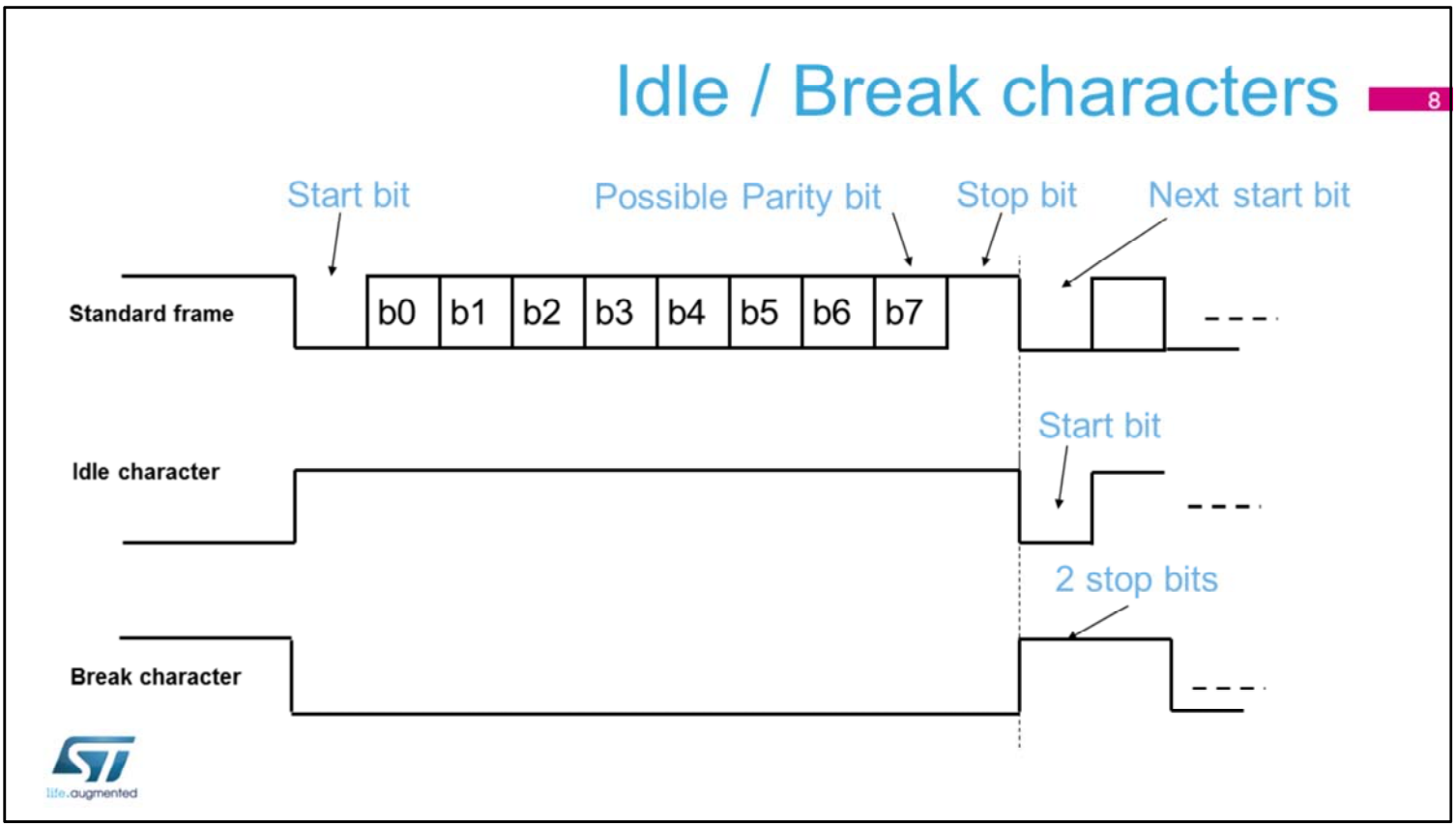


The LPUART has a flexible clocking scheme. Its clock source can be selected in the RCC, and can be either the PCLK which is the default clock source, or **HSI16**, LSE or System clock.
The registers are accessed through the APB bus, and the module is clocked with fck which is independent from the APB clock.
The maximum baudrate that can be reached is 9600 baud when the clock source is LSE, and 26 Mbaud when the clock source is at 80 MHz.

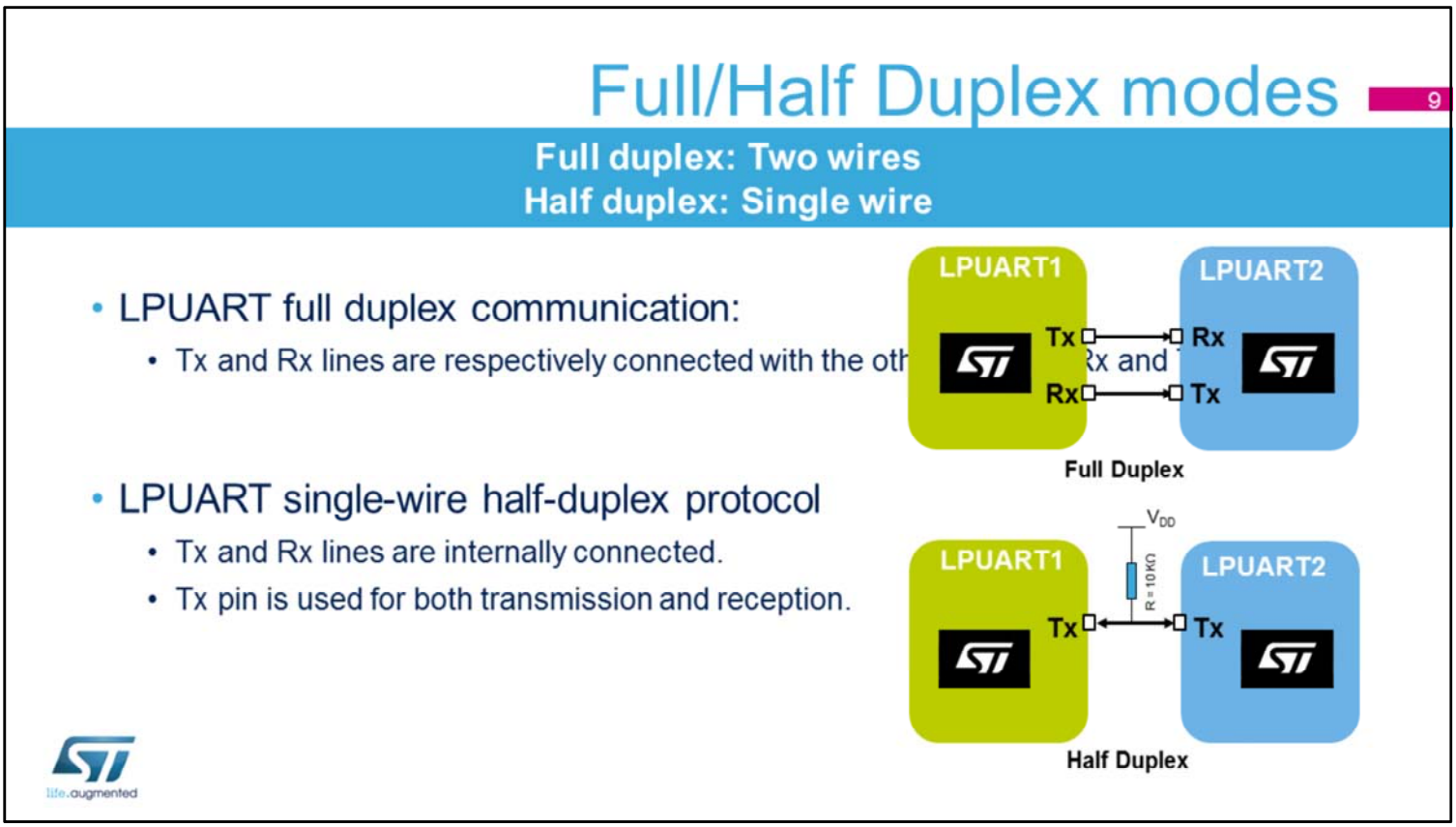


The frame format consists of a set of data bits in addition to bits for synchronization and optionally a parity bit for error checking. A frame starts with one start-bit (S), where the line is driven low for one bit-period. This signals the start of a frame and is used for synchronization.

The data length can be 9, 8, or 7 bits with the parity bit counted. Finally, 1 or 2 stop bits, where the line is driven high, indicate the end of the frame.



The previous slide described a standard frame. This slide shows an example of an 8-bit data frame configured with 1 stop bit.
An Idle character is interpreted as an entire frame of “1”s. The number of “1”s will include the number of stop bits as well.
A Break character is interpreted as receiving all “0”s for a frame period. At the end of the break frame, 2 stop bits are inserted.



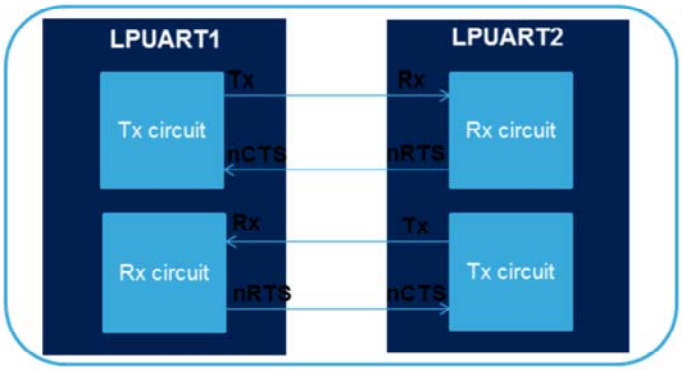
The LPUART supports full-duplex communication where the Tx and Rx lines are respectively connected with the other interface's Rx and Tx lines.

The LPUART can be also configured for single-wire half-duplex protocol where the Tx and Rx lines are internally connected. In this communication mode, only the Tx pin is used for both transmission and reception. The Tx pin is always released when no data is transmitted. Thus, it acts as a standard I/O in idle or reception states. For this usage, the I/O must be configured with the Tx pin in alternate function open-drain mode with an external pull-up resistor.

RS-232 hardware flow control

Hardware handshaking to avoid data underrun/overrun

- RS-232 hardware flow control
  - nRTS (Request to Send) output assterted means the receiver is ready to accept data.
  - nCTS (Clear to Send) input asserted means that the trasmitter can continue communication.
  - Particulary useful for half-duplex systems.



In the RS-232 standard, it is possible to control the serial data flow between two devices by using the nCTS input and the nRTS output. These two lines allow the receiver and the transmitter to alert each other of their state. This slide shows how to connect two devices in this mode. The idea is to prevent dropped bytes or conflicts in case of half-duplex communication. Both signals are active low.

RS-485 hardware flow control

Hardware handshaking

- Useful in half-duplex systems where the master needs to generate a direction signal to control the transceiver (Physical Layer (PHY)). This signal informs the physical layer if it must act in send or receive mode.
- It uses the DE (Driver Enable) pin to activate the external RS-485 bus driver.
- The DE and nRTS signals are available on the same pin.

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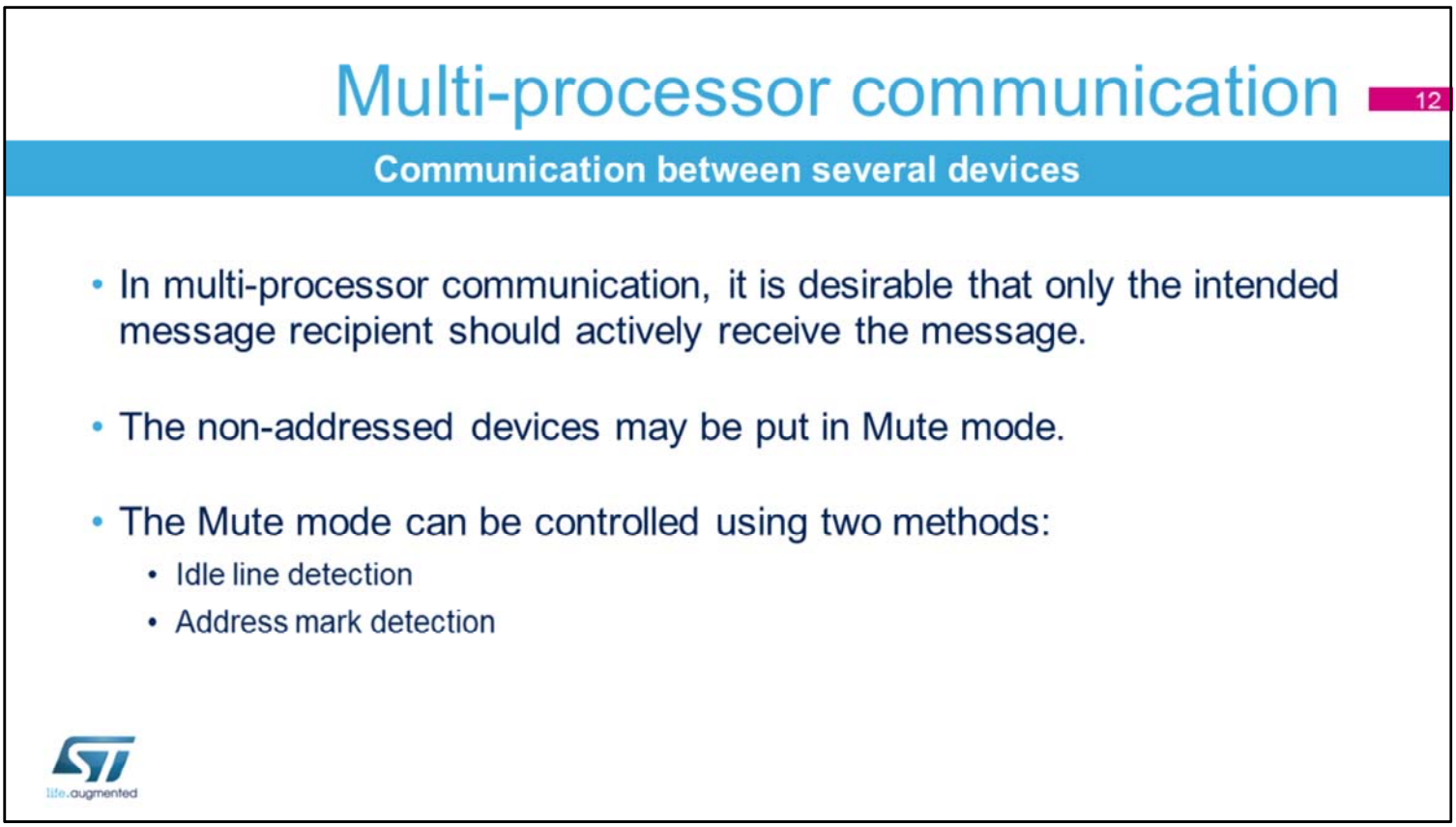
For serial half-duplex communication protocols like RS-485, the master needs to generate a direction signal to control the transceiver (Physical Layer). This signal informs the physical layer if it must act in send or receive mode.

In RS-485 mode, a control line “Driver enable” is used to activate the external transceiver control. DE shares the pin with nRTS.



To simplify communication between multiple processors, the LPUART supports a special multi-processor mode. In multi-processor communication, it is desirable that only the intended message recipient should actively receive the message. The non-addressed devices may be put in Mute mode using two methods: Idle line or address mark.
The LPUART can enter or exit from Mute mode using one of two methods:
- Idle line detection
- Address mark detection

Wakeup from STOP mode

- The LPUART is able to wakeup the MCU from Stop mode when the LPUART clock source is:
  - HSI16 or
  - LSE
- The sources of wakeup can be:
  - Standard RXNE interrupt or
  - A specific wakeup event triggered by:
    - Start bit
    - Address match
    - Any received data

The LPUART is able to wake up the MCU from Stop mode when the LPUART clock source is **HSI16** or LSE. The sources of wakeup can be the standard RXNE interrupt or a specific event triggered by a Start bit detection, an address match or whenever any data is received.

Interrupts

Interrupt event	Description
Transmit Data register empty	Set when the Transmit Data register is empty.
Transmit complete	Set when the data transmission is complete and both data and shift registers are empty.
CTS	Set when the nCTS input toggles.
Receive data register Not Empty	Set when the Receive Data register contains data.
Idle line	Set when an idle line is detected.
Character match	Set when the received data corresponds to the programmed address.
Wakeup from stop mode	Set when a wakeup from stop mode is verified.

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Several LPUART events can provide an interrupt.

The Transmit Data Register Empty flag is set when the Transmit Data Register is empty and ready to be written.
The Transmit Complete flag is set when the data transmission is complete and both data register and shift register are empty.
The CTS flag is set when the nCTS input toggles.
The Receive Data Register Not Empty flag is set when the Receive Data Register contains data ready to be read.
The Idle Line flag is set when an idle line is detected.
The Character Match flag is set when the received data corresponds to the programmed address.
The Wakeup from Stop Mode flag is set when the wakeup event (Start bit or address match or any received data) is verified.

Error interrupts and DMA

Interrupt event	Description
Overrun error	Set when an overrun error occurs.
Parity error	Set when a parity error occurs.
Framing error	Set when a de-synchronization or excessive noise is detected.
Noise error	Set when noise is detected on the received frame's Start bit.

- DMA requests are triggered by Transmit Data Register Empty and Receive Data Register Full flags.

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Several errors flags can also be generated by the LPUART as shown in the table.
The Overrun, Parity and Framing error flags are each set when the corresponding error occurs.
The Noise error flag is set when a noise is detected on the received frame’s Start bit.

DMA requests can be triggered when Receive Buffer Not Empty or Transmit Buffer Empty flags are set.

Low-power modes

Mode	Description
Run	Active.
Sleep	Active. Peripheral interrupts cause the device to exit Sleep mode.
Low-power run	Active.
Low-power sleep	Active. Peripheral interrupts cause the device to exit Low-power sleep mode.
Stop 0/Stop 1	The LPUART is able to wake up the MCU from Stop 0, Stop 1 and Stop 2 modes when the LPUART clock is set to HSI16 or LSE. The MCU wakeup from Stop0, Stop 1 and Stop 2 modes can be done using either a standard RXNE interrupt or a WUF event.
Stop 2	
Standby	Powered-down. The peripheral must be reinitialized after exiting Standby mode.
Shutdown	Powered-down. The peripheral must be reinitialized after exiting Shutdown mode.

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The LPUART peripheral is active in Run, Low-power run, Sleep and Low-power sleep modes. The LPUART interrupts cause the device to exit Sleep or Low-power sleep modes.
The LPUART is able to wake up the MCU from **Stop 0,** Stop 1 and Stop 2 modes when the LPUART clock is set to HSI16 or LSE. The MCU wakeup from **Stop 0,** Stop 1 and Stop 2 modes can be done using either a standard RXNE interrupt or a WUF event.

In Standby and Shutdown, the peripheral is in power-down, and it must be reinitialized after exiting these modes.

STM32L4 LPUART features

U(S)ART/LPUART features	USART	LPUART
Hardware flow control for modem	x	x
Multi-processor communication	x	x
Synchronous mode	x	-
Smartcard mode	x	-
Single-wire half-duplex communication	x	x
IrDA SIR ENDEC	x	-
LIN mode	x	-
Dual clock domain and wakeup from stop mode	x	x
Receiver timeout	x	-
Modbus communication	x	-
Auto-baudrate detection	x	-
Driver enable	x	x

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The STM32L4 devices embed a single LPUART instance. Compared to the USART, the LPUART doesn't support Synchronous, Smartcard, IrDA and LIN modes. It does not support the Receiver timeout, modbus communication and the auto-baudrate detection features as well.

Related peripherals

18

- Refer to these other peripheral trainings related to the LPUART
  - GPIO (alternate function configurations)
  - Reset and Clock Controller (RCC)
  - Power controller (PWR)
  - Interrupts (NVIC and EXTI)
  - Direct memory access controller (DMA)

This is a list of peripherals related to the LPUART. Please refer to these peripheral trainings for more information if needed.
- General-purpose input/output
- Reset and clock controller
- Power controller
- Interrupts controller
- Direct memory access controller