Hello, and welcome to this presentation of the STM32L4 reset and clock controller.

STM32L4 categories

2

- This presentation has been written for STM32L47x/48x devices.
- Key differences with other devices are indicated at the end of the presentation unless otherwise specified.

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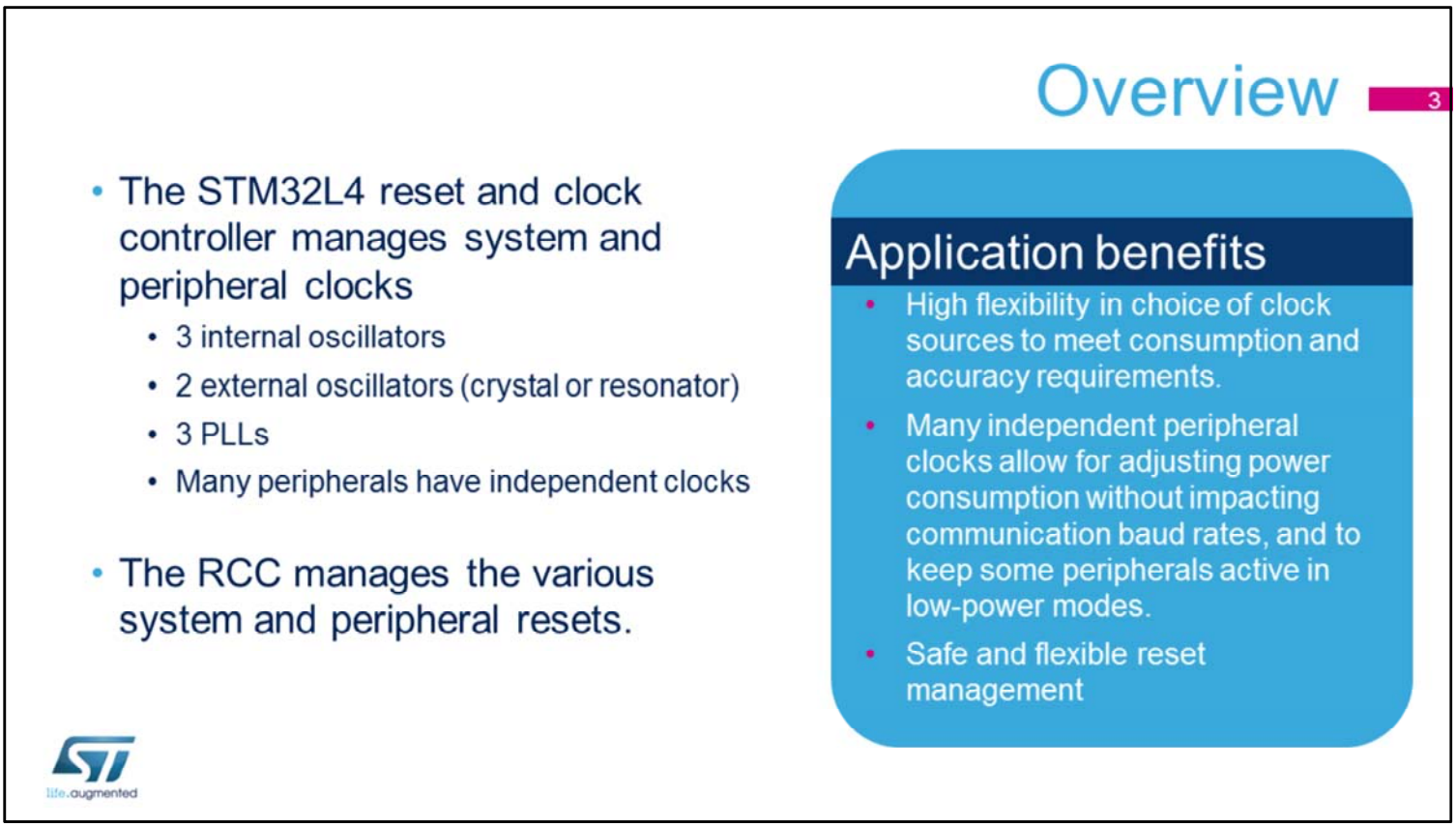


The STM32L4 reset and clock controller manages system and peripheral clocks. STM32L4 devices embed three internal oscillators, 2 oscillators for an external crystal or resonator, and three phase-locked loops (PLL). Many peripherals have their own clock, independent of the system clock.
The RCC also manages the various resets present in the device.
The STM32L4 RCC provides high flexibility in the choice of clock sources, which allows the system designer to meet both power consumption and accuracy requirements. The numerous independent peripheral clocks allow a designer to adjust the system power consumption without impacting the communication baud rates, and also to keep some peripherals active in low-power modes. Finally, the RCC provides safe and flexible reset management.

Reset key features

Safe and flexible reset management without external components

- Manages three types of reset:
  - System reset
  - Power reset
  - Backup domain reset
- Peripherals have individual reset control bits

Safe and flexible reset management without any need for external components reduces application costs.
The RCC manages three types of resets: the system reset, the power reset and the backup domain reset.
The peripherals have individual reset control bits.

Reset sources

5

- System reset
  - Resets all registers except certain RCC registers, PWR registers, and the Backup domain
  - Reset sources
    - Low level on the NRST pin (external reset)
    - WWDG event
    - IWDG event
    - Firewall event
    - A software reset (through NVIC)
    - Low-power-mode security reset
    - Option byte loader reset
    - Brown-out reset
  - The Reset Source flag is in the RCC_CSR register

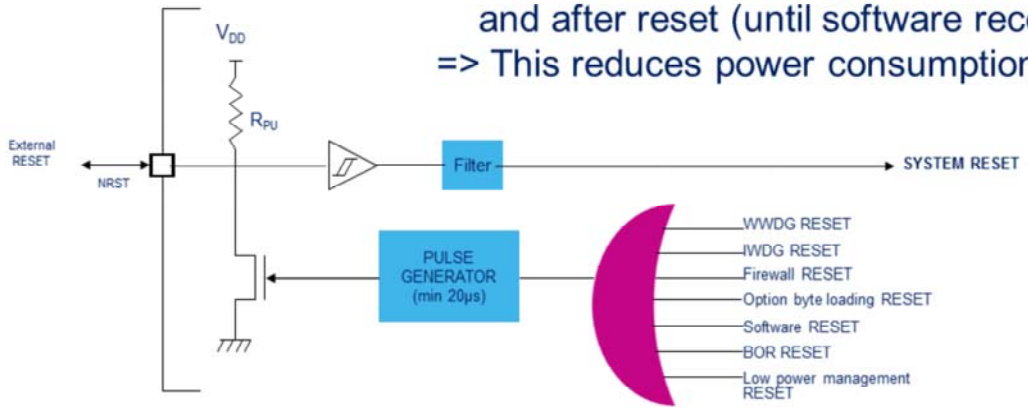
The first type of reset is the System Reset, which resets all the registers except certain registers for the Reset and Clock Controller and Power Controller. It also does not reset the Backup domain.
The system reset sources are the external reset (generated by a low level on the NRST pin), a window watchdog event, an independent watchdog event, a firewall event, a software event through the Nested Vectored Interrupt Controller, a low-power-mode security reset (which is generated when Stop, Standby or Shutdown mode is entered but is prohibited by the option byte configuration), an option byte loader reset, and a brown-out reset.
The reset source flag can be found in the RCC Control and Status register.

Reset sources

- No external components are needed due to internal filter and power monitoring
- System reset sources can reset external components

- Reset pull-up deactivated during internal reset
- I/Os in analog mode (no Schmitt trigger) during and after reset (until software reconfiguration).

=> This reduces power consumption under reset



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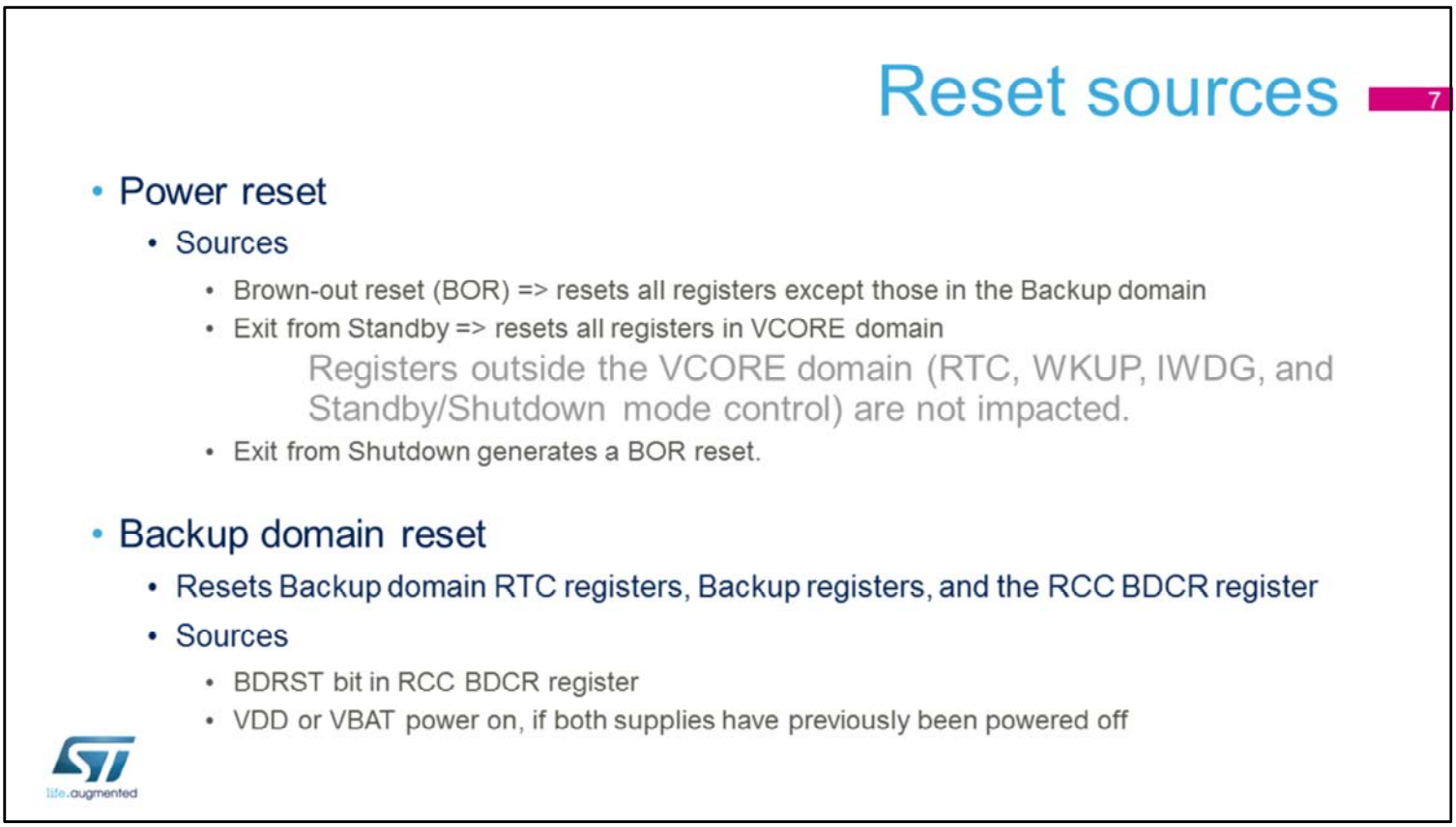
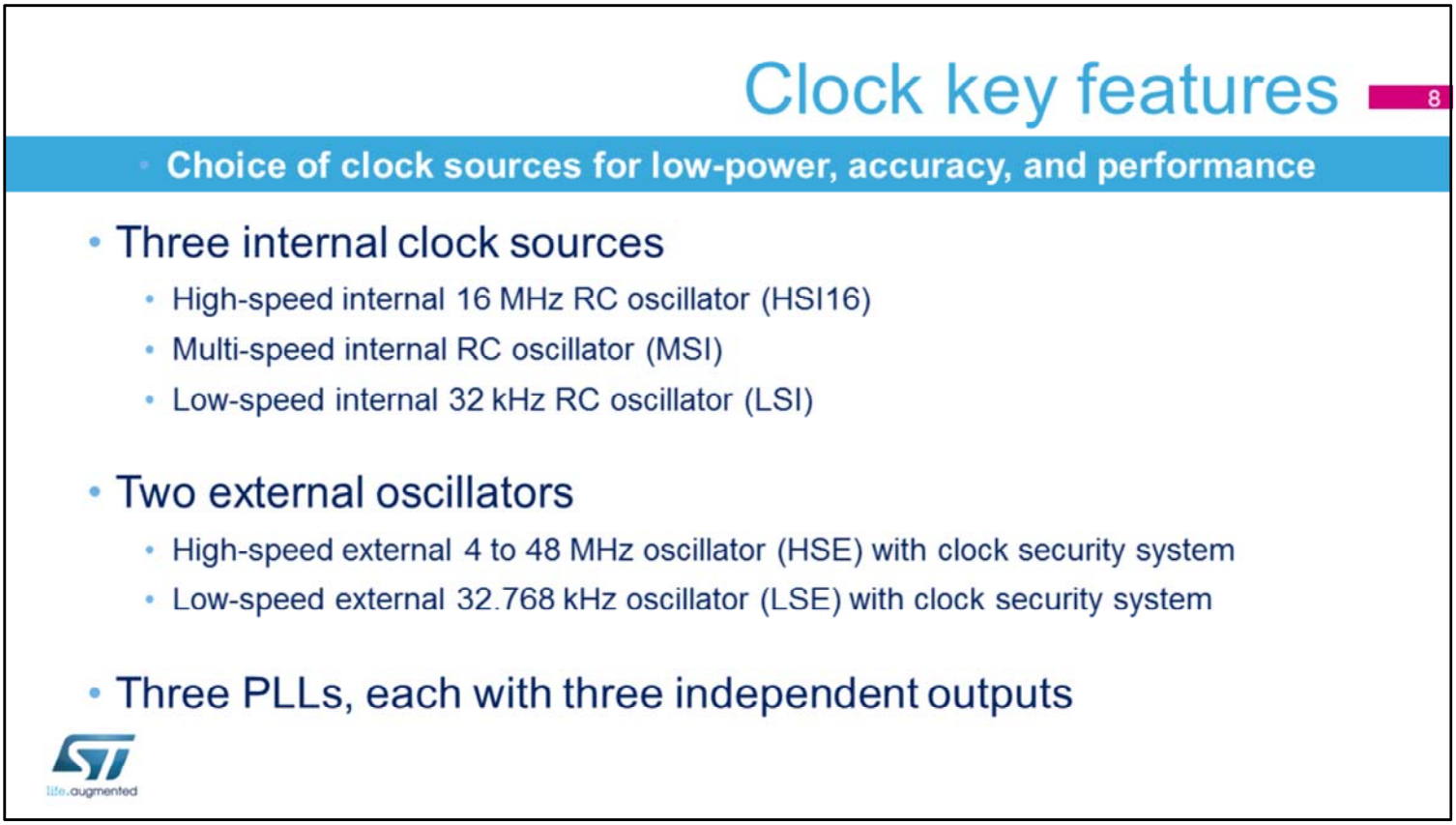
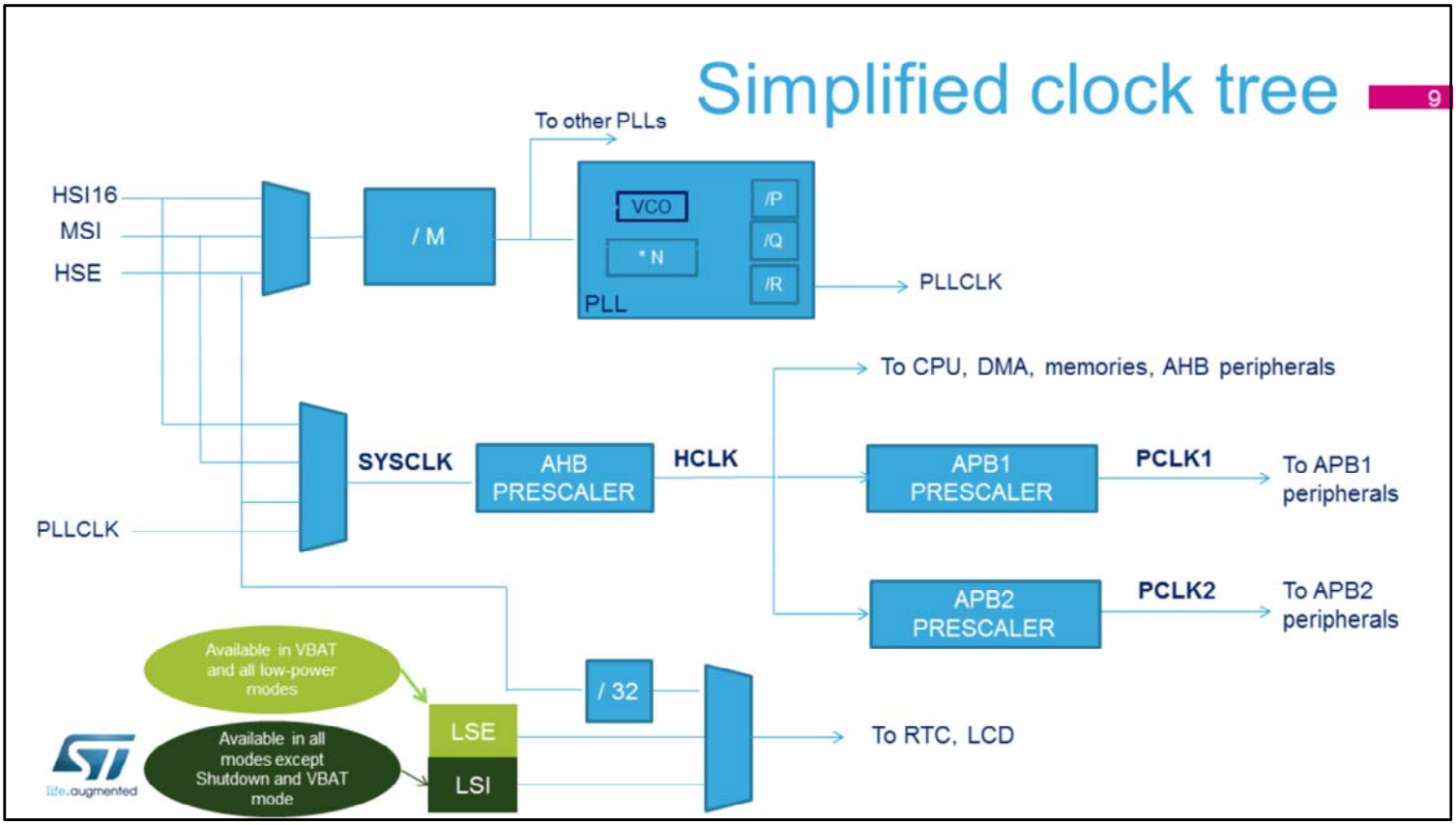
Here is the simplified block diagram of the system reset. All internal reset sources provide a reset signal on the NRST pin, which can be used to reset other components of the application board. In addition, no external reset circuitry is needed due to the internal glitch filter and the safe power monitoring feature which guarantees the reset of the application when VDD is below the selected threshold. The internal pull-up on the NRST pin, which maintains a high level when no reset signal is driven low, is deactivated when an internal reset is driven in order to reduce power consumption under reset. Additionally, all I/O pins are placed in analog mode during and after reset to eliminate power consumption through the Schmitt trigger when the I/Os are floating under reset and before software initialization.



The second type of reset is the power reset. The Brown-out reset (BOR) resets all registers except those in the Backup domain powered by VBAT which contains the RTC and the external low-speed oscillator. When exiting Standby mode, all registers powered by the regulator are reset. When exiting Shutdown mode, a Brown-out reset is generated.
The third type of reset is the Backup domain reset, which resets the RTC registers, the Backup registers, and the RCC Backup Domain Control Register. This reset occurs when the BDRST bit is set in the RCC Backup Domain control register. It also occurs when VDD and VBAT are powered on if both supplies have previously been powered off.



The RCC offers a large choice of clock sources, which can be selected depending on low-power, accuracy, and performance requirements.
STM32L4 devices embed three internal clock sources: a high-speed internal 16 MHz RC oscillator (HSI16), a multi-speed internal RC oscillator (MSI), and a low-speed internal 32 kHz RC oscillator (LSI).
STM32L4 devices embed two oscillators for use with an external crystal or resonator: a high-speed external 4 to 48 MHz oscillator (HSE) with a clock security system and a low-speed external 32.768 kHz oscillator (LSE) also with a clock security system.
STM32L4 devices embed three phase-locked loops, each with three independent outputs for clocking different peripherals at different frequencies.



The system clock can be derived from the high-speed internal 16 MHz RC oscillator (HSI16), the multi-speed internal RC oscillator (MSI), or the high-speed external 4 to 48 MHz oscillator (HSE). The AHB clock, called HCLK, is derived by dividing the system clock by a programmable prescaler. The APB clocks, called PCLK1 and PCLK2, are generated by dividing the AHB clock by programmable prescalers.

The RTC and LCD clock is generated by the low-speed external 32.768 kHz oscillator (LSE), the low-speed internal 32 kHz RC oscillator (LSI), or the HSE divided by 32. The LSE can remain enabled in all low-power modes and in VBAT mode. The LSI can remain enabled in all modes except Shutdown and VBAT modes.

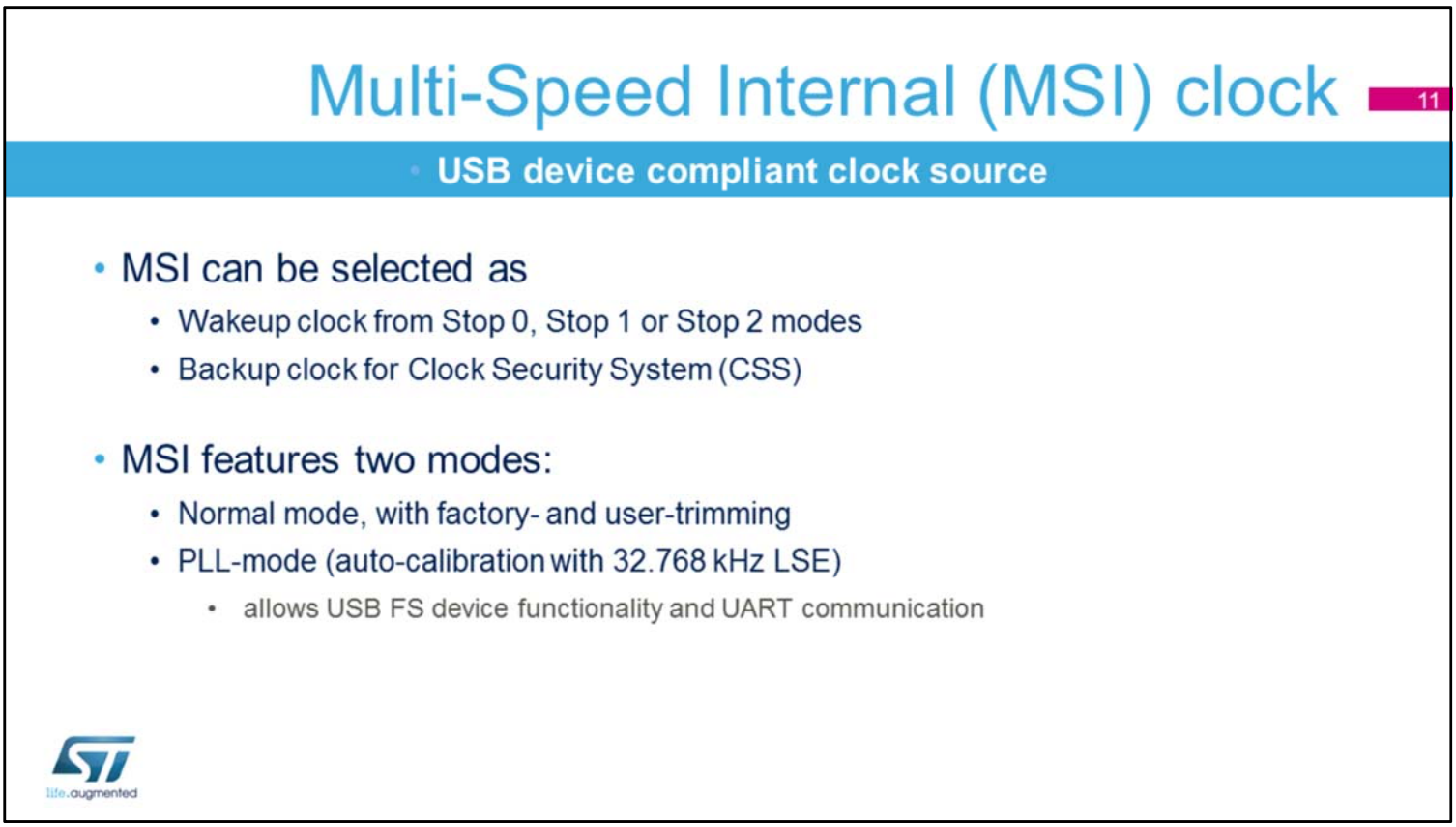
Multi-Speed Internal (MSI) clock

10

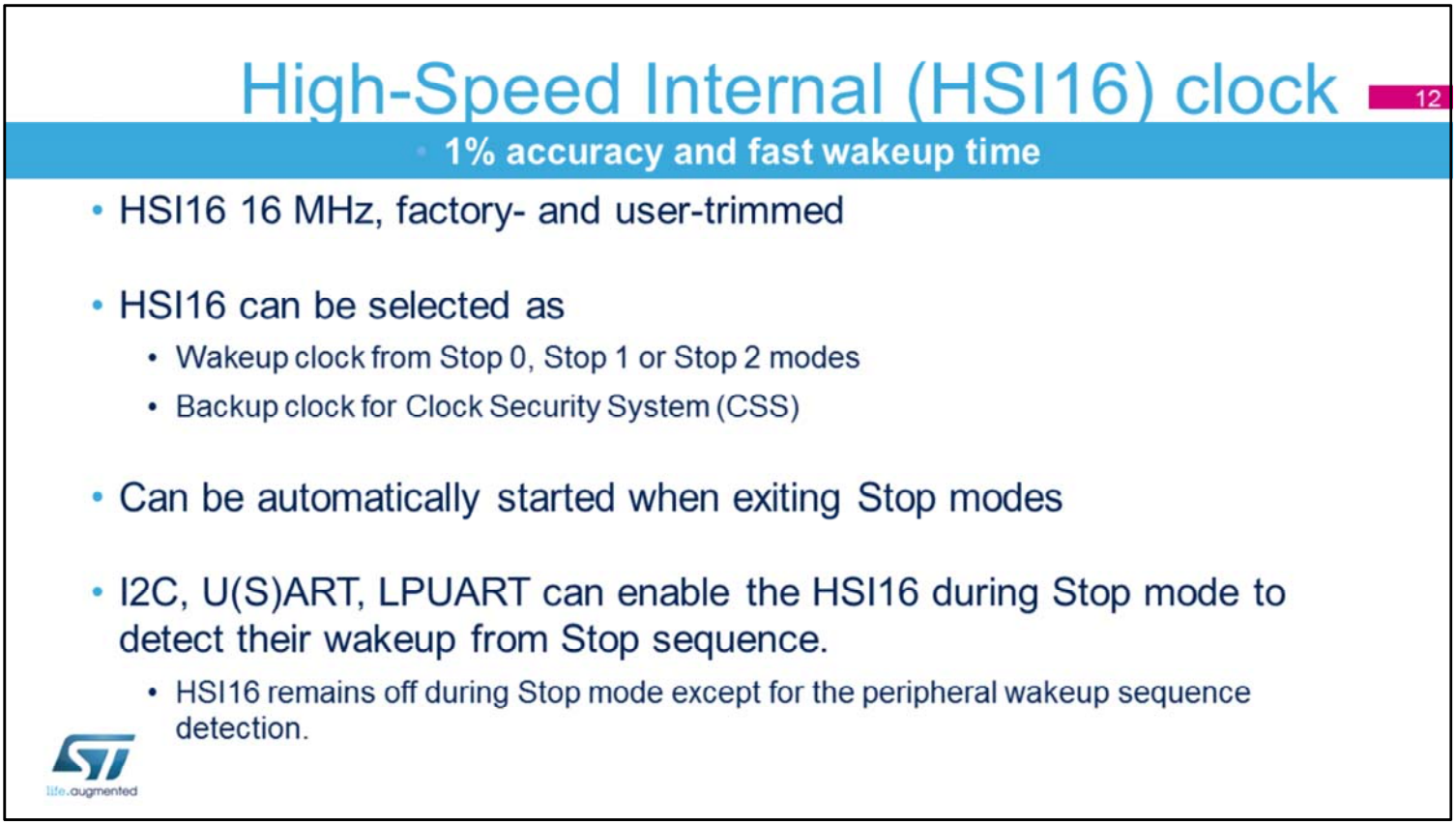
- **Low frequencies for low-power, high frequencies for performance**

- Programmable frequency:
  - 12 ranges selected with MSIRANGE in RCC_CR: 100 kHz, 200 kHz, 400 kHz, 800 kHz, 1 MHz, 2 MHz, 4 MHz (reset value), 8 MHz, 16 MHz, 24 MHz, 32 MHz, 48 MHz.
    - MSIRGSEL bit must be set in RCC_CR register to switch to the frequency selected by MSIRANGE
  - After Standby, MSI frequency is selected from 1, 2, 4 or 8 MHz according to MSISRANGE in RCC_CSR register.
  - After Reset and Shutdown, MSI frequency is 4 MHz.

The Multi-Speed Internal oscillator (MSI) is a configurable oscillator, offering a compromise between ultra-low power and performance.
The MSI which is the system clock used at startup from Reset, Standby or Shutdown modes, is programmable.
It supports 12 ranges from 100 kHz to 48 MHz, selected through the MSIRANGE control bits.
The MSIRGSEL bit must be set in order to select the frequency provided by MSIRANGE.
The MSI frequency after wakeup from Standby mode is configurable between 1, 2, 4 or 8 MHz, through the MSISRANGE control bits.
The frequency after reset or at wake up from shutdown mode is 4 MHz.



The MSI can be selected as a wakeup clock from Stop 0, Stop 1 or Stop 2 modes, and as the backup clock if an HSE failure is detected by the Clock Security System.
The MSI has two modes, normal mode and PLL mode. PLL mode offers an automatic calibration feature with the Low-speed external oscillator at 32.768 kHz. The accuracy of PLL mode allows the MSI to be used as a USB full-speed clock in device mode, and to be used as a UART peripherals clocks.
The MSI in normal mode is trimmed during production testing, and can also be user-trimmed.



The high-speed internal oscillator is a 16 MHz RC oscillator which provides 1% accuracy and fast wakeup times. The HSI16 is trimmed during production testing, and can also be user-trimmed.
The HSI16 can be selected as clock at wakeup from Stop 0, Stop 1 or Stop 2 modes, and as the backup clock if an HSE failure is detected by the Clock Security System.
The HSI16 can be automatically awaken up when exiting Stop mode in order to make it available for peripherals when it is not used as the system clock. This avoids waiting for the HSI16 to wake up when the system clock is the MSI.
The HSI16 is requested by the I2C and the U(S)ART/LPUART peripherals to support wakeup from Stop 0, Stop 1 or Stop 2 modes. HSI16 is enabled only for the wakeup sequence detection and remains disabled

outside of this wakeup sequence.

HSI16 vs. MSI characteristics

	MSI (100 kHz to 48 MHz)		HSI16 (16 MHz)
	MSI mode (w/o LSE)	PLL mode (w/ 32.768 kHz LSE)	
Accuracy (typ.)	Over [0 - 85 C]: +/- 1.55 %	Average accuracy = LSE accuracy Jitter < 0.25%	Over [0-85 C]: +/- 0.8 %
	Over [1.62 - 3.6 V]: +0.8/-4.5 %		Over [1.62 - 3.6 V]: +0.1/-0.2 %
Consumption (typ.)	100 kHz : 0.6 µA 800 kHz : 1.9 µA 1 MHz : 4.7 µA 8 MHz : 18.5 µA 16 MHz : 62 µA 48 MHz : 155 µA		150 µA
Startup time (typ.)	100 kHz : 10 µs 48 MHz : 2.5 µs	5% final frequency : 0.5 ms 1% final frequency : 1.5 ms max	1 µs

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This table compares the HSI16 and MSI characteristics. The HSI16 accuracy is better than that of the MSI when not used in PLL mode. In PLL mode, the average MSI accuracy is the LSE accuracy (32.768 kHz external crystal, resonator or clock).The MSI power consumption is much lower for the same frequency than the HSI16, and is only 600 nA at 100 kHz. The HSI16 offers the fastest wakeup time, only 1 µs. The maximum time needed for the MSI to be stabilized at 1% of final frequency in PLL mode is 1.5 ms.

High-Speed External (HSE) clock

Safe crystal system clock

- HSE 4-48MHz
  - External source (Bypass mode) up to 48 MHz
  - External crystal/ceramic resonator (4 - 48 MHz)
- Clock Security System (CSS)
  - Automatic detection of HSE failure with
    - Non-maskable interrupt generation
    - Break input to TIM1/TIM8/TIM15/TIM16/TIM17 => critical applications such as motor control can be put in a safe state.
  - Backup clock can be HSI16 or MSI => application software does not stop in case of crystal failure
    - MSI by default

The high-speed external oscillator provides a safe crystal system clock.
The HSE supports a 4 to 48 MHz external crystal or ceramic resonator, and also an external source in bypass mode.
A clock security system allows an automatic detection of HSE failure. In this case a Non-Maskable Interrupt is generated, and a break input can be sent to timers in order to put critical applications such as motor control in a safe state. When an HSE failure is detected, the system clock is automatically switched to an internal oscillator, the HSI16 or the MSI, so the application software does not stop in case of crystal failure.

Low-Speed Internal (LSI) clock

- Ultra-low power internal 32 kHz oscillator
- Available in all modes except Shutdown and VBAT

	LSI 32 kHz
Accuracy (typ.)	Over Temperature: +/- 1.5 %
	Over VDD: +0.1 / -0.2%
Consumption (typ.)	110 nA

STM32L4 devices embed an ultra-low-power 32 kHz RC oscillator, which is available in all modes except Shutdown and VBAT.
The LSI can be used to clock the RTC, the LCD, the low-power timers, and the independent watchdog. The accuracy of the LSI is plus or minus 1.5% over temperature and plus 0.1 minus 0.2% over voltage. The LSI consumption is typically 110 nA.

Low-Speed External (LSE) clock

16

- **32.768 kHz configurable for low-power or high-drive**
- **Available in all power modes and in VBAT mode**

- The LSE can be used with external quartz or resonator, or with external clock source in bypass mode
- **Clock Security System on LSE**: Available in all modes except Shutdown and VBAT. Operates under reset.
- The LSE can be used for RTC, LCD, U(S)ARTs, LPUART, LPTIMs.

Mode	Maximum critical crystal gm (µA/V)	Consumption (nA)
Ultra-low power	0.5	250
Medium-low driving	0.75	315
Medium-high driving	1.7	500
High driving	2.7	630

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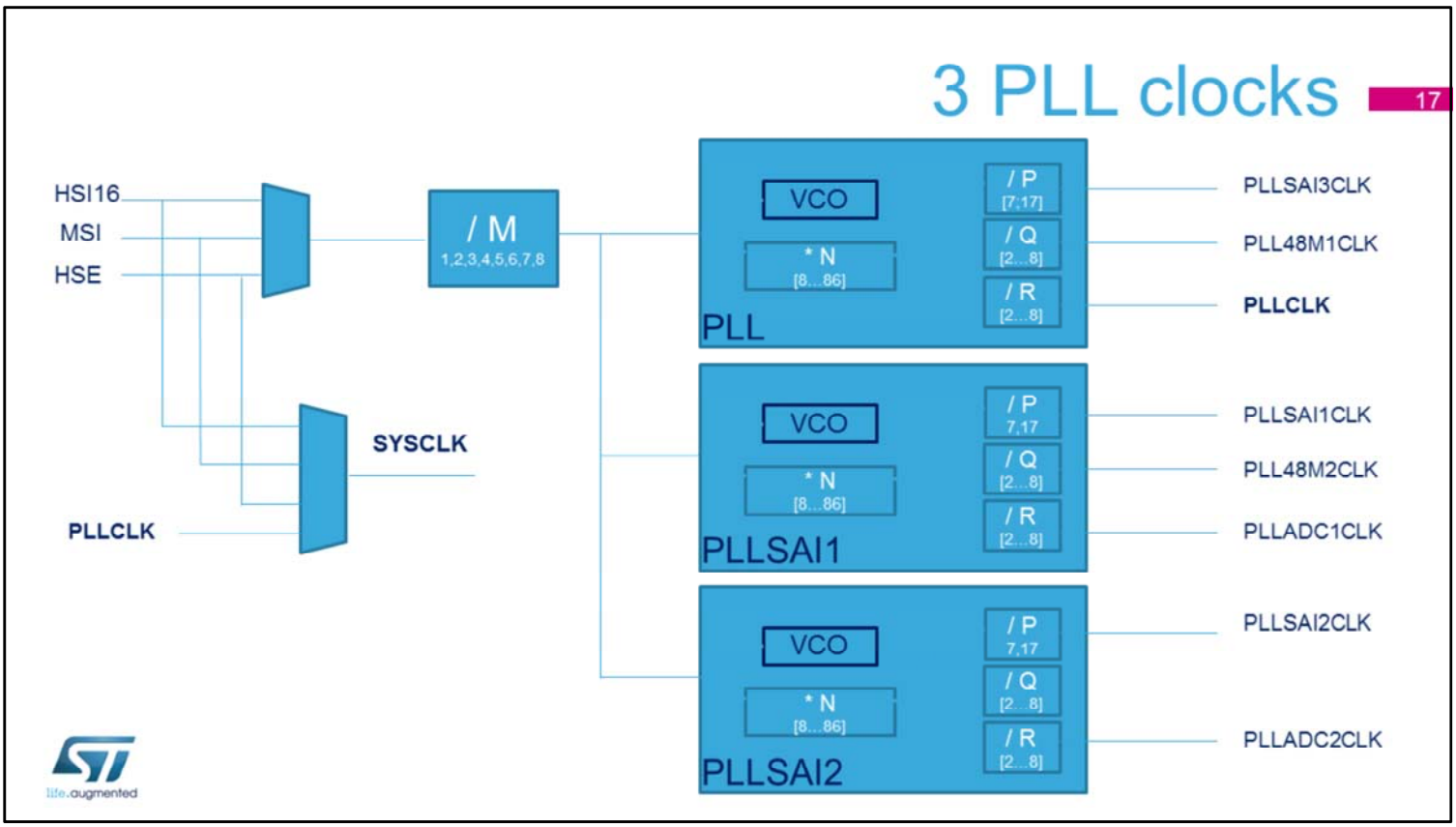
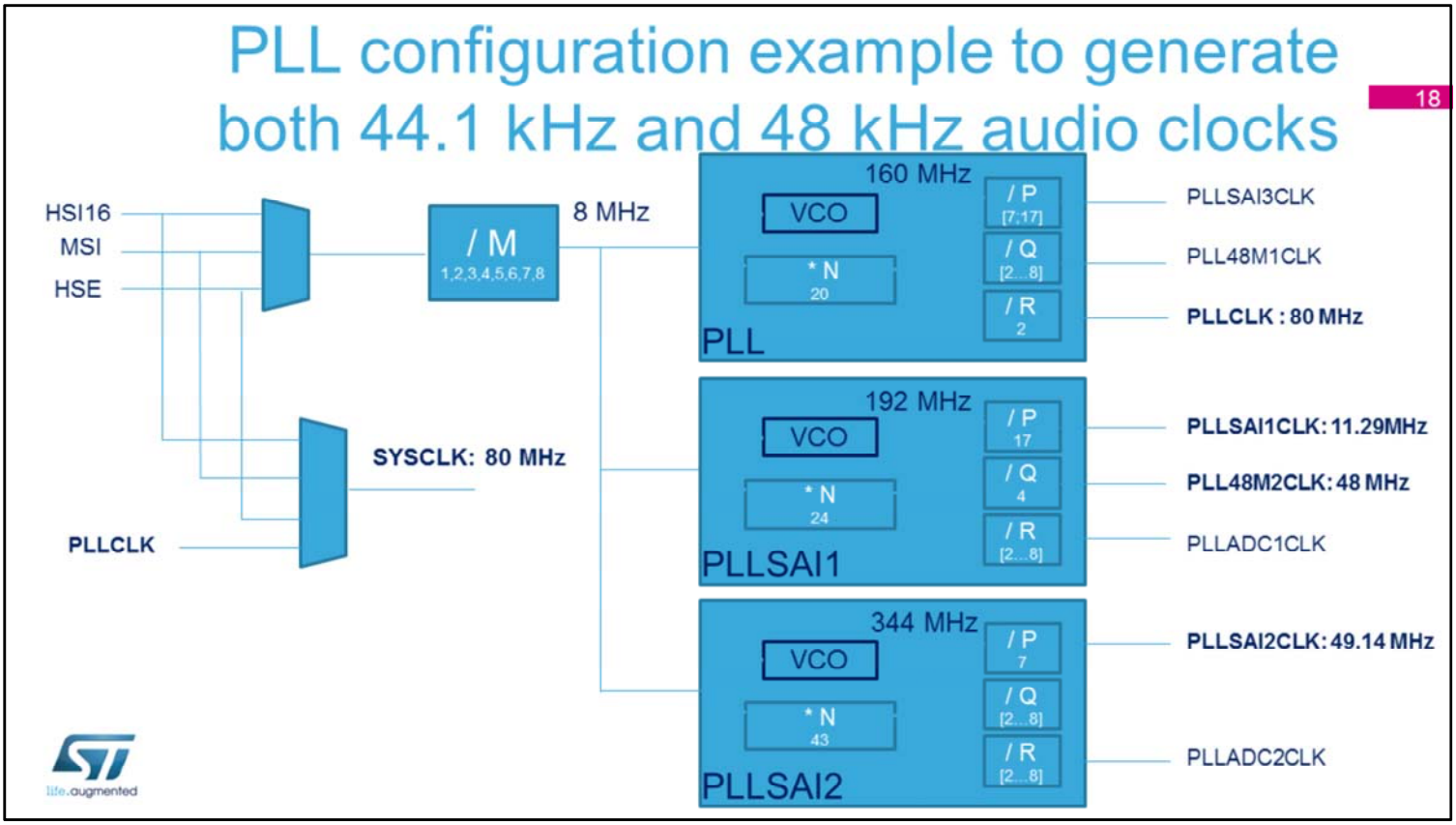
The 32.768 kHz low-speed external oscillator can be used with external quartz or resonator, or with an external clock source in bypass mode. The oscillator driving capability is programmable. Four modes are available, from ultra-low power mode with a consumption of only 250 nanoamps, to high-driving mode.
A clock security system monitors for failure of the LSE oscillator. In case of failure, the application can switch the RTC clock to the LSI. The CSS is functional in all modes except Shutdown and VBAT. It is also functional under reset.
The LSE can be used to clock the RTC, the LCD, the USARTs or low-power UART peripherals, and the low-power timers.



STM32L4 devices embed 3 phase-locked loops, each with 3 independent outputs. The input clock of the PLL can be selected between HSI16, MSI and HSE.
The main PLL can provide the system clock.
Then the different PLL outputs can be used for the 2 Serial audio interfaces, ADC interface, USB, Random Number Generator, and SDMMC peripherals.



Here is a configuration example where the first PLL is configured to generate the 80 MHz system clock. The second PLL, PLLSAI1, is used to provide the 11.29 MHz audio clock used to generate a sample frequency submultiple of 44.1 kHz, and to provide the 48 MHz USB clock.

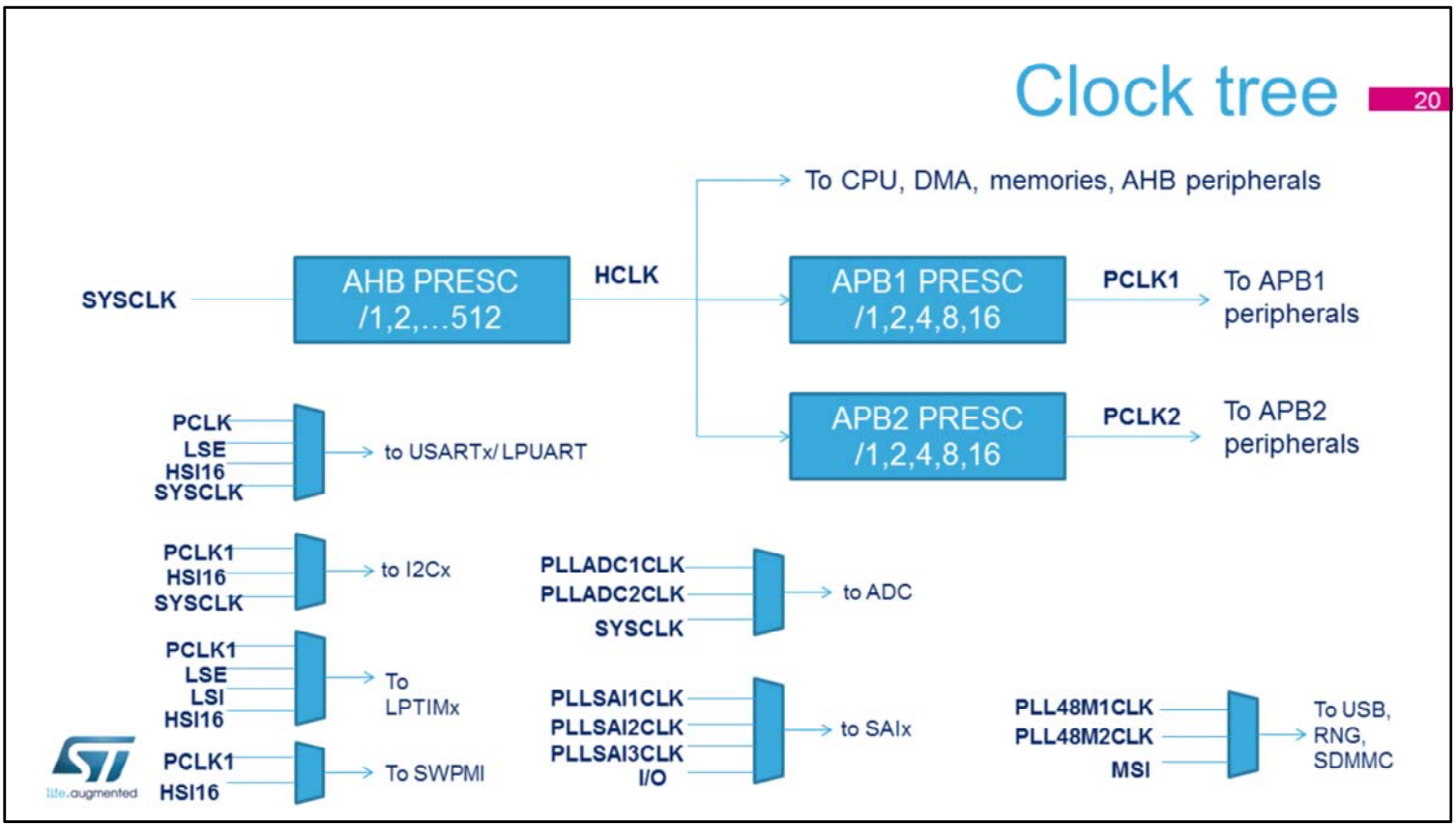
The third PLL, PLLSAI2, is used to provide the 49.14 MHz audio clock used to generate a sample frequency submultiple of 192 kHz.

System clock

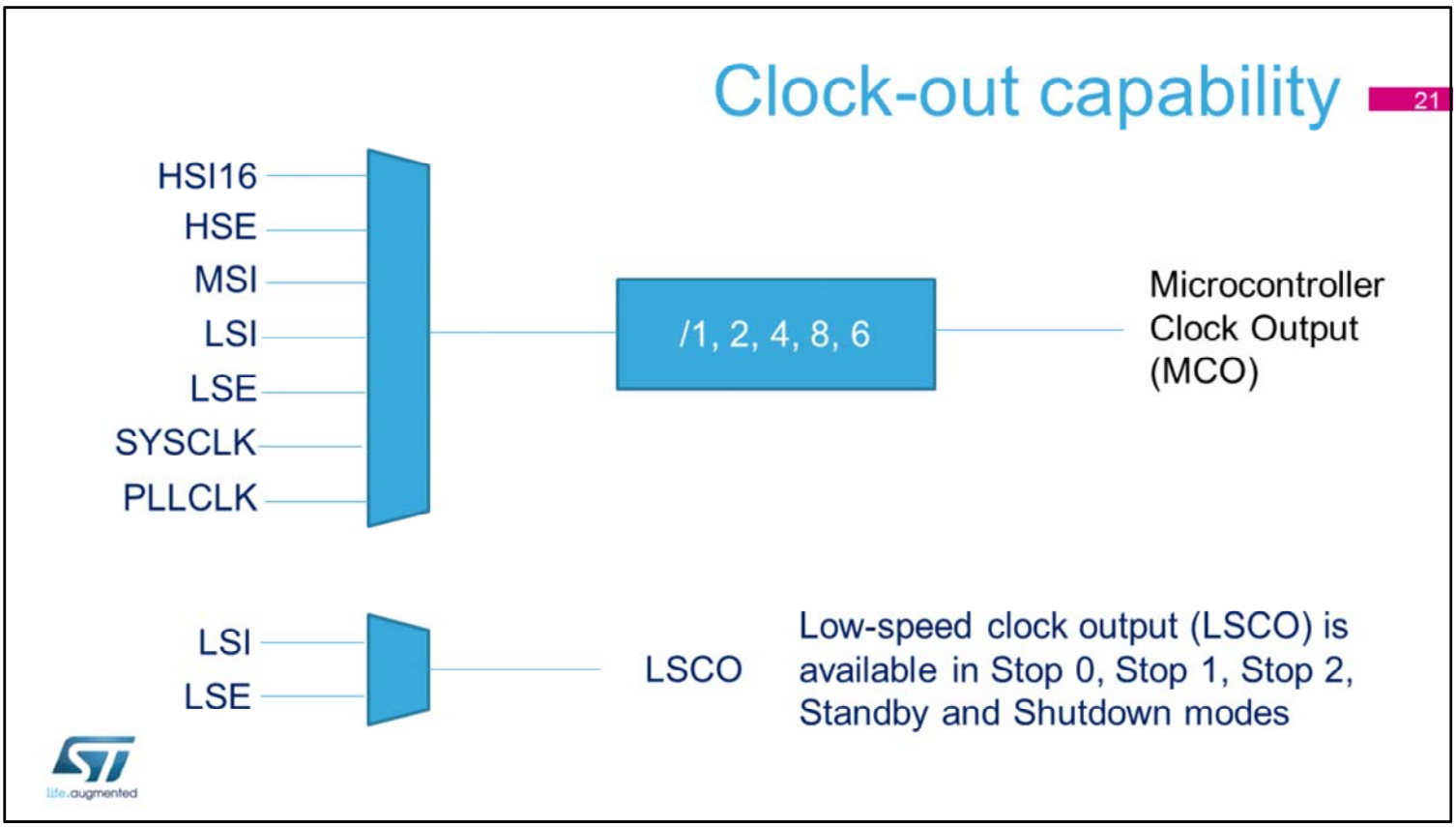
- Selected between HSI16/HSE/MSI/PLL
- System clock, AHB, APB1, and APB2 maximum frequency: 80 MHz

Voltage range	SYSCLK	MSI	HSI16	HSE	PLL
Range 1	80 MHz max.	48 MHz range	16 MHz	48 MHz	80 MHz VCO max = 344 MHz
Range 2	26 MHz max.	24 MHz range	16 MHz	26 MHz	26 MHz VCO max = 128 MHz
Low-power run/sleep	2 MHz max.	2 MHz range	Allowed	Allowed with divider	Not allowed

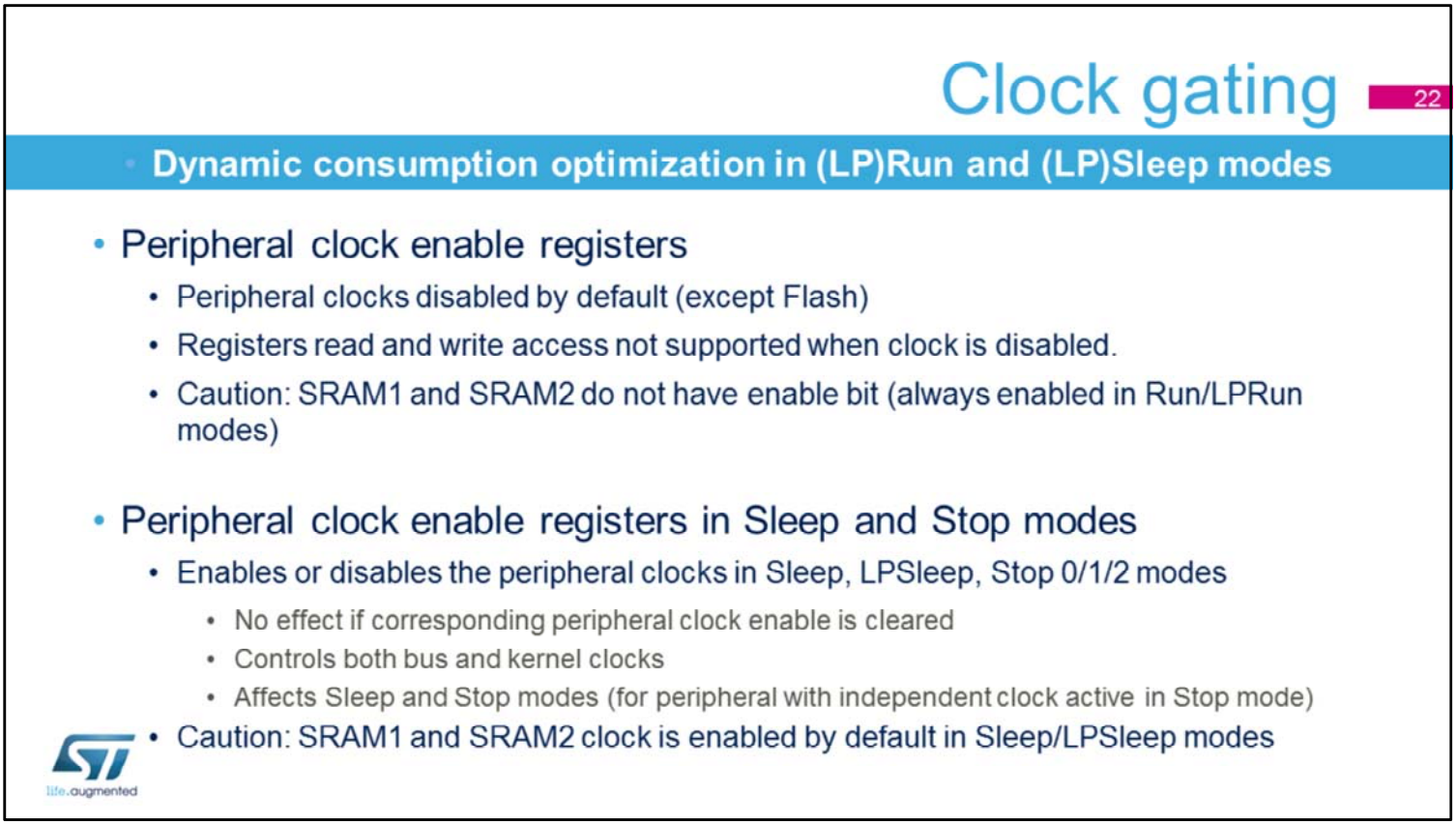
The system clock is selected between the HSI16, HSE, MSI and PLL output.
The maximum system clock frequency is 80 MHz. The APB1 and APB2 bus frequencies are also up to 80 MHz.
The maximum clock source frequency depends on the voltage scaling and power mode. The system clock is limited to 80 MHz in Range 1, 26 MHz in Range 2 and 2 MHz in Low-power run/Low-power sleep modes.



The clock tree is shown here. The AHB clock is generated from the system clock divided by the AHB prescaler, from 1 to 512. The AHB clock feeds the CPU, DMA, memories, and AHB peripherals. The 2 APB clocks are derived from the AHB clock, divided by the APB1 prescaler and the APB2 prescaler, each from 1 to 16. Several peripherals have their own clock independent from the system clock. This is the case for the USARTs, low-power UART, I2Cs, low-power timers, single-wire protocol master interface, ADC interface, serial audio interfaces, USB, random number generator, and SDMMC interface. All of these clocks can be selected from the internal or external oscillators.



The various clocks can be output on an I/O. The Microcontroller Clock Output feature allows you to output on a pin one of these seven clocks, HSI16, HSE, MSI, LSI, LSE, SYSCLK, and PLLCLK.
The low-speed clock output feature allows you to output on a pin the LSI or LSE clock. The low-speed clock output is available in Stop 0, Stop 1, Stop 2, Standby and Shutdown modes.



The dynamic power consumption can be optimized by using peripheral clock gating.
Each peripheral clock can be gated ON or OFF in Run and Low-power run mode, except SRAM1 and SRAM2 which are always clocked in Run and Low-power run modes. By default, the peripheral's clock is disabled, except the Flash clock which is enabled by default.
When a peripheral's clock is disabled, the peripheral's registers cannot be read or written.
Other registers allow for configuring the peripheral's clock during the Sleep and Low-power sleep modes. This also affects Stop 0, Stop 1 and Stop 2 modes for peripherals with an independent clock active in Stop modes. These control bits have no effect if the corresponding peripheral clock enable is cleared. By default the SRAM1 and SRAM2 clocks are enabled in Sleep and Low-power sleep modes. If they are not

needed, the SRAM clock enable bits should be disabled to reduce power consumption.

Interrupts

Interrupt event	Description
LSE clock security system	Set when a failure is detected in the LSE oscillator
HSE clock security system	Set when a failure is detected in the HSE oscillator
PLLSAI2 ready interrupt flag	Clock ready caused by PLLSAI2 lock
PLLSAI2 ready interrupt flag	Clock ready caused by PLLSAI1 lock
PLL ready interrupt flag	Clock ready caused by PLL lock
HSE ready	Clock ready caused by the HSE oscillator
HSI16 ready	Clock ready caused by the HSI16 oscillator
MSI ready	Clock ready caused by the MSI oscillator
LSE ready	Clock ready caused by the LSE oscillator
LSI ready	Clock ready caused by the LSI oscillator

This slide lists the RCC interrupts. The LSE and HSE clock security systems, the PLL ready, and all five oscillator ready signals can generate an interrupt.

Related peripherals

- Refer to these trainings linked to this peripheral, if any
  - STM32L4 Power control (PWR)
  - STM32L4 Interrupts (NVIC-EXTI)

In addition to this training, you may find the Power Control and Interrupt Controller trainings useful.

References

- For more details, please refer to following sources
  - AN2867 Oscillator design guide for STM8S, STM8A and STM32 microcontrollers
  - AN4736 How to calibrate STM32L4 internal RC oscillators

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For more details, please refer to application note AN2867, an oscillator design guide for STM8S, STM8A and STM32 microcontrollers and application note AN4736 which explains how to calibrate STM32L4 internal RC oscillators.

Differences with STM32L47x/48x devices

- The features listed below are not implemented in STM32L47x/48x devices
- HSI48 and Clock Recovery System (CRS).
  - A new internal oscillator HSI48 is available on all derivatives
  - It allows can drive USB, SDMMC and RNG
  - It can be coupled to a new Clock Recovery System for Crystal less solution.
  - It can be output on MCO pin
- HSI16 is a selectable input to SAI1/2 peripherals.
- PLLP division factor has been extended from [7,17] to [2-31] on all PLL.

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This slide presents the key differences between baseline STM32L47x/48x devices and other devices.
The features listed below are not implemented in STM32L47x/48x devices.
A new HSI48 internal oscillator is now available allowing a crystal less solution when coupled with the new Clock Recovery System (CRS).
The HSI48 clock can be output on the MCO pin.
On the audio side, the HSI16 is now a possible input to SAI peripherals and the PLLP division factor has been extended to the range 2-31 in order to allow more flexibility on the SAI input clock frequency.