Hello, and welcome to this presentation of the STM32U5 general-purpose IO interface. It covers the general-purpose input and output interface, and how it allows connectivity to the environment around the microcontroller.

GPIOs/LPGPIOs

- Up to 151 GPIOs, up to 133 or 166 MHz
- Up to 14 GPIOs on the dedicated VDDIO2 supply PG[15:2]
- Up to 16 LPGPIOs:
  - GPIOs that can be controlled as input or output in Stop 2 mode thanks to LPDMA

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The number of GPIOs depends on the STM32U5 product and package. Refer to the product datasheet for availability of peripherals according to package size.
The maximum frequency for very high-speed capable GPIOs is 166 MHz. It is 133 MHz for the other GPIOs.
VDDIO2 is the external power supply for 14 I/Os: port G[15 down to 2].
The VDDIO2 voltage level is independent of the VDD voltage and must preferably be connected to VDD when PG[15:2] are not used.
The LPGPIO allows dynamic I/O control in Stop 2 mode thanks to Low Power DMA.
Up to 16 I/Os can be configured as LPGPIOs.

High Speed Low Voltage (HSLV)

- Some I/Os support very high-speed mode thanks to new HSLV control bits in the GPIOx_HSLVR registers
  - Only I/Os with "_h" option support HSLV mode (refer to the I/O structure in the datasheet)
- The speed is improved by setting HSLV = 1 when VDDIOx < 2.7V
- Caution! HSLV must not be set if VDDIO > 2.7V (destructive !!…)
  - 2 option bytes forbid write access to the HSLV control bits and must be configured if needed:
    - IO_VDD_HSLV and IO_VDDIO2_HSLV
- Caution! Unless all I/Os of a communication peripheral support HSLV mode, this mode must not be set to avoid bad timing side effects

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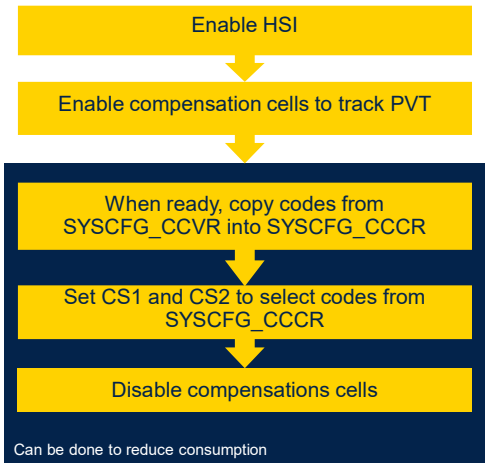
Some I/Os have the capability to increase their maximum speed at low voltage when configured in HSLV mode.
They are identified by the suffix _h in the data sheet.
The I/O HSLV bit controls whether the I/O output speed is optimized to operate at 3.3 V (default setting) or at 1.8 V (HSLV = 1).
Caution: The I/O HSLV configuration bit must not be set if the I/O supply (VDD or VDDIO2) is above 2.7 V.
Setting it while the voltage is higher than 2.7 V can damage the device.
The I/O HSLV bit can be only set when the corresponding option bit is activated: IO_VDD_HSLV or IO_VDDIO2_HSLV depending on the I/O supply.
There is no hardware protection associated with this

feature so it is recommended to use it only as a static configuration for fixed I/O supply.
High Speed Low Voltage should be disabled unless all I/Os connected to a particular peripheral support this capability.

I/O compensation cell

- I/O commutation slew rate (tfall / trise) can be adapted by software depending on Process, Voltage and Temperatures conditions, in order to reduce the I/O noise on the power supply
- Three compensation cells:
  - one for I/Os supplied by VDD
  - one for I/Os supplied by VDDIO2
  - one dedicated to GPIOs with HSPI alternate functions (AF) capabilities.
- Compensation cells can be used only when 1.6V ≤ VDDIOx ≤ 3.6 V
  - Enabled in the I/Os electrical characteristics



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The I/O commutation slew rate, affecting rise and fall times, can be adapted by software depending on Process, Voltage and Temperatures conditions, in order to reduce the I/O noise on the power supply.
The compensation cell can be used only when VDDIOx is within in the range of 1.6 V to 3.6 V.
Three compensation cells are embedded, one for the I/Os supplied by VDD, one for the I/Os supplied by VDDIO2, and one dedicated to GPIOs with HSPI alternate functions(AF) capabilities.
The I/O compensation cell generates an 8-bit value for the I/O buffer (4 bits for N-MOS and 4 bits for P-MOS), which depends on PVT operating conditions (process, voltage, temperature).

These bits are used to control the current slew-rate and output impedance in the I/O buffer.
By default, the compensation cells are disabled, and a fixed code is applied to all I/Os.
The following sequence should be implemented to enable the compensation cells:
1- The HSI is used by the compensation cells and must be enabled.
2- Enable the compensation cells in the SYSCFG compensation cell control/status register.
3- When enabled, the compensation cell tracks the PVT, and the 8-bit code is available in SYSCFG_CCVR once the ready bit is set.
4- If the Code Selection bit is cleared, the I/O receives the code from SYSCFG_CCVR, resulting from the compensation cell.
To reduce the power consumption, it is recommended to copy the code from SYSCFG_CCVR to SYSCFG_CCCR. After the result is ready, set the Code Selection bit and disable the compensation cell.
When the Code Selection bit is set, VDD I/O codes are received from the SYSCFG compensation cell code register and not from the cell, which reduces the consumption.

I/O target spec with: VDDIO ≥ 2.7V

OSPEED[1:0]	All I/Os except FT_c	FT_c
00 – low speed	12.5 MHz with 50 pF	10 MHz with 50 pF
01 – medium speed	55 MHz with 30 pF	25 MHz with 50 pF
10 – high speed	133 MHz with 10 pF	40 MHz with 50 pF
11 – very high speed	133 MHz with 10 pF for I/Os without “v” option 166 MHz with 10 pF for I/Os with “v” option	Not supported

FT_c : I/O with USB Type-C power delivery function (PA15/PB15)
FT_v : I/O very high-speed capable

Caution! Unless all I/Os of a communication peripheral support Very High Speed “v” mode, this mode must not be set to avoid bad timing side effects

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The following slides indicate how to select the OSPEED value in the GPIO port output speed register according to the following parameters:

- VDDIO power supply range
- High Speed Low Voltage mode enabled or disabled.

For each OSPEED value, the maximum frequency also depends on the capacitive load.

The same assumptions apply to all tables in order to perform coherent comparisons:

- 50 picofarad for OSPEED equal to 0
- 30 picofarad for OSPEED equal to 1
- 10 picofarad for OSPEED equal to 2 and 3.

The larger the capacitive load, the lower the maximum frequency.

This presentation does not provide the exhaustive list of all combinations; please refer to the data sheet.
The table in this slide is relevant when the VDDIO power supply is greater than or equal to 2.7 volts.
The first column contains the value to be programmed in the OSPEED field.
The second column applies to all I/Os except 5V-tolerant I/Os with USB type-C power delivery function.
When very high speed is chosen, a second parameter has to be taken into account: the very high speed capability.
Very high speed configuration should not be selected unless all I/Os connected to a particular peripheral support this capability.
The third column applies to 5V-tolerant I/Os with the USB type-C power delivery function.

I/O target spec with: 1.58V < VDDIO < 2.7V with HSLV=1

OSPEED[1:0]	All I/Os with “h” option
00 – low speed	10 MHz with 50 pF
01 – medium speed	50 MHz with 30 pF
10 – high speed	100 MHz with 10 pF
11 – very high speed	100 MHz with 10 pF for I/Os without “v” option 150 MHz with 10 pF for I/Os with “v” option

FT_v : I/O very high-speed capable

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This table is relevant when the VDDIO power supply is in the range of 1.58 to 2.7 Volts and High Speed Low Voltage mode is enabled.
In comparison to the table on the next slide, the maximum frequency is higher when HSLV is enabled.

I/O target spec with: 1.58V < VDDIO < 2.7V with HSLV=0

OSPEED[1:0]	All I/Os except FT_c	FT_c
00 – low speed	5 MHz with 50 pF	5 MHz with 50 pF
01 – medium speed	12.5 MHz with 30 pF	10 MHz with 50 pF
10 – high speed	40 MHz with 10 pF	20 MHz with 50 pF
11 – very high speed	40 MHz with 10 pF for I/Os without “v” option 50 MHz with 10 pF for I/Os with “v” option	Not supported

FT_c : I/O with the USB Type-C power delivery function (PA15/PB15)
FT_v : I/O very high-speed capable

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This table is relevant when the VDDIO power supply is in the range of 1.58 to 2.7 Volts and High Speed Low Voltage mode is disabled.
The third column applies to 5V-tolerant I/Os with the USB type-C power delivery function.
Note that the maximum frequency of these FT_c IOs is always provided for a 50 picofarad capacitive load.

I/O target spec with: 1.08V < VDDIO < 1.58V with HSLV=1

OSPEED[1:0]	FT_s I/Os
00 – low speed	4 MHz with 50 pF
01 – medium speed	10 MHz with 30 pF
10 – high speed	15 MHz with 10 pF
11 – very high speed	15 MHz with 10 pF for I/Os without “v” option 25 MHz with 10 pF for I/Os with “v” option

FT_s: I/O supplied by VDDIO2

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This table is relevant when the VDDIO power supply is in the range of 1.08 to 1.58 Volts and High Speed Low Voltage mode is enabled.

I/O target spec with: 1.08V < VDDIO < 1.58V with HSLV=0

OSPEED[1:0]	FT_s I/Os
00 – low speed	1 MHz with 50 pF
01 – medium speed	2.5 MHz with 30 pF
10 – high speed	5 MHz with 10 pF
11 – very high speed	5 MHz (1) for I/Os without “v” option 5 MHz (1) for I/Os with “v” option

FT_s : I/O supplied by VDDIO2

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This table is relevant when the VDDIO power supply is in the range of 1.08 to 1.58 Volts and High Speed Low Voltage mode is disabled.

GPIO TrustZone Security

- Each I/O pin of the GPIO port can be individually configured as secure/non-secure in the GPIOx_SECCFGR register
  - Secure I/O access from non-secure is RAZ/WI

Security configuration		Alternate function
Peripheral	**I/O pin**	
Secure	Secure*	OK
Non-secure*		
Secure	Non-secure	Zero
Non-secure		OK

Security configuration		Analog value
Analog peripheral	**Allocated I/O pin with analog switch**	
Secure	Secure	OK
Non-secure		zero
Secure	Non-secure	zero
Non-secure		OK

*Default configuration after reset

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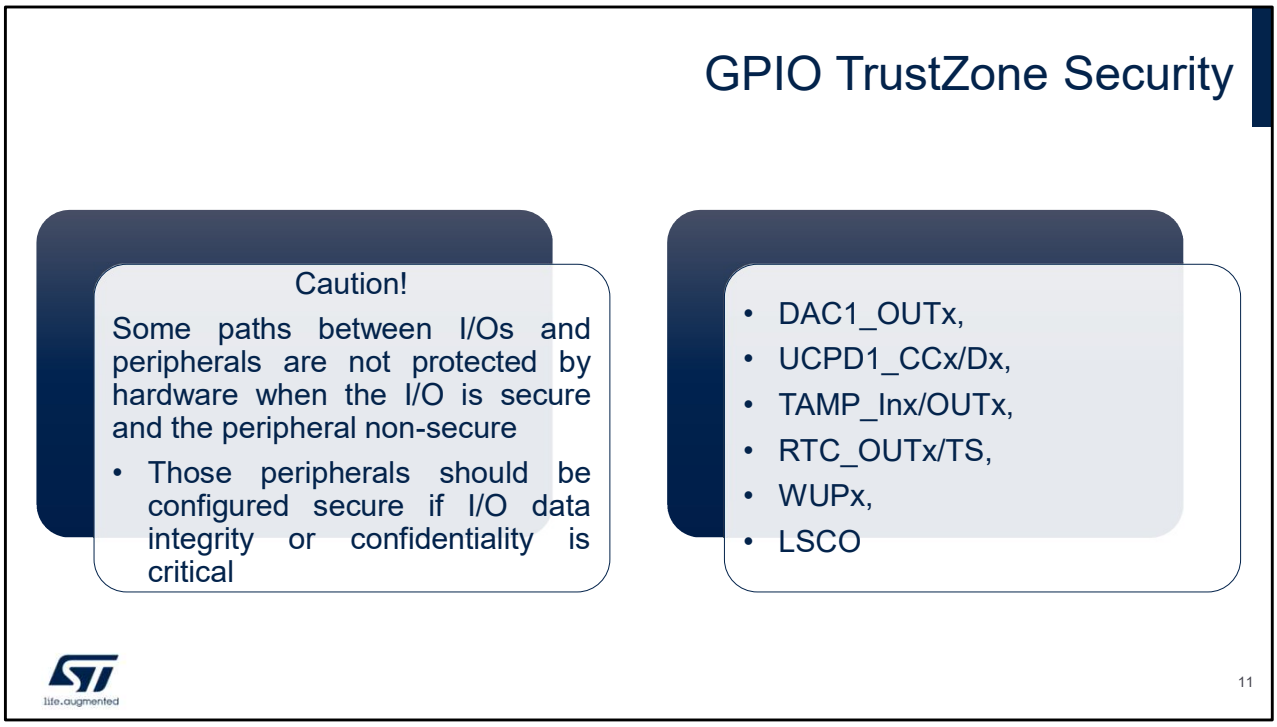
When the TrustZone is active, each I/O pin of the GPIO port can be individually configured as secure through the GPIOx_SECCFGR register.
When the selected I/O pin is configured as secure, its corresponding configuration bits for alternate function, mode selection, and I/O data are secure against a non-secure access.
In the case of a non-secure access, these fields are read as zero, and writes are ignored.
I/Os with peripheral functions are also conditioned by the peripheral security configuration.
In peripherals for which the I/O pin selection is done through alternate functions registers: if the peripheral is configured as secure, it cannot be connected to a non-

secure I/O pin.
If this is not respected, the input data to the secure peripheral is forced to 0 and the output pin value is forced to 0, thus avoiding any secure information leak through non-secure I/Os.
For I/Os with analog switches, directly controlled by peripherals, such as the ADC for instance: if the I/O is secure, the I/O analog switch cannot be controlled by a non-secure peripheral.
If this is not respected, the switch remains open. This prevents the redirection of secure data to a non-secure peripheral or I/O through the analog path.



The pin function is generally controlled by the GPIO Alternate Function Registers.
However, the so-called additional functions are directly selected and enabled through peripheral registers, not involving the GPIO module.
Some of the paths between these I/Os additional functions and peripherals are not blocked if the I/O is secure and the peripheral is non-secure.
Therefore it is recommended to configure those peripherals as secure even when not used by the application.
The list of these additional functions is indicated on the right.

GPIO Privileged/Unprivileged mode

All GPIO registers can be read and written by privileged and unprivileged accesses, whatever the security state: secure or non-secure

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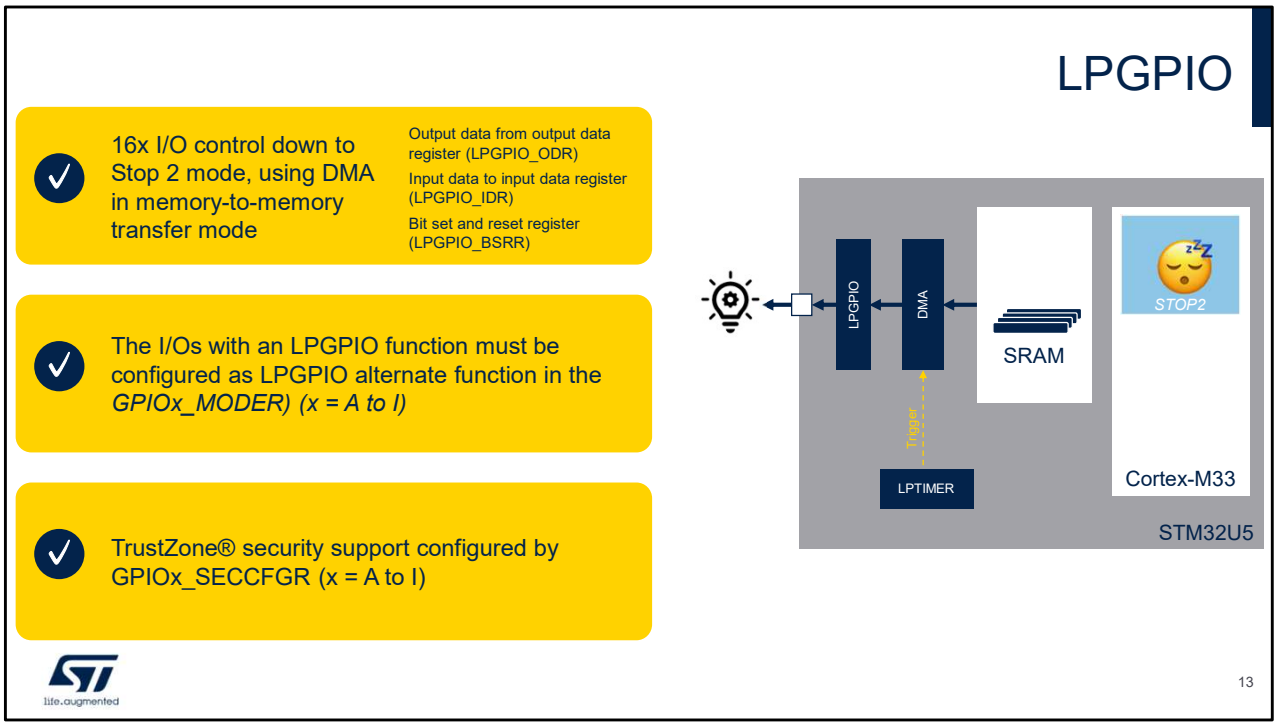
The GPIO module filters out accesses to its memory-mapped registers according to the security level, but not the privilege level.



The STM32U5 supports low-power background autonomous mode (LPBAM), which allows peripherals to be functional and autonomous in Stop 0, Stop 1 and Stop 2 modes, without any software running.
In Stop 2, only 16 low power GPIOs remain functional. Each of them can be enabled independently by programming its alternate function as a low power GPIO. Then LPGPIO-specific registers are used to capture data when configured as an input or to force the state when configured as an output.
The security attribute is programmed in the associated GPIO Security configuration register.
An example of LPBAM is shown on the right.
A low power timer periodically triggers a DMA transfer

which writes data from SRAM4 to LPGPIO registers in order to generate a particular waveform. Making a LED blink is an example.

Low-power modes

Mode	I/O state
RUN, SLEEP	Active
STOP 0	
STOP 1	
STOP 2	Only LPGPIOs remain active
STOP 3	I/Os can be configured with internal pull-up, pull-down or floating in Standby mode
STANDBY	
SHUTDOWN	I/Os can be configured with internal pull-up, pull-down or floating in Shutdown mode but the configuration is lost when exiting the Shutdown mode
RESET	During and just after reset, the alternate functions are not active and most of the I/O ports are configured in analog mode

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GPIOs are active in Run, Sleep, Stop 0 and Stop 1 modes.
Lo-power GPIOs are active in Run, Sleep, Stop 0, Stop 1 and Stop 2 modes.
In Stop 3, Standby and Shutdown, the only available configuration is input with internal pull-up, pull-down resistor or floating input.
When exiting Shutdown mode, the I/O configuration is lost.
When the microcontroller is under reset, most I/O pins are forced into an analog input mode.

Thank you

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Thank you for attending this presentation on STM32U5's GPIO and LPGPIO.
Please refer to the following presentations for more information if needed:

- USB Type-C Power Delivery (UCPD)
- Power Management (PWR)
- Low-power background autonomous mode (LPBAM).