



Introduction

This programming manual describes how to program the STM32F101xF/G and STM32F103xF/G Flash memory of XL-density microcontrollers. For convenience, these will be referred to as STM32F10xFG in the rest of this document unless otherwise specified.

The STM32F10xFG embedded Flash memory can be programmed using in-circuit programming or in-application programming.

The **in-circuit programming (ICP)** method is used to update the entire contents of the Flash memory, using the JTAG, SWD protocol or the boot loader to load the user application into the microcontroller. ICP offers quick and efficient design iterations and eliminates unnecessary package handling or socketing of devices.

In contrast to the ICP method, **in-application programming (IAP)** can use any communication interface supported by the microcontroller (I/Os, USB, CAN, UART, I²C, SPI, etc.) to download programming data into memory. IAP allows the user to re-program the Flash memory while the application is running. Nevertheless, part of the application has to have been previously programmed in the Flash memory using ICP.

The Flash interface implements instruction access and data access based on the AHB protocol. It implements a prefetch buffer that speeds up CPU code execution. It also implements the logic necessary to carry out Flash memory operations (Program/Erase). Program/Erase operations can be performed over the whole product voltage range. Read/Write protections and option bytes are also implemented.

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Glossary

This section gives a brief definition of acronyms and abbreviations used in this document:

- **XL-density devices** are STM32F101xF/G and STM32F103xF/G microcontrollers where the Flash memory density ranges between 512 and 1024 Kbytes.
- The Cortex-M3 core integrates two debug ports:
 - JTAG debug port (JTAG-DP) provides a 5-pin standard interface based on the Joint Test Action Group (JTAG) protocol.
 - SWD debug port (SWD-DP) provides a 2-pin (clock and data) interface based on the Serial Wire Debug (SWD) protocol.
For both the JTAG and SWD protocols please refer to the *Cortex M3 Technical Reference Manual*.
- Word: data/instruction of 32-bit length
- Half word: data/instruction of 16-bit length
- Byte: data of 8-bit length
- FPEC (Flash memory program/erase controller): write operations to the main memory and the information block are managed by an embedded Flash program/erase controller (FPEC).
- IAP (in-application programming): IAP is the ability to re-program the Flash memory of a microcontroller while the user program is running.
- ICP (in-circuit programming): ICP is the ability to program the Flash memory of a microcontroller using the JTAG protocol, the SWD protocol or the boot loader while the device is mounted on the user application board.
- I-Code: this bus connects the Instruction bus of the Cortex-M3 core to the Flash instruction interface. Prefetch is performed on this bus.
- D-Code: this bus connects the D-Code bus (literal load and debug access) of the Cortex-M3 to the Flash Data Interface.
- Option bytes: product configuration bits stored in the Flash memory
- OBL: option byte loader.
- AHB: advanced high-performance bus.

1 Overview

1.1 Features

- Up to 1 Mbytes of Flash memory
- Dual bank architecture for read-while-write (RWW) capability
 - Bank 1: fixed size of 512 Kbytes
 - Bank 2: up to 512 Kbytes
- Flash memory interface (FLITF)
 - Read interface with prefetch buffer (2 × 64-bit words) for each bank
 - Option byte loader
 - Flash program/erase operation
 - Read/write protection
 - Low-power mode

1.2 Flash module organization

The Flash memory is divided into an information block and a main memory block containing 512 pages of 2 Kbytes each as shown in [Table 1](#).

An additional memory area contains the Flash memory registers.

Table 1. XL-density Flash module organization

Block		Name	Base addresses	Size (bytes)
Main memory	Bank 1	Page 0	0x0800 0000 - 0x0800 07FF	2 Kbytes
		Page 1	0x0800 0800 - 0x0800 0FFF	2 Kbytes
	
		Page 255	0x0807 F800 - 0x0807 FFFF	2 Kbytes
	Bank 2	Page 256	0x0808 0000 - 0x0808 07FF	2 Kbytes
		Page 257	0x0808 0800 - 0x0808 0FFF	2 Kbytes
		⋮	⋮	⋮
		Page 511	0x080F F800 - 0x080F FFFF	2 Kbytes
Information block	System memory	0x1FFF E000 - 0x1FFF F7FF	6 Kbytes	
	Option bytes	0x1FFF F800 - 0x1FFF F80F	16	

Table 1. XL-density Flash module organization (continued)

Block	Name	Base addresses	Size (bytes)
Flash memory interface registers	FLASH_ACR	0x4002 2000 - 0x4002 2003	4
	FLASH_KEYR	0x4002 2004 - 0x4002 2007	4
	FLASH_OPTKEYR	0x4002 2008 - 0x4002 200B	4
	FLASH_SR	0x4002 200C - 0x4002 200F	4
	FLASH_CR	0x4002 2010 - 0x4002 2013	4
	FLASH_AR	0x4002 2014 - 0x4002 2017	4
	Reserved	0x4002 2018 - 0x4002 201B	4
	FLASH_OBR	0x4002 201C - 0x4002 201F	4
	FLASH_WRPR	0x4002 2020 - 0x4002 2023	4
	Reserved	0x4002 2024 - 0x4002 2043	32
	FLASH_KEYR2	0x4002 2044 - 0x4002 2047	4
	Reserved	0x4002 2048 - 0x4002 204B	4
	FLASH_SR2	0x4002 204C - 0x4002 204F	4
	FLASH_CR2	0x4002 2050 - 0x4002 2053	4
	FLASH_AR2	0x4002 2054 - 0x4002 2057	4

The Flash memory is organized as 32-bit wide memory cells that can be used for storing both code and data constants. The Flash module is located at a specific base address in the memory map of the microcontroller. For the base address, please refer to the related *STM32F101xF/G and STM32F103xF/G reference manual*.

The information block is divided into two parts:

- System memory is used to boot the device in System memory boot mode. The area is reserved to STMicroelectronics and contains the boot loader which is used to reprogram the Flash memory using the USART1 or USART2 (remapped) serial interface. It is programmed by ST when the device is manufactured, and protected against spurious write/erase operations. For further details please refer to AN2606.
- Option bytes

Write operations to the main memory block and the option bytes are managed by an embedded Flash program/erase Controller (FPEC). The high voltage needed for program/erase operations is generated internally.

The main Flash memory can be protected against different types of unwanted access (read/write/erase). There are two types of protection:

- Page Write Protection
- Read Protection

Refer to [Section 2.4 on page 14](#) for more details.

During a write operation to the Flash memory, any attempt to read the Flash memory will stall the bus. The read operation will proceed correctly once the write operation has completed. This means that code or data fetches cannot be made while a write/erase operation is ongoing.

For write and erase operations on the Flash memory (write/erase), the internal RC oscillator (HSI) must be ON.

The Flash memory can be programmed and erased using in-circuit programming and in-application programming.

Note: In the low-power modes, all Flash memory accesses are aborted. Refer to the *STM32F10xFG reference manual* for further information.

1.3 Dual bank architecture

The XL-density Flash memory features a dual bank architecture based on bank 1 (512 Kbytes) and bank 2 (up to 512 Kbytes). This architecture supports the RWW (read-while-write) capability. This means that while a read or program operation is performed in a bank, the other bank can be accessed for another operation (read or program) without the need to wait for the End of Operation on the first bank.

The registers that control the Flash memory are divided into two categories:

- Registers for Flash memory access control (FLASH_ACR) and option bytes management (FLASH_OPTKEYR, FLASH_OBR and FLASH_WRP). These registers are common to both banks. Option bytes programming is controlled through FLASH_CR register.
- A dedicated set of registers allows to control and program each bank; FLASH_KEYRx, FLASH_SRx, FLASH_CRx and FLASH_ARx. However, the programming procedure is identical for both banks. As an example, to perform a page erase on bank 1, the user code must write to FLASH_CR register, while it must write to FLASH_CR2 for bank 2.

In the rest of the document:

- [Section 2.2](#) to [Section 2.3.4](#) apply to both banks. However for simplification purposes, only one bank will be referred to. The user code must use the registers corresponding to the selected bank.
- [Section 2.3.5](#) and [Section 2.4](#) describe option bytes management and are consequently common to both banks. The user code must program the same set of registers whatever the bank.

2 Reading/programming the STM32F101xF/G and STM32F103xF/G embedded Flash memory

2.1 Introduction

This section describes how to read from or program to the STM32F101xF/G and STM32F103xF/G embedded Flash memory.

2.2 Read operation

The embedded Flash module can be addressed directly, as a common memory space. Any data read operation accesses the content of the Flash module through dedicated read senses and provides the requested data.

The read interface consists of a read controller on one side to access the Flash memory and an AHB interface on the other side to interface with the CPU. The main task of the read interface is to generate the control signals to read from the Flash memory and to prefetch the blocks required by the CPU. The prefetch block is only used for instruction fetches over the I-Code bus. The Literal pool is accessed over the D-Code bus. Since these two buses have the same Flash memory as target, D-code bus accesses have priority over prefetch accesses.

2.2.1 Instruction fetch

The Cortex-M3 fetches the instruction over the I-Code bus and the literal pool (constant/data) over the D-code bus. The prefetch block aims at increasing the efficiency of I-Code bus accesses.

Prefetch buffer

The prefetch buffer is 2 blocks wide where each block consists of 8 bytes. The prefetch blocks are direct-mapped. A block can be completely replaced on a single read to the Flash memory as the size of the block matches the bandwidth of the Flash memory.

The implementation of this prefetch buffer makes a faster CPU execution possible as the CPU fetches one word at a time with the next word readily available in the prefetch buffer. This implies that the acceleration ratio will be of the order of 2 assuming that the code is aligned at a 64-bit boundary for the jumps.

Prefetch controller

The prefetch controller decides to access the Flash memory depending on the available space in the prefetch buffer. The Controller initiates a read request when there is at least one block free in the prefetch buffer.

After reset, the state of the prefetch buffer is on.

The prefetch buffer should be switched on/off only when SYSCLK is lower than 24 MHz and no prescaler is applied on the AHB clock (SYSCLK must be equal to HCLK). The prefetch buffer is usually switched on/off during the initialization routine, while the microcontroller is running on the internal 8 MHz RC (HSI) oscillator.

Note: The prefetch buffer must be kept on (`FLASH_ACR[4]='1'`) when using a prescaler different from 1 on the AHB clock.

In case of non-availability of a high frequency clock in the system, Flash memory accesses can be made on a half cycle of HCLK (AHB clock), the frequency of HCLK permitting (half-cycle access can only be used with a low-frequency clock of less than 8 MHz that can be obtained with the use of HSI or HSE but not of PLL). This mode can be chosen by setting a control bit in the Flash access control register.

Note: Half-cycle access cannot be used when there is a prescaler different from 1 on the AHB clock.

Access time tuner

In order to maintain the control signals to read the Flash memory, the ratio of the prefetch controller clock period to the access time of the Flash memory has to be programmed in the Flash access control register. This value gives the number of cycles needed to maintain the control signals of the Flash memory and correctly read the required data. After reset, the value is zero and only one cycle is required to access the Flash memory.

2.2.2 D-Code interface

The D-Code interface consists of a simple AHB interface on the CPU side and a request generator to the Arbiter of the Flash access controller. D-code accesses have priority over prefetch accesses. This interface uses the Access Time Tuner block of the prefetch buffer.

2.2.3 Flash access controller

Mainly, this block is a simple arbiter between the read requests of the prefetch/I-code and D-Code interfaces.

D-Code interface requests have priority over I-Code requests.

2.3 Flash program and erase controller (FPEC)

The FPEC block handles the program and erase operations of the Flash memory. The FPEC consists of twelve 32-bit registers.

- Flash access control register (FLASH_ACR), common to bank 1 and bank 2
- FPEC key register (FLASH_KEYR), dedicated to bank 1
- Option byte key register (FLASH_OPTKEYR), common to bank 1 and bank 2
- Flash control register (FLASH_CR), dedicated to bank 1 and option bytes programming
- Flash status register (FLASH_SR), dedicated to bank 1
- Flash address register (FLASH_AR), dedicated to bank 1
- Option byte register (FLASH_OBR), common to bank 1 and bank 2
- Write protection register (FLASH_WRPR), common to bank 1 and bank 2
- FPEC key register2 (FLASH_KEYR2), dedicated to bank 2
- Flash control register2 (FLASH_CR2), dedicated to bank 2
- Flash status register2 (FLASH_SR2), dedicated to bank 2
- Flash address register2 (FLASH_AR2), dedicated to bank 2

An ongoing Flash memory operation will not block the CPU as long as the CPU does not access the Flash memory.

2.3.1 Key values

The key values are as follows:

- RDPRT key = 0x00A5
- KEY1 = 0x45670123
- KEY2 = 0xCDEF89AB

2.3.2 Unlocking the Flash memory

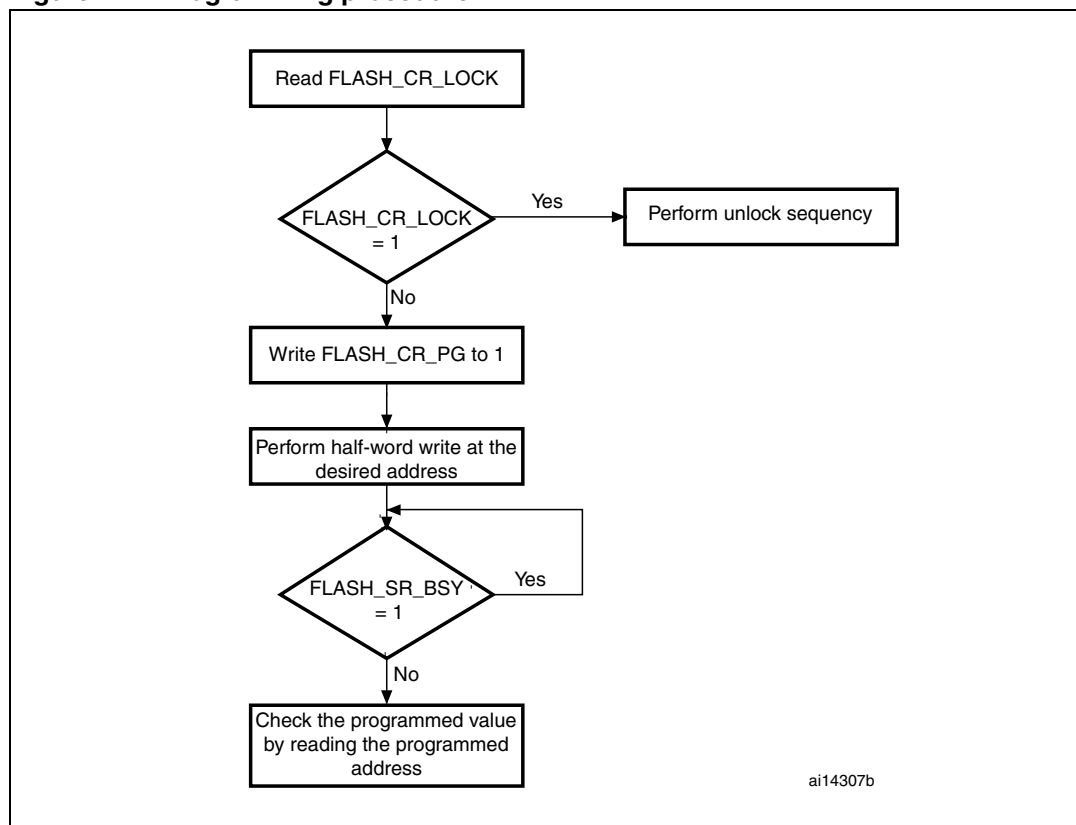
After reset, the FPEC block is protected. The FLASH_CR register is not accessible in write mode. An unlocking sequence should be written to the FLASH_KEYR register to open up the FPEC block. This sequence consists of two write cycles, where two key values (KEY1 and KEY2) are written to the FLASH_KEYR address (refer to [Section 2.3.1](#) for key values). Any wrong sequence locks up the FPEC block and FLASH_CR register until the next reset.

Also a bus error is returned on a wrong key sequence. This is done after the first write cycle if KEY1 does not match, or during the second write cycle if KEY1 has been correctly written but KEY2 does not match. The FPEC block and FLASH_CR register can be locked by the user's software by writing the LOCK bit of the FLASH_CR register to 1. In this case, the FPEC can be unlocked by writing the correct sequence of keys into FLASH_KEYR.

2.3.3 Main Flash memory programming

The main Flash memory can be programmed 16 bits at a time. The program operation is started when the CPU writes a half-word into a main Flash memory address with the PG bit of the FLASH_CR register set. Any attempt to write data that are not half-word long will result in a bus error response from the FPEC. If a read/write operation is initiated during programming, (BSY bit set), the CPU stalls until the ongoing main Flash memory programming is over.

Figure 1. Programming procedure



Standard programming

In this mode the CPU programs the main Flash memory by performing standard half-word write operations. The PG bit in the FLASH_CR register must be set. FPEC preliminarily reads the value at the addressed main Flash memory location and checks that it has been erased. If not, the program operation is skipped and a warning is issued by the PGERR bit in FLASH_SR register (the only exception to this is when 0x0000 is programmed. In this case, the location is correctly programmed to 0x0000 and the PGERR bit is not set). If the addressed main Flash memory location is write-protected by the FLASH_WRPFR register, the program operation is skipped and a warning is issued by the WRPRTERR bit in the FLASH_SR register. The end of the program operation is indicated by the EOP bit in the FLASH_SR register.

The main Flash memory programming sequence in standard mode is as follows:

- Check that no main Flash memory operation is ongoing by checking the BSY bit in the FLASH_SR register.
- Set the PG bit in the FLASH_CR register.
- Perform the data write (half-word) at the desired address.
- Wait for the BSY bit to be reset.
- Read the programmed value and verify.

Note: The registers are not accessible in write mode when the BSY bit of the FLASH_SR register is set.

2.3.4 Flash memory erase

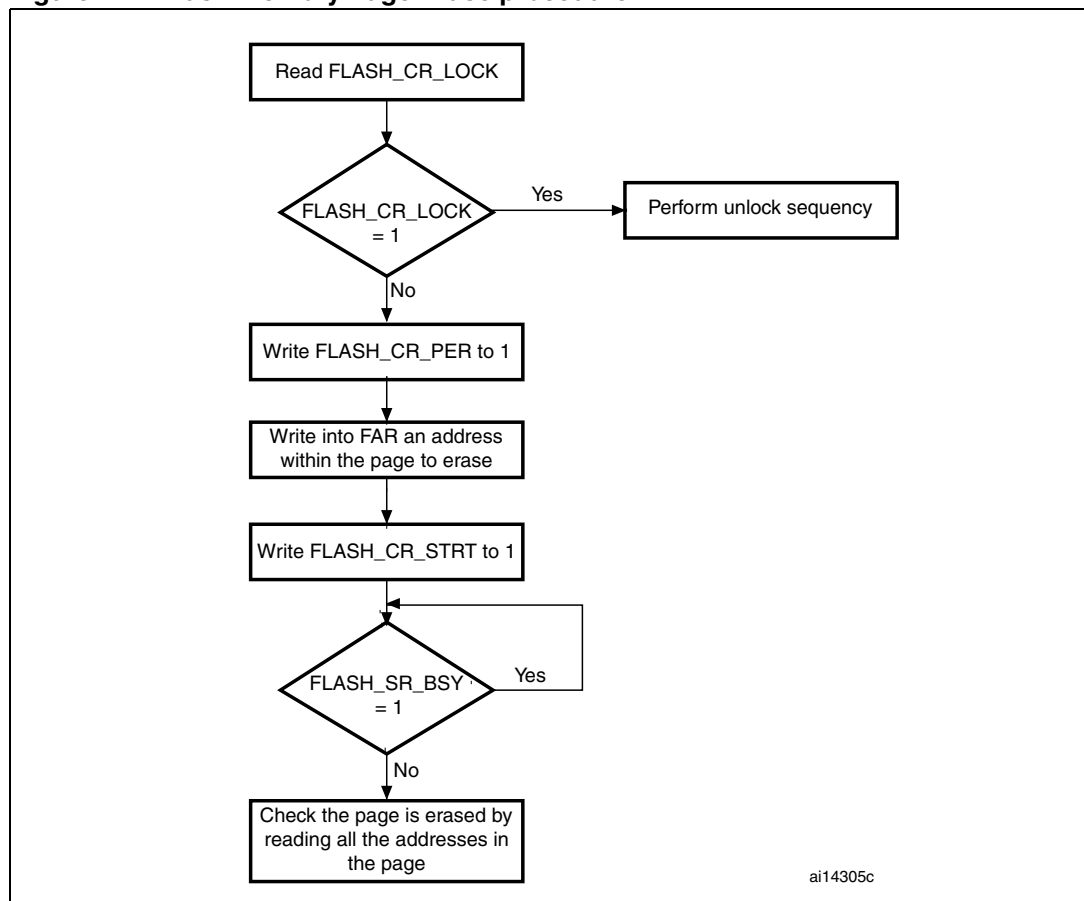
The Flash memory can be erased page by page or completely (Mass Erase).

Page Erase

A page of the Flash memory can be erased using the Page Erase feature of the FPEC. To erase a page, the procedure below should be followed:

- Check that no Flash memory operation is ongoing by checking the BSY bit in the FLASH_CR register
- Set the PER bit in the FLASH_CR register
- Program the FLASH_AR register to select a page to erase
- Set the STRT bit in the FLASH_CR register
- Wait for the BSY bit to be reset
- Read the erased page and verify

Figure 2. Flash memory Page Erase procedure



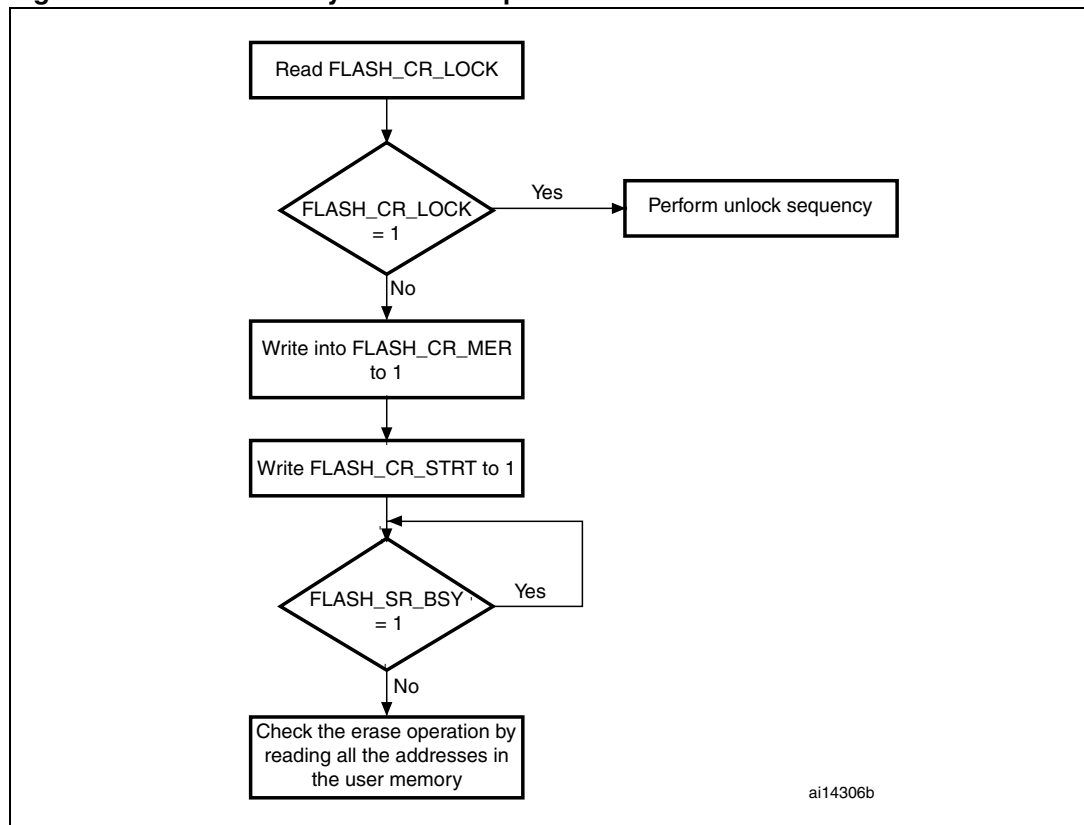
Mass Erase

The Mass Erase command can be used to completely erase the user pages of the Flash memory. The information block is unaffected by this procedure. The following sequence is recommended:

- Check that no Flash memory operation is ongoing by checking the BSY bit in the FLASH_SR register
- Set the MER bit in the FLASH_CR register
- Set the STRT bit in the FLASH_CR register
- Wait for the BSY bit to be reset
- Read all the pages and verify

Note: To perform a mass erase on the whole Flash memory, a mass erase must be issued to bank 1 and bank 2.

Figure 3. Flash memory Mass Erase procedure



2.3.5 Option byte programming

The option bytes are programmed differently from normal user addresses. The number of option bytes is limited to 8 (4 for write protection, 1 for read protection, 1 for configuration and 2 for user data storage). After unlocking the FPEC, the user has to authorize the programming of the option bytes by writing the same set of KEYS (KEY1 and KEY2) to the FLASH_OPTKEYR register to set the OPTWRE bit in the FLASH_CR register (refer to [Section 2.3.1](#) for key values). Then the user has to set the OPTPG bit in the FLASH_CR register and perform a half-word write operation at the desired Flash address.

FPEC preliminarily reads the value of the addressed option byte and checks that it has been erased. If not, the program operation is skipped and a warning is issued by the PGERR bit in the FLASH_SR register. The end of the program operation is indicated by the EOP bit in the FLASH_SR register.

The FPEC takes the LSB and automatically computes the MSB (which is the complement of the LSB) and starts the programming operation. This guarantees that the option byte and its complement are always correct.

The sequence is as follows:

- Check that no Flash memory operation is ongoing by checking the BSY bit in the FLASH_SR register.
- Unlock the OPTWRE bit in the FLASH_CR register.
- Set the OPTPG bit in the FLASH_CR register.
- Write the data (half-word) to the desired address.
- Wait for the BSY bit to be reset.
- Read the programmed value and verify.

When the Flash memory read protection option is changed from protected to unprotected, a Mass Erase of the main Flash memory is performed before reprogramming the read protection option. If the user wants to change an option other than the read protection option, then the mass erase is not performed. The erased state of the read protection option byte protects the Flash memory.

Erase procedure

The option byte erase sequence (OPTERASE) is as follows:

- Check that no Flash memory operation is ongoing by reading the BSY bit in the FLASH_SR register.
- Unlock the OPTWRE bit in the FLASH_CR register.
- Set the OPTER bit in the FLASH_CR register.
- Set the STRT bit in the FLASH_CR register.
- Wait for BSY to reset.
- Read the erased option bytes and verify.

2.4 Protections

The user area of the Flash memory can be protected against read by untrusted code. The pages of the Flash memory can also be protected against unwanted write due to loss of program counter contexts. The write-protection granularity is two pages.

2.4.1 Read protection

The read protection is activated by setting the RDP option byte and then, by applying a system reset to reload the new RDP option byte.

Note: If the read protection is set while the debugger is still connected through JTAG/SWD, apply a POR (power-on reset) instead of a system reset (without debugger connection).

Once the protection byte has been programmed:

- Main Flash memory read access is not allowed except for the user code (when booting from main Flash memory itself with the debug mode not active).
- Pages 0-1 are automatically write-protected. The rest of the memory can be programmed by the code executed from the main Flash memory (for IAP, constant storage, etc.), but it is protected against write/erase (but not against mass erase) in debug mode or when booting from the embedded SRAM.
- All features linked to loading code into and executing code from the embedded SRAM are still active (JTAG/SWD and boot from embedded SRAM) and this can be used to disable the read protection. When the read protection option byte is altered to a memory-unprotect value, a mass erase is performed.
- When booting from the embedded SRAM, Flash memory accesses through the code and through data read using DMA1 and DMA2 are not allowed.
- Flash memory access through data read using JTAG, SWV (serial wire viewer), SWD(serial wire debug), ETM and boundary scan are not allowed.

The Flash memory is protected when the RDP option byte and its complement contain the pair of values shown in [Table 2](#).

Table 2. Flash memory protection status

RDP byte value	RDP complement value	Read protection status
0xFF	0xFF	Protected
RDPRT	Complement of RDP byte	Not protected
Any value	Not the complement value of RDP	Protected

Note: Erasing the option byte block will not trigger a mass erase as the erased value (0xFF) corresponds to a protected value.

Unprotection

To disable the read protection from the embedded SRAM:

- Erase the entire option byte area. As a result, the read protection code (RDP) will be 0xFF. At this stage the read protection is still enabled.
- Program the correct RDP code 0x00A5 to unprotect the memory. This operation first forces a Mass Erase of the main Flash memory. Mass erase is performed both on bank 1 and bank 2.
- Reset the device (POR Reset) to reload the option bytes (and the new RDP code) and, to disable the read protection.

Note: The read protection can be disabled using the boot loader (in this case only a System Reset is necessary to reload the option bytes). For more details refer to AN2606.

2.4.2 Write protection

From page 0 to page 61, write protection is implemented with a granularity of two pages at a time. The remaining memory block (from page 62 to page 511) is write-protected at once.

If a program or an erase operation is performed on a protected page, the Flash memory returns a protection error flag on the Flash memory Status Register (FLASH_SR).

The write protection is activated by configuring the WRP[3:0] option bytes, and then by applying a system reset to reload the new WRPx option bytes.

Unprotection

To disable the write protection, two application cases are provided:

- Case 1: Read protection disabled after the write unprotection:
 - Erase the entire option byte area by using the OPTER bit in the Flash memory control register (FLASH_CR)
 - Program the correct RDP code 0x00A5 to unprotect the memory. This operation first forces a Mass Erase of the main Flash memory. Mass erase is performed both on bank 1 and bank 2.
 - Reset the device (system reset) to reload the option bytes (and the new WRP[3:0] bytes), and to disable the write protection
- Case 2: Read protection maintained active after the write unprotection, useful for in-application programming with a user boot loader:
 - Erase the entire option byte area by using the OPTER bit in the Flash memory control register (FLASH_CR)
 - Reset the device (system reset) to reload the option bytes (and the new WRP[3:0] bytes), and to disable the write protection.

2.4.3 Option byte block write protection

The option bytes are always read-accessible and write-protected by default. To gain write access (Program/Erase) to the option bytes, a sequence of keys (same as for lock) has to be written into the OPTKEYR. A correct sequence of keys gives write access to the option bytes and this is indicated by OPTWRE in the FLASH_CR register being set. Write access can be disabled by resetting the bit through software.

2.5 Option byte description

There are eight option bytes. They are configured by the end user depending on the application requirements. As a configuration example, the watchdog may be selected in hardware or software mode.

A 32-bit word is split up as follows in the option bytes.

Table 3. Option byte format

31-24	23-16	15 -8	7-0
complemented option byte1	Option byte 1	complemented option byte0	Option byte 0

The organization of these bytes inside the information block is as shown in [Table 4](#).

The option bytes can be read from the memory locations listed in [Table 4](#) or from the Option byte register (FLASH_OBR).

Note: The new programmed option bytes (user, read/write protection) are loaded after a system reset.

Table 4. Option byte organization

Address	[31:24]	[23:16]	[15:8]	[7:0]
0x1FFF F800	nUSER	USER	nRDP	RDP
0x1FFF F804	nData1	Data1	nData0	Data0
0x1FFF F808	nWRP1	WRP1	nWRP0	WRP0
0x1FFF F80C	nWRP3	WRP3	nWRP2	WRP2

Table 5. Description of the option bytes

Flash memory address	Option bytes
0x1FFF F800	<p>Bits [31:24]: nUSER</p> <p>Bits [23:16]: USER: User option byte (stored in FLASH_OBR[9:2]) This byte is used to configure the following features:</p> <ul style="list-style-type: none"> - Select the Flash bank to boot from: bank 1 or bank 2. - Select the watchdog event: Hardware or software. - Reset event when entering Stop mode. - Reset event when entering Standby mode. <p><i>Note: Only bits [19:16] are used, bits [23:20] are not used and set to 0xF.</i></p> <p>Bit 19: BFB2 Boot from Flash memory bank 1 or bank 2 This bit allows to select the active Flash bank to boot from: bank 1 or bank 2. 0: The device boots from Flash memory bank 1 or bank 2, depending on the activation of the bank. The active banks are checked in the following order: bank 2, followed by bank 1. The active bank is identified by the value programmed at the base address of the bank (corresponding to the initial stack pointer value in the interrupt vector table). Refer to application note AN2606 for further details. In this case, the boot pins can only select user Flash or RAM boot. 1: The device will boot from Flash memory bank 1 when boot pins are set in “boot from user Flash” position (default).</p> <p>Bit 18: nRST_STDBY 0: Reset generated when entering Standby mode. 1: No reset generated.</p> <p>Bit 17: nRST_STOP 0: Reset generated when entering Stop mode 1: No reset generated</p> <p>Bit 16: WDG_SW 0: Hardware watchdog 1: Software watchdog</p> <p>Bits [15:8]: nRDP</p> <p>Bits [7:0]: RDP: Read protection option byte The read protection helps the user protect the software code stored in Flash memory. It is activated by setting the RDP option byte. When this option byte is programmed to a correct value (RDPRT key = 0x00A5), read access to the Flash memory is allowed. (The result of RDP level enabled/disabled is stored in FLASH_OBR[1].)</p>

Table 5. Description of the option bytes (continued)

Flash memory address	Option bytes
0x1FFF F804	<p>Datax: Two bytes for user data storage. These addresses can be programmed using the option byte programming procedure.</p> <p>Bits [31:24]: nData1 Bits [23:16]: Data1 (stored in FLASH_OBR[25:18]) Bits [15:8]: nData0 Bits [7:0]: Data0 (stored in FLASH_OBR[17:10])</p>
0x1FFF F808	<p>WRPx: Flash memory write protection option bytes</p> <p>Bits [31:24]: nWRP1 Bits [23:16]: WRP1 (stored in FLASH_WRPR[15:8]) Bits [15:8]: nWRP0 Bits [7:0]: WRP0 (stored in FLASH_WRPR[7:0])</p>
0x1FFF F80C	<p>WRPx: Flash memory write protection option bytes</p> <p>Bits [31:24]: nWRP3 Bits [23:16]: WRP3 (stored in FLASH_WRPR[31:24]) Bits [15:8]: nWRP2 Bits [7:0]: WRP2 (stored in FLASH_WRPR[23:16])</p> <p>One bit of the user option bytes WRPx is used to protect 2 pages of 2 Kbytes in the main memory block. However, bit 7 of WRP3 write protects pages 62 to 511.</p> <p>0: Write protection active 1: Write protection not active</p> <p>In total, four user option bytes are used to protect 1 Mbytes of main Flash memory:</p> <p>WRP0 write-protects pages 0 to 15. WRP1 write-protects pages 16 to 31. WRP2 write-protects pages 32 to 47. WRP3: bits 0-6 write-protect pages 48 to 61, and bit 7 write-protects pages 62 to 511.</p>

On every system reset, the option byte loader (OBL) reads the information block and stores the data into the Option byte register (FLASH_OBR) and the Write protection register (FLASH_WRPR). Each option byte also has its complement in the information block. During option loading, by verifying the option bit and its complement, it is possible to check that the loading has correctly taken place. If this is not the case, an option byte error (OPTERR) is generated. When a comparison error occurs the corresponding option byte is forced to 0xFF. The comparator is disabled when the option byte and its complement are both equal to 0xFF (Electrical Erase state).

All option bytes (but not their complements) are available to configure the product. The option registers are accessible in read mode by the CPU. See [Section 3: Register descriptions](#) for more details.

3 Register descriptions

In this section, the following abbreviations are used:

Table 6. Abbreviations

Abbreviation	Meaning
read/write (rw)	Software can read from and write to these bits.
read-only (r)	Software can only read these bits.
write-only (w)	Software can only write to this bit. Reading the bit returns the reset value.
read/clear (rc_w0)	Software can read as well as clear this bit by writing '0'. Writing '1' has no effect on the bit value.
read/set (rs)	Software can read as well as set this bit. Writing '0' has no effect on the bit value.
Reserved (Res.)	Reserved bit, must be kept at reset value.

Note: The Flash memory registers have to be accessed by 32-bit words (half-word and byte accesses are not allowed).

3.1 Flash access control register (FLASH_ACR)

Address offset: 0x00

Reset value: 0x0000 0030

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										PRFT BS	PRFT BE	HLF CYA	LATENCY		
										r	rw	rw	rw	rw	rw

Bits 31:6 Reserved, must be kept cleared.

Bit 5 **PRFTBS**: Prefetch buffer status

This bit provides the status of the prefetch buffer.

0: Prefetch buffer is disabled

1: Prefetch buffer is enabled

Bit 4 **PRFTBE**: Prefetch buffer enable

0: Prefetch is disabled

1: Prefetch is enabled

Bit 3 **HLFCYA**: Flash half cycle access enable

0: Half cycle is disabled

1: Half cycle is enabled

Bits 2:0 **LATENCY**: Latency

These bits represent the ratio of the SYSCLK (system clock) period to the Flash access time.

000 Zero wait state, if $0 < \text{SYSCLK} \leq 24 \text{ MHz}$

001 One wait state, if $24 \text{ MHz} < \text{SYSCLK} \leq 48 \text{ MHz}$

010 Two wait states, if $48 \text{ MHz} < \text{SYSCLK} \leq 72 \text{ MHz}$

3.2 FPEC key register (FLASH_KEYR)

This register is dedicated to Flash memory bank 1.

Address offset: 0x04

Reset value: xxxx xxxx

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FKEYR[31:16]															
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FKEYR[15:0]															
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

Note: These bits are all write-only and will return a 0 when read.

Bits 31:0 **FKEYR**: FPEC key

These bits represent the keys to unlock the FPEC.

3.3 Flash OPTKEY register (FLASH_OPTKEYR)

Address offset: 0x08

Reset value: xxxxx xxxx

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OPTKEYR[31:16]															
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OPTKEYR[15:0]															
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

Note: These bits are all write-only and will return a 0 when read.

Bits 31:0 **OPTKEYR**: Option byte key

These bits represent the keys to unlock the OPTWRE.

3.4 Flash status register (FLASH_SR)

This register is dedicated to Flash memory bank 1.

Address offset: 0x0C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										EOP	WRPRT ERR	Res.	PGERR	Res.	BSY
										rw	rw		rw		r

Bits 31:6 Reserved, must be kept cleared.

Bit 5 **EOP**: End of operation

Set by hardware when a Flash operation (programming / erase) is completed. Reset by writing a 1

Note: EOP is asserted at the end of each successful program or erase operation

Bit 4 **WRPRTERR**: Write protection error

Set by hardware when programming a write-protected address of the Flash memory. Reset by writing 1.

Bit 3 Reserved, must be kept cleared.

Bit 2 **PGERR**: Programming error

Set by hardware when an address to be programmed contains a value different from '0xFFFF' before programming.

Reset by writing 1.

Note: The STRT bit in the FLASH_CR register should be reset before starting a programming operation.

Bit 1 Reserved, must be kept cleared

Bit 0 **BSY**: Busy

This indicates that a Flash operation is in progress. This is set on the beginning of a Flash operation and reset when the operation finishes or when an error occurs.

3.5 Flash control register (FLASH_CR)

This register is dedicated to Flash memory bank 1 and option bytes programming.

Address offset: 0x10

Reset value: 0x0000 0080

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			EOPIE	Res.	ERRIE	OPTWRE	Res.	LOCK	STRT	OPTER	OPTPG	Res.	MER	PER	PG
			rw		rw	rw		rw	rw	rw	rw		rw	rw	rw

Bits 31:13 Reserved, must be kept cleared.

Bit 12 **EOPIE**: End of operation interrupt enable

This bit enables the interrupt generation when the EOP bit in the FLASH_SR register goes to 1.

0: Interrupt generation disabled

1: Interrupt generation enabled

Bit 11 Reserved, must be kept cleared

Bit 10 **ERRIE**: Error interrupt enable

This bit enables the interrupt generation on an FPEC error (when PGERR / WRPRTErr are set in the FLASH_SR register).

0: Interrupt generation disabled

1: Interrupt generation enabled

Bit 9 **OPTWRE**: Option bytes write enable

When set, the option bytes can be programmed. This bit is set on writing the correct key sequence to the FLASH_OPTKEYR register.

This bit can be reset by software

Bit 8 Reserved, must be kept cleared.

Bit 7 **LOCK**: Lock

Write to 1 only. When it is set, it indicates that the FPEC and FLASH_CR are locked. This bit is reset by hardware after detecting the unlock sequence.

In the event of unsuccessful unlock operation, this bit remains set until the next reset.

Bit 6 **STRT**: Start

This bit triggers an ERASE operation when set. This bit is set only by software and reset when the BSY bit is reset.

Bit 5 **OPTER**: Option byte erase

Option byte erase chosen.

Bit 4 **OPTPG**: Option byte programming

Option byte programming chosen.

Bit 3 Reserved, must be kept cleared.

Bit 2 **MER**: Mass erase

Erase of all user pages chosen.

Bit 1 **PER**: Page erase

Page Erase chosen.

Bit 0 **PG**: Programming
Flash programming chosen.

3.6 Flash address register (FLASH_AR)

This register is dedicated to Flash memory bank 1.

Address offset: 0x14

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FAR[31:16]															
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FAR[15:0]															
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

Updated by hardware with the currently/last used address. For Page Erase operations, this should be updated by software to indicate the chosen page.

Bits 31:0 **FAR**: Flash Address

Chooses the address to program when programming is selected, or a page to erase when Page Erase is selected.

Note: Write access to this register is blocked when the BSY bit in the FLASH_SR register is set.

3.7 Option byte register (FLASH_OBR)

Address offset 0x1C

Reset value: 0x03FF FFFC

Note: The reset value of this register depends on the value programmed in the option byte and the OPTERR bit reset value depends on the comparison of the option byte and its complement during the option byte loading phase.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Reserved								Data1								Data0								Not used				BFB2	nRST_STDBY	nRST_STOP	WDG_SW	RDPRT	OPTERR
								r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Bits 31:25 Reserved, must be kept cleared.

Bits 25:18 Data1

Bits 17:10 Data0

Bits 9:2 **USER**: User option bytes

This contains the user option byte loaded by the OBL.

Bits [9:6]: Not used (if these bits are written in the Flash option byte, they will be read in this register with no effect on the device.)

Bit 5: BFB2

Bit 4: nRST_STDBY

Bit 3: nRST_STOP

Bit 2: WDG_SW

Bit 1 **RDPR**: Read protection

When set, this indicates that the Flash memory is read-protected.

Note: This bit is read-only.

Bit 0 **OPTERR**: Option byte error

When set, this indicates that the loaded option byte and its complement do not match. The corresponding byte and its complement are read as 0xFF in the FLASH_OBR or FLASH_WRPR register.

Note: This bit is read-only.

3.8 Write protection register (FLASH_WRPR)

Address offset: 0x20

Reset value: 0xFFFF FFFF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
WRP[31:16]															
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WRP[15:0]															
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Bits 31:0 **WRP**: Write protect

This register contains the write-protection option bytes loaded by the OBL.

0: Write protection active

1: Write protection not active

Note: These bits are read-only.

3.9 FPEC key register2 (FLASH_KEYR2)

This register is dedicated to Flash memory bank 2.

Address offset: 0x44

Reset value: xxxx xxxx

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FKEYR[31:16]															
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FKEYR[15:0]															
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

Note: These bits are all write-only and will return a 0 when read.

Bits 31:0 **FKEYR**: FPEC key for bank 2
 These bits represent the keys to unlock the FPEC.

3.10 Flash status register2 (FLASH_SR2)

This register is dedicated to Flash memory bank 2.

Address offset: 0x4C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										EOP	WRPRT ERR	Res.	PG ERR	Res.	BSY
										rw	rw	Res.	rw	Res.	r

Bits 31:6 Reserved, must be kept cleared.

Bit 5 **EOP**: End of operation

Set by hardware when a Flash operation (programming / erase) is completed. Reset by writing a 1

Note: EOP is asserted at the end of each successful program or erase operation

Bit 4 **WRPRTERR**: Write protection error

Set by hardware when programming a write-protected address of the Flash memory. Reset by writing 1.

Bit 3 Reserved, must be kept cleared.

Bit 2 **PGERR**: Programming error

Set by hardware when an address to be programmed contains a value different from '0xFFFF' before programming.

Reset by writing 1.

Note: The STRT bit in the FLASH_CR2 register should be reset before starting a programming operation.

Bit 1 Reserved, must be kept cleared

Bit 0 **BSY**: Busy

This indicates that a Flash operation is in progress. This is set on the beginning of a Flash operation and reset when the operation finishes or when an error occurs.

3.11 Flash control register2 (FLASH_CR2)

This register is dedicated to Flash memory bank 2.

Address offset: 0x50

Reset value: 0x0000 0080

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			EOPIE	Res.	ERRIE	Reserved		LOCK	STRT	Reserved			MER	PER	PG
			rw		rw			rw	rw				rw	rw	rw

Bits 31:13 Reserved, must be kept cleared.

Bit 12 **EOPIE**: End of operation interrupt enable

This bit enables the interrupt generation when the EOP bit in the FLASH_SR2 register goes to 1.

0: Interrupt generation disabled

1: Interrupt generation enabled

Bit 11 Reserved, must be kept cleared

Bit 10 **ERRIE**: Error interrupt enable

This bit enables the interrupt generation on an FPEC error (when PGERR / WRPRERR are set in the FLASH_SR2 register).

0: Interrupt generation disabled

1: Interrupt generation enabled

Bit 9 Reserved, must be kept cleared.

Bit 8 Reserved, must be kept cleared.

Bit 7 **LOCK**: Lock

Write to 1 only. When it is set, it indicates that the FPEC and FLASH_CR2 are locked. This bit is reset by hardware after detecting the unlock sequence.

In the event of unsuccessful unlock operation, this bit remains set until the next reset.

Bit 6 **STRT**: Start

This bit triggers an ERASE operation when set. This bit is set only by software and reset when the BSY bit is reset.

Bits 5:3 Reserved, must be kept cleared.

Bit 2 **MER**: Mass erase

Erase of all user pages selected.

Bit 1 **PER**: Page erase

Page Erase chosen.

Bit 0 **PG**: Programming

Flash programming selected.

3.12 Flash address register2 (FLASH_AR2)

This register is dedicated to Flash memory bank 2.

Address offset: 0x54

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FAR[31:16]															
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FAR[15:0]															
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

Updated by hardware with the currently/last used address. For Page Erase operations, this should be updated by software to indicate the chosen page.

Bits 31:0 **FAR**: Flash Address

Chooses the address to program when programming is selected, or a page to erase when Page Erase is selected.

Note: Write access to this register is blocked when the BSY bit in the FLASH_SR2 register is set.

3.13 Flash register map

Table 7. Flash interface - register map and reset values

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																										
0x000	FLASH_ACR Reset value	Reserved																								1	PRFTBS	1	PRFTBE	0	HLFCYA	0	LATENCY [2:0]	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
0x004	FLASH_KEYR Reset value	FKEYR[31:0]																								x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		
0x008	FLASH_OPTKEYR Reset Value	OPTKEYR[31:0]																								x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
0x00C	FLASH_SR Reset value	Reserved																								0	EOP	0	WRPRERR	0	Reserved	0	PGERR	0	ERLYBSY	0	BSY	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
0x010	FLASH_CR Reset value	Reserved																								0	EOPIE	0	Reserved	0	ERRIE	0	OPTWRE	0	Reserved	0	LOCK	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
0x014	FLASH_AR Reset value	FAR[31:0]																								0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x018		Reserved																																																									
0x01C	FLASH_OBR Reset value	Reserved				Data1				Data0				Not used				0	BFB2	1	nRST_STDBY	1	nRST_STOP	1	WDG_SW	0	RDPR	0	OPTERR	0	0	0	0	0	0																								
0x020	FLASH_WRPR Reset value	WRP[31:0]																								1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
0x044	FLASH_KEYR2 Reset value	FKEYR[31:0]																								x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
0x04C	FLASH_SR2 Reset value	Reserved																								0	EOP	0	WRPRERR	0	Reserved	0	PGERR	0	ERLYBSY	0	BSY	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
0x050	FLASH_CR2 Reset value	Reserved																								0	EOPIE	0	Reserved	0	ERRIE	0	Reserved	0	Reserved	0	LOCK	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x054	FLASH_AR2 Reset value	FAR[31:0]																								0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

4 Revision history

Table 8. Document revision history

Date	Revision	Changes
05-Mar-2010	1alpha	Alpha release.
19-Apr-2010	1	Added size of reserved areas in Table 1: XL-density Flash module organization . Updated list of registers in Section 2.3: Flash program and erase controller (FPEC) . Updated description of BFB2 in Table 5: Description of the option bytes .
13-Jan-2012	2	Updated warning bit designation in Section 2.3.5: Option byte programming .

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