VD5941, VD5943, VD1943, VB5943, and VB1943 user interface register descriptions

Introduction

This reference manual details the user interface registers for programming the VD5941, VD5943, and VB5943 monochrome sensors, as well as the VD1943 and VB1943 RGB-NIR sensors

Table 1. Order codes

Product	Variant	Order code
VD5941	Monochrome	VD5941CE/RWT
VD5943		VD5943CE/RW
VB5943		VB5943CAJX
VD1943	RGB-NIR	VD1943CE/RW
VB1943		VB1943CAJX

1 Address group summary

The user interface is exposed in different groups of registers.

The following table is providing the base address of these groups.

Table 2. Address group summary

Group base address	Group name	Description
0x0000	STATUS	Read only registers providing the sensor's state and configuration
0x0514	CMD	A set of commands triggering sensor's firmware actions
0x0734	SENSOR_SETTINGS	Configuration to perform prior to streaming images
0x090C	STREAM_STATICS	Configuration to perform prior to streaming images
0x0B40	STREAM_CTX0_STATIC	Context0 configuration to perform prior to streaming images
0x0B88	STREAM_CTX1_STATIC	Context1 configuration to perform prior to streaming images
0x0BD0	STREAM_CTX2_STATIC	Context2 configuration to perform prior to streaming images
0x0C18	STREAM_CTX3_STATIC	Context3 configuration to perform prior to streaming images
0x0C78	STREAM_CTX0_DYNAMIC	Context0 configuration can be live updated during streaming
0x0CA0	STREAM_CTX1_DYNAMIC	Context1 configuration can be live updated during streaming
0x0CC8	STREAM_CTX2_DYNAMIC	Context2 configuration can be live updated during streaming
0x0CF0	STREAM_CTX3_DYNAMIC	Context3 configuration can be live updated during streaming
0x0EC4	OTP_CTM_MIRROR	Location for permanent customer area information
0x1000	DEBUG	Miscellaneous

The four STREAM_CTX0/1/2/3_STATIC groups expose the same register fields for the four possible contexts. Only one table is provided to describe the fields of these groups.

The four STREAM_CTX0/1/2/3_DYNAMIC groups expose the same register fields for the four possible contexts. Only one table is provided to describe the fields of these groups.

The register address for register fields in groups STREAM_CTXn_STATIC or STREAM_CTXn_DYNAMIC is obtained by adding the group base address provided in Table 2. Address group summary to the address offset provided in the tables of groups STREAM_CTXn_STATIC or STREAM_CTXn_DYNAMIC.

Register fields have different sizes from one byte up to 4 bytes.

Register fields greater than one byte are written LSB (least significant bit) first.

Register fields from group STATUS are read-only registers.

Register fields from other group are read/write registers.

Register fields from SENSOR_SETTINGS, STREAM_STATIC, or STREAM_CTXn_STATIC groups cannot be written when the sensor is streaming.

The reset value column in the following tables represents the values when the sensor is in SW_STBY state after executing a BOOT command.

2 Description of registers from STATUS group

Table 3. Description of registers from STATUS group

Register name	Absolute address	Register size	Reset value	Bits	Field name	Description
DEVICE_MODEL_ID	0x0000	4	0x53393431	31:0	VALUE	Device model ID in ASCII ("S941")
DEVICE_REVISION	0x0004	4	0x0A040A0A	31:24	DEVICE_REVISION	Device revision
UI_REVISION	0x0008	2	0x04	15:8	MAJOR_REVISION	Major user interface revision
			0x0C	7:0	MINOR_REVISION	Minor user interface revision
DEVICE_VARIANT	0x000A	2	0x03	15:0	VALUE	Device variant ID
ROM_REVISION	0x000C	2	0x540	15	ROM_REVISION	Firmware ROM revision
CFA_SELECTION	0x000E	2	0x0	3:0	VALUE	Color filter: 0x0: (RGB-NIR) 0x1: (MONOCHROME)
DEVICE_NUMBER_1	0x0010	4	0x0	31:0	VALUE	Device number from traceability
DEVICE_NUMBER_2	0x0014	4	0x0	31:0	VALUE	Device number from traceability
DEVICE_NUMBER_3	0x0018	4	—	31:0	VALUE	Device number from traceability
DEVICE_NUMBER_4	0x001C	4	—	31:0	VALUE	Device number from traceability
DEVICE_NUMBER_5	0x0020	4	—	31:0	VALUE	Device number from traceability
SYSTEM_FSM_STATE	0x0044	1	0x3	7:0	VALUE	Sensor system FSM status: 0x0: (HW_STBY) 0x1: (SYSTEM_UP) 0x2: (BOOT) 0x3: (SW_STBY) 0x4: (STREAMING) 0x6: (HALT)
MIPI_LANE_NB	0x0045	1	0x0	7:0	VALUE	MIPI LANE NB: 0x0: (LANES_NB_4) 0x1: (LANES_NB_2) 0x2: (LANES_NB_1)
SYSTEM_WARNING	0x0046	2	0x0	15:0	VALUE	Firmware module in which error occurred
SYSTEM_ERROR	0x0048	2	0x0	15:0	VALUE	Firmware module in which warning occurred
FWPATCH_REVISION	0x004A	2	0x0	15:8	MAJOR_REVISION	Major firmware patch revision
			0x0	7:0	MINOR_REVISION	Minor firmware patch revision
VTIMING_PATCH	0x004E	1	0x0	7:0	VTRAM_UPDATED	Status of VT RAM patch update: 0x0: Not updated 0x01: Updated
TEMPERATURE_1	0x006A	2	0x0	15:0	TH_DEGREE_INT	Temperature sensor 1 in celsius
TEMPERATURE_2	0x006C	2	0x0	15:0	TH_DEGREE_INT	Temperature sensor 2 in celsius
FRAME_COUNTER	0x006E	2	0x0	15:0	VALUE	Current frame count
CURRENT_CONTEXT	0x0072	1	0x0	7:0	VALUE	Current frame context
NEXT_CONTEXT	0x0073	1	0x0	7:0	VALUE	Next context in the CONTEXT_SEQUENCING vector
LOOP_ELEMENT	0x0074	1	0x0	5:0	VALUE	Element position in the sequence before repeating the sequence (0..31)
CURRENT_ELEMENT	0x0075	1	0x0	5:0	VALUE	Index of the current element in the sequence of contexts (0..31)
I2C_ADDRESS	0x0076	1	0x10	6:0	DEVICE_ID	Device I^2C address without R/W bit
ORIENTATION	0x0077	1	0x0	1:0	MODE	Image orientation mode control: 0x0: (NORMAL) No flip 0x1: (X_FLIP) X flip 0x2: (Y_FLIP) Y flip 0x3: (XY_FLIP) XY flip

Register name	Absolute address	Register size	Reset value	Bits	Field name	Description
VT_CTRL	0x0078	1	0x0	1:0	SYNC_MODE	Video timing synchronous mode: 0x0: (LEADER_MODE) 0x1: (FOLLOWER_MODE) frame triggered by FSYNC_IN pulses
OUTPUT_FORMAT	0x0079	1	0x0	4:0	VALUE	Frame output format control: 0x8: (RAW8) 0xA: (RAW10) 0xC: (RAW12)
VIRTUAL_CHANNEL	0x007A	1	0x0	7:0	VALUE	Current frame virtual channel ID By default, all contexts are on VC 0
ROI_SELECTION	0x007B	1	0x0	3	ROI_D_ENABLE	ROI D: 0x0: (NOT_ACTIVE) 0x1: (ACTIVE)
			0x0	2	ROI_C_ENABLE	ROI C: 0x0: (NOT_ACTIVE) 0x1: (ACTIVE)
			0x0	1	ROI_B_ENABLE	ROI B: 0x0: (NOT_ACTIVE) 0x1: (ACTIVE)
			0x0	0	ROI_A_ENABLE	ROI A: 0x0: (NOT_ACTIVE) 0x1: (ACTIVE)
ROI_A_OFFSET	0x007C	4	0x0	31:16	WIDTH	ROI A image: Width offset, relative to output size
			0x0	15:0	HEIGHT	ROI A image: Height offset, relative to output size
ROI_A_SIZE	0x0080	4	0x0	31:16	WIDTH	ROI A image: Width, relative to output size
			0x0	15:0	HEIGHT	ROI A image: Height, relative to output size
ROI_B_OFFSET	0x0084	4	0x0	31:16	WIDTH	ROI B image: Width offset, relative to output size
			0x0	15:0	HEIGHT	ROI B image: Height offset, relative to output size
ROI_B_SIZE	0x0088	4	0x0	31:16	WIDTH	ROI B image: Width, relative to output size
			0x0	15:0	HEIGHT	ROI B image: Height, relative to output size
ROI_C_OFFSET	0x008C	4	0x0	31:16	WIDTH	ROI C image: Width offset, relative to output size
			0x0	15:0	HEIGHT	ROI C image: Height offset, relative to output size
ROI_C_SIZE	0x0090	4	0x0	31:16	WIDTH	ROI C image Width, relative to output size
			0x0	15:0	HEIGHT	ROI C image: Height, relative to output size
ROI_D_OFFSET	0x0094	4	0x0	31:16	WIDTH	ROI D image: Width offset, relative to output size
			0x0	15:0	HEIGHT	ROI D image: Height offset, relative to output size
ROI_D_SIZE	0x0098	4	0x0	31:16	WIDTH	ROI D image: Width, relative to output size
			0x0	15:0	HEIGHT	ROI D image: Height, relative to output size

Register name	Absolute address	Register size	Reset value	Bits	Field name	Description
ROI_A_DT	0x009C	1	0x0	7:0	VALUE	ROI A: Data type
ROI_B_DT	0x009D	1	0x0	7:0	VALUE	ROI B: Data type
ROI_C_DT	0x009E	1	0x0	7:0	VALUE	ROI C: Data type
ROI_D_DT	0x009F	1	0x0	7:0	VALUE	ROI D: Data type
PATGEN_CTRL	0x00A0	2	0x0	15:8	TYPE	Pattern generator content: 0x22: (DGREY) Diagonal gray scale 0x28: (PN28) Pseudorandom
			0x0	1:0	ENABLE	Pattern generator configuration: 0x00: (PATGEN_BYPASS) 0x01: (PATGEN_NORMAL)
VT_ANALOG_GAIN	0x00A2	2	0x0	4:0	VALUE	Coded analog gain: Coded gain = 16/(16-VT_ANALOG_GAIN)
INTEGRATION_TIME_PRIMARY	0x00A4	2	0x0	15:0	VALUE	Integration time in line equivalent. Long exposure in rolling shutter mode. Exposure of all pixels in global shutter single exposure mode. Exposure of RGB (or P1P2P3) pixels in global shutter split exposure mode.
RGB-NIR: INTEGRATION_TIME_IR MONOCHROME: INTEGRATION_TIME_P4	0x00A6	2	0x0	15:0	VALUE	Integration time for the NIR pixel (or P4) in line equivalent. Only available for configurations using split exposure.
INTEGRATION_TIME_SHORT	0x00A8	2	0x0	15:0	VALUE	Integration time in line equivalent. Only available for short exposure in rolling shutter HDR mode.
RGB-NIR: DIGITAL_GAIN_R MONOCHROME: DIGITAL_GAIN_P1	0x00AA	2	0x0	12:8	INTEGER	Digital gain (integer part) for R channel or P1 for monochrome version
			0x0	7:0	FRACT	Digital gain (fractional part) for R channel or P1 for monochrome version
RGB-NIR: DIGITAL_GAIN_G MONOCHROME: DIGITAL_GAIN_P4	0x00AC	2	0x0	12:8	INTEGER	Digital gain (integer part) for G channel or P4 for monochrome split pixel
			0x0	7:0	FRACT	Digital gain (fractional part) for G channel or P4 for monochrome split pixel
RGB-NIR: DIGITAL_GAIN_B MONOCHROME: DIGITAL_GAIN_P2	0x00AE	2	0x0	12:8	INTEGER	Digital gain (integer part) for B channel or P2 for monochrome version
			0x0	7:0	FRACT	Digital gain (fractional part) for B channel or P2 for monochrome version
RGB-NIR: DIGITAL_GAIN_IR MONOCHROME: DIGITAL_GAIN_P3	0x00B0	2	0x0	12:8	INTEGER	Digital gain (integer part) for IR channel or P3 for monochrome version
			0x0	7:0	FRACT	Digital gain (fractional part) for IR channel or P3 for monochrome version
LINE_LENGTH	0x00B2	2	0x0	15:0	VALUE	Line length duration (number of quarters of pixel clock period)
FRAME_LENGTH	0x00B4	4	0x0	31:0	VALUE	Frame length duration in number of lines
READOUT_CTRL	0x00B8	1	0x0	2:0	CFG	Streaming readout mode control: 0x00: (NORMAL) Normal streaming 0x01: (SS_X2) Subsampling x2 0x02: (SS_X4) Subsampling x4 0x03: (SS_X32) Subsampling x32
GPIO_STATUS	0x00B9	1	0x0	3	GPIO_3	Value read on GPIO_3 when configured as input
			0x0	2	GPIO_2	Value read on GPIO_2 when configured as input

Register name	Absolute address	Register size	Reset value	Bits	Field name	Description
GPIO_STATUS	0x00B9	1	0x0	1	GPIO_1	Value read on GPIO_1 when configured as input
			0x0	0	GPIO_0	Value read on GPIO_0 when configured as input
PWL	0x00BA	1	0x0	1	LUT_SEL	PWL status: 0x0: (DEFAULT) 0x1: (CUSTOM)
			0x0	0	ENABLE	0x0: (DISABLE) 0x1: (ENABLE)
IMAGE_CONFIG	0x00BC	1	0x0	7:0	VALUE	Image/sensor configuration being streamed out. Refer to Section 6: Description of registers from STREAM_CTX0_STATIC group.
SHUTTER_MODE	0x00BD	1	0x0	7:0	VALUE	0:(GLOBAL_SHUTTER) 1:(ROLLING_SHUTTER)
HDR	0x00BE	1	0x0	7:0	VALUE	Status of rolling shutter HDR 0x0: (DISABLE) 0x1:(ENABLE)
CFABLEND_ALPHA_R	0x00C0	2	0x0	15:0	VALUE	RGB-NIR version only: FP 8.8 Alpha for CFA blender red pixel
CFABLEND_ALPHA_B	0x00C2	2	0x0	15:0	VALUE	RGB-NIR version only: FP 8.8 Alpha for CFA blender blue pixel
CFABLEND_ALPHA_GIB	0x00C4	2	0x0	15:0	VALUE	RGB-NIR version only: FP 8.8 Alpha for CFA blender green in blue pixel
PLL_STATUS	0x00C6	1	0x0	1	MIPI_PLL_LOCK	PLL lock status: 0x0:(UNLOCK) 0x1: (LOCK)
			0x0	0	SYS_PLL_LOCK	PLL lock status: 0x0:(UNLOCK) 0x1: (LOCK)
PEDESTAL	0x00D6	2	0x0	11:0	VALUE	DARKCAL pedestal value
OIF_LANE_PHY_MAP	0x016C	1	0x0	7:6	LANE4	Lane mapping for physical lane 4
			0x0	5:4	LANE3	Lane mapping for physical lane 3
			0x0	3:2	LANE2	Lane mapping for physical lane 2
			0x0	1:0	LANE1	Lane mapping for physical lane 1
NVM	0x0204	4	0x1	31	UNPACK	NVM data unpack: 0x0: (NOT_DONE) 0x1: (DONE)
			0x1	30	DOWNLOAD	NVM download: 0x0: (NOT_DONE) 0x1: (DONE)
			0x0	24	ECC_CORRECTION	ECC correction status: 0x0: (NO_CORRECTION) 0x1: (ECC_CORRECTION_DETECTED)
			0x0	23:16	NB_ECC	Number of ECC errors detected
			0x0	15:8	ERROR_ADDRESS	NVM address on ERROR
			0x0	7:4	ERROR	NVM ERROR STATUS: 0x0: (NO_ERROR) 0x1: (BAD_CONFIG) 0x2: (READ_FAIL) 0x3: (PROG_FAIL) 0x4: (ECC_CORRECTION_FAIL)

Register name	Absolute address	Register size	Reset value	Bits	Field name	Description
NVM	0x0204	4				0x5: (PROG_ON_NON_VIRGIN_WORD) 0xA: (VIRGINITY_ERROR) 0xE: (LOCK_ERROR)
			0x5	3:0	OPERATION	NVM OPERATION STATUS: 0x0: (NOT_USED) 0x5: (OPERATION_SUCCESS) 0xF: (OPERATION_FAIL)
SYSTEM_PLL_CLK	0x0228	4	0x59682F00 for CLK_RANGE_0/1=00	31:0	VALUE	PLL output frequency in Hz
PIXEL_CLK	0x022C	4	0xBEBC20 for CLK_RANGE_0/1=00	31:0	VALUE	Pixel clock frequency in Hz
MCU_CLK	0x0230	4	0x17D7840 for CLK_RANGE_0/1=00	31:0	VALUE	MCU clock frequency in Hz
CLK_SYS_PLL_MULT	0x0234	1	0x3C	7:0	VALUE	System PLL multiplier value
CLK_MIPI_PLL_MULT	0x0235	1	0x0	7:0	VALUE	MIPI PLL multiplier value
FRAME_RATE	0x0236	2	0x0	15:0	VALUE	Frame rate in frames per-second rolls over after 255
HUBBLEEYES_DMP_KNEE1	0x02C0	4	0x0	31:0	VALUE	Value of the first HDR knee point in percentage multiplied by 256
HUBBLEEYES_DMP_KNEE2	0x02C4	4	0x0	31:0	VALUE	Value of the second HDR knee point in percentage multiplied by 256
EXPO_STAT_SELECTION	0x02C9	1	0x0	0	SELECT	Statistics computation: 0x0: (BEFORE_CFA) 0x1: (AFTER_CFA) - RGB-NIR version only
STAT_ROI_WIDTH_OFFSET	0x02CA	2	0x0	15:0	VALUE	Statistics image area: The reference is the output image.
STAT_ROI_HEIGHT_OFFSET	0x02CC	2	0x0	15:0	VALUE	Statistics image area: The reference is the output image.
STAT_ROI_WIDTH	0x02CE	2	0x0	15:0	VALUE	Statistics image area: The reference is the output image.
STAT_ROI_HEIGHT	0x02D0	2	0x0	15:0	VALUE	Statistics image area: The reference is the output image.
CHANNEL_STAT_CFG	0x02D2	1	0x0	7:0	CONFIG	Pixel type selection for statistics
HISTO_CFG	0x02D3	1	0x0	7:0	CONFIG	Pixel type selection for histograms

3 Description of registers from CMD group

Table 4. Description of registers from CMD group

Register name	Absolute address	Register size	Reset value	Bits	Field name	Description
SYSTEM_UP	0x0514	1	0x0	1:0	COMMAND	0x0:(CMD_ACK) 0x1:(START_SENSOR)
BOOT	0x0515	1	0x0	4:0	COMMAND	0x0:(CMD_ACK) 0x2:(LOAD_FWP) 0x10:(END_BOOT)
SW_STBY	0x0516	1	0x0	5:0	COMMAND	0x0:(CMD_ACK) 0x1:(START_STREAMING) 0x2:(THSENS_READ) 0x3: (UPDATE_VT_RAM_START) 0x4: (UPDATE_VT_RAM_END) 0x15:(NVM_READ) 0x16:(NVM_PROG) 0x18:(I2C_COMMS_UPDATE)
STREAMING	0x0517	1	0x0	3:0	COMMAND	0x0:(CMD_ACK) 0x1:(STOP_STREAM)

4 Description of registers from SENSOR_SETTINGS group

Table 5. Description of registers from SENSOR_SETTINGS group

Register name	Absolute address	Register size	Reset value	Bits	Field name	Description
EXT_CLOCK	0x0734	4	0x17D7840 (25M) for CLK_RANGE0/1=00	31:0	VALUE	External clock frequency in Hz
MIPI_DATA_RATE	0x0738	4	0x4D7C6D00	31:0	VALUE	PLL MIPI clock frequency in Hz
NVM_CTRL	0x073C	1	0x0	1	OFFSET	OTP address offset selection: 0x1: (CTM_AREA)
			0x0	0	ECC_CTRL	NVM ECC control: 0x0: (NVM_ECC_ON)
NVM_START_ADDRESS	0x073D	1	0x0	7:0	VALUE	Start address in NVM for read/ write burst operation
NVM_NB_OF_WORDS	0x073E	2	0x0	8:0	VALUE	Number of 32-bit words to read/write in burst mode
DEVICE_COMMS_CTRL	0x0740	2	0x6	10:8	DRIVE	I^2C pads drive configuration: 0x6: (20 mA) 0x0: (4 mA)
			0x20	7:0	DEVICE_ID	Device I^2C address including R/W bit
LANE_NB_SEL	0x0743	1	0x1	7:0	VALUE	0: (LANES_NB_4) 1: (LANES_NB_2) 2: (LANES_NB_1)

5 Description of registers from STREAM_STATIC group

Table 6. Description of registers from STREAM_STATIC group

Register name	Absolute address	Register size	Reset value	Bits	Field name	Description
ROI_A_WIDTH_OFFSET	0x090C	2	0x0	15:0	VALUE	ROI A image width offset, relative to the output size
ROI_A_HEIGHT_OFFSET	0x090E	2	0x0	15:0	VALUE	ROI A image height offset, relative to the output size
ROI_A_WIDTH	0x0910	2	0xA00	15:0	VALUE	ROI A image width, relative to the output size
ROI_A_HEIGHT	0x0912	2	0x7C0	15:0	VALUE	ROI A image height, relative to the output size
ROI_A_DT	0x0914	1	0x2C	7:0	VALUE	If 0, ROI A uses the DT from the SENSOR_CONFIGURATION value. If not 0, the ROI A DT is set to the specified value.
NB_FRAMES_TO_SEND	0x0915	1	0x0	7:0	VALUE	0: Continuous streaming Not 0: Streams the configured number of frames before stopping and going to SW_STBY state
ROI_B_WIDTH_OFFSET	0x0916	2	0x0	15:0	VALUE	ROI B image width offset, relative to the output size
ROI_B_HEIGHT_OFFSET	0x0918	2	0x0	15:0	VALUE	ROI B image height offset, relative to the output size
ROI_B_WIDTH	0x091A	2	0xA00	15:0	VALUE	ROI B image width, relative to the output size
ROI_B_HEIGHT	0x091C	2	0x7C0	15:0	VALUE	ROI B image height, relative to the output size
ROI_B_DT	0x091E	1	0x2C	7:0	VALUE	If 0, ROI B uses the DT from the SENSOR_CONFIGURATION value. If not 0, the ROI B DT is set to the specified value.
ROI_C_WIDTH_OFFSET	0x0920	2	0x0	15:0	VALUE	ROI C image width offset, relative to the output size
ROI_C_HEIGHT_OFFSET	0x0922	2	0x0	15:0	VALUE	ROI C image height offset, relative to the output size
ROI_C_WIDTH	0x0924	2	0xA00	15:0	VALUE	ROI C image width, relative to the output size
ROI_C_HEIGHT	0x0926	2	0x7C0	15:0	VALUE	ROIC image height, relative to the output size
ROI_C_DT	0x0928	1	0x2C	7:0	VALUE	If 0, ROI C uses the DT from the SENSOR_CONFIGURATION value. If not 0, the ROI C DT is set to the specified value.
ROI_D_WIDTH_OFFSET	0x092A	2	0x0	15:0	VALUE	ROI D image width offset, relative to the output size
ROI_D_HEIGHT_OFFSET	0x092C	2	0x0	15:0	VALUE	ROI D image height offset, relative to the output size
ROI_D_WIDTH	0x092E	2	0xA00	15:0	VALUE	ROI D image width, relative to the output size
ROI_D_HEIGHT	0x0930	2	0x7C0	15:0	VALUE	ROI D image height, relative to the output size
ROI_D_DT	0x0932	1	0x2C	7:0	VALUE	If 0, ROI D uses the DT from the SENSOR_CONFIGURATION value. If not 0, the ROI D DT is set to the specified value.
LINE_LENGTH	0x0934	2	0x1EA8	15:0	VALUE	Line length duration measured in quarters of the pixel clock period
ORIENTATION	0x0937	1	0x2	7:0	MODE	Image orientation mode control: 0x0: (NORMAL) No flip 0x1: (X_FLIP) X flip 0x2: (Y_FLIP) Y flip 0x3: (XY_FLIP) XY flip

Register name	Absolute address	Register size	Reset value	Bits	Field name	Description
PATGEN_CTRL	0x0938	2	0x22	15:8	TYPE	Pattern generator content: 0x22: (DGREY) Diagonal grayscale 0x28: (PN28) Pseudorandom
			0x0	1:0	ENABLE	Pattern generator configuration: 0x00: (PATGEN_BYPASS) 0x01: (PATGEN_NORMAL)
OIF_LANE_PHY_MAP	0x093A	1	0x3	7:6	LANE4	Lane mapping for physical lane 4
			0x0	5:4	LANE3	Lane mapping for physical lane 3
			0x1	3:2	LANE2	Lane mapping for physical lane 2
			0x2	1:0	LANE1	Lane mapping for physical lane 1
OIF_LANE_PHY_SWAP	0x093B	1	0x1	4	CLK	CSI CLOCK lane swap: 0: (NO_SWAP) 1: (LANE_SWAP)
			0x0	3	DATALANE4	CSI lane 4 swap: 0: (NO_SWAP) 1: (LANE_SWAP)
			0x0	2	DATALANE3	CSI lane 3 swap: 0: (NO_SWAP) 1: (LANE_SWAP)
			0x0	1	DATALANE2	CSI lane 2 swap: 0: (NO_SWAP) 1: (LANE_SWAP)
			0x0	0	DATALANE1	CSI lane 1 swap: 0: (NO_SWAP) 1: (LANE_SWAP)
OIF_INTERPACKET_DELAY	0x093C	2	0x1E	15:0	VALUE	Minimum delay between two consecutive CSI-2 packets (minimum value is 30)
PWL_ABSCISSA_n	0x0940 + n*0x4 (where n = 0 to 31)	128	0x0	31:0	VALUE	Abscissa of a custom LUT used for HDR imaging with a rolling shutter into 32 distinct segments.
PWL_ORDINATE_n	0x09C0 + n*0x4 (where n = 0 to 31)	128	0x0	31:0	VALUE	Ordinate of a custom LUT used for HDR imaging with a rolling shutter into 32 distinct segments.
PWL_GRADIENT_n	0x0A40 + n*0x4 (where n = 0 to 31)	128	0x0	31:0	VALUE	Gradient of a custom LUT used for HDR imaging with a rolling shutter into 32 distinct segments.
PWL_EXPO_BIAS	0x0AC0	4	0xA	31:0	VALUE	Exposure bias of a custom LUT used for rolling shutter HDR imaging
FSYNC_IN_DELAY	0x0AC4	2	0x0	15:0	VALUE	Tunable delay in follower mode measured in lines
VT_CTRL	0x0AC6	1	0x0	1:0	SYNC_MODE	Video timing synchronous mode: 0x0: (LEADER_MODE) 0x1: (FOLLOWER_MODE) Frame triggered by FSYNC_IN pulses
OIF_ISL_ENABLE	0x0AC7	1	0x1	1	VALUE	Output of top ISL 0x0:(Disable) 0x1:(Enable)
OIF_STATUS_LINE_CFG	0x0AC8	1	0x0	1	VALUE	0x0: (STATUS_LINE_SIZE_IMG_ACTIVE) Align status line payload size to image line payload size 0x1: (STATUS_LINE_SIZE_ACTUAL)
VSYNC_START_DELAY	0x0AC9	1	0x0	7:0	DELAY_L	Signed value of delay to apply (in number of lines)
VSYNC_END_DELAY	0x0ACA	1	0x0	7:0	DELAY_L	Signed value of delay to apply in number of lines
STROBE_START_DELAY	0x0ACB	1	0x0	7:0	DELAY_L	Signed value of delay to apply in number of lines

Register name	Absolute address	Register size	Reset value	Bits	Field name	Description
STROBE_END_DELAY	0x0ACC	1	0x0	7:0	DELAY_L	Signed value of delay to apply in number of lines
PWM_CTRL	0x0AD0	4	0x64	31:16	CLKDIVISOR	MCU_CLK division factor to achieve PWM frequency
			0x7	3:0	DUTYCYCLE	Low-level duty cycle using the formula (16-VALUE)/16
GPIO_0_CTRL	0x0AD4	1	0x0	5	POLARITY	Polarity value: 0x00: (NO_INVERSION) 0x01: (INVERTED)
			0x0	4	VALUE	GPIO_VALUE: 0x00: (GPIO_LOW) 0x01: (GPIO_HIGH)
			0x0	3:0	MODE	GPIO mode: 0x0: (STROBE) 0x1: (PWM_STROBE) 0x2: (PWM) 0x3: (GP_IN) 0x4: (GP_OUT) 0x5: (FSYNC_IN) 0x7: (FSYNC_OUT) 0xB: (VSYNC_GS) 0xC: (VSYNC_RS)
GPIO_1_CTRL	0x0AD5	1	0x0	5	POLARITY	Polarity value: 0x00: (NO_INVERSION) 0x01: (INVERTED)
			0x0	4	VALUE	GPIO_VALUE: 0x00: (GPIO_LOW) 0x01: (GPIO_HIGH)
			0x3	3:0	MODE	GPIO mode: 0x0: (STROBE) 0x1: (PWM_STROBE) 0x2: (PWM) 0x3: (GP_IN) 0x4: (GP_OUT) 0x5: (FSYNC_IN) 0xB: (VSYNC_GS) 0xC: (VSYNC_RS)
GPIO_2_CTRL	0x0AD6	1	0x0	5	POLARITY	Polarity value: 0x00: (NO_INVERSION) 0x01: (INVERTED)
			0x0	4	VALUE	GPIO_VALUE: 0x00: (GPIO_LOW) 0x01: (GPIO_HIGH)
			0x3	3:0	MODE	GPIO mode: 0x0: (STROBE) 0x1: (PWM_STROBE) 0x2: (PWM) 0x3: (GP_IN) 0x4: (GP_OUT) 0x5: (FSYNC_IN) 0xB: (VSYNC_GS) 0xC: (VSYNC_RS)
GPIO_3_CTRL	0x0AD7	1	0x0	5	POLARITY	Polarity value: 0x00: (NO_INVERSION) 0x01: (INVERTED)
			0x0	4	VALUE	GPIO_VALUE:

Register name	Absolute address	Register size	Reset value	Bits	Field name	Description
GPIO_3_CTRL	0x0AD7	1				0x00: (GPIO_LOW) 0x01: (GPIO_HIGH)
			0x3	3:0	MODE	GPIO mode: 0x0: (STROBE) 0x1: (PWM_STROBE) 0x2: (PWM) 0x3: (GP_IN) 0x4: (GP_OUT) 0x5: (FSYNC_IN) 0xB: (VSYNC_GS) 0xC: (VSYNC_RS)
CONTEXT_SWITCH_SEQUENCE_VECTOR_n	0x0ADC+ 4xn (where n = 0 to 1)	8	0x0	31:0	VALUE	Vector containing the sequence of context IDs to link together. The list can have a maximum of 32 items.
CONTEXT_SWITCH_LOOP_ELEMENT	0x0AE4	1	0x0	7:0	VALUE	Position of an element in a sequence before the sequence starts over again. The position can be any number from 0 to 31.
HDR_GHOST_FLICKER_CTRL	0x0AEC	1	0x1	7:0	VALUE	0x0: (DISABLE) 0x1: (GHOST_REMOVAL)
CFA_BLENDER_ALPHA_CTRL	0x0AED	1	0x0	7:0	VALUE	RGB-NIR version only 0x0:(NORMAL) Normal alpha is applied and the damper is disabled. 0x1:(DAMPER) Faded alpha is applied and the damper is enabled. 0x2:(ZERO) All alpha are set to zero (suitable for pure RGB applications).
EXPO_STAT_CTRL	0x0AEE	1	0x1	7:0	VALUE	Control of the exposure statistics 0x0: (DISABLE) 0x1: (CHANNEL_STATS_ONLY) 0x2: (CHANNEL_STATS_2_HISTOGRAM) 0x3: (CHANNEL_STATS_3_HISTOGRAM)
HDEFCOR_ENABLE	0x0AF2	1	0x01	7:0	VALUE	Dark lines defect correction 0x00: (DISABLE) 0x01: (ENABLE)
DARKCAL_ENABLE	0x0AF3	1	0x01	7:0	VALUE	Dark calibration 0x00: (DISABLE) 0x01: (ENABLE)
OIF_DT_STAT	0x0AF4	1	0x2C	7:0	VALUE	Data type of the bottom status lines including histograms and statistics
CFABLEND_ALPHA_R	0x0AF6	2	0x0100	15:0	VALUE	RGB-NIR version only: FP 8.8 alpha value for a red pixel in the CFA blender must be adjusted according to the lens characteristics
CFABLEND_ALPHA_B	0x0AF8	2	0x0100	15:0	VALUE	RGB-NIR version only: FP 8.8 alpha value for a blue pixel in the CFA blender must be adjusted according to the lens characteristics
CFABLEND_ALPHA_GIB	0x0AFA	2	0x0100	15:0	VALUE	RGB-NIR version only: FP 8.8 alpha value for a green pixel in the CFA blender must be adjusted according to the lens characteristics
OIF_DT_ISL	0x0AFC	1	0x2C	7:0	VALUE	Data type of the top status line (ISL)

6 Description of registers from STREAM_CTX0_STATIC group

There are four different STATIC groups to configure the STATIC parameters of the four available contexts.

Table 7. Static groups

Group base address	Group name	Description
0x0B40	STREAM_CTX0_STATIC	Context0 configuration to perform prior to streaming images
0x0B88	STREAM_CTX1_STATIC	Context1 configuration to perform prior to streaming images
0x0BD0	STREAM_CTX2_STATIC	Context2 configuration to perform prior to streaming images
0x0C18	STREAM_CTX3_STATIC	Context3 configuration to perform prior to streaming images

The table below provides the registers relative address. It must be added to the group base address of the targeted context to get the absolute address.

Table 8. Description of registers from STREAM_CTX0_STATIC group

Register name	Relative address	Register size	Reset value	Bits	Field name	Description
SENSOR_CONFIGURATION for RGB-NIR versions	0x0000	4	0x13 for CTX0/2 0x23 for CTX1/3	31:0	VALUE	0x1: CONFIG 1, global shutter, single exposure, RGB-NIR, RAW8 0x2: CONFIG 2, global shutter, single exposure, RGB-NIR, RAW10 0x3: CONFIG 3, global shutter, split exposure, RGB-NIR, RAW8 0x4: CONFIG 4, global shutter, split exposure, RGB-NIR, RAW10 0x5: CONFIG 5, global shutter, single exposure, RGB, RAW8 0x6: CONFIG 6, global shutter, single exposure, RGB, RAW10 0x9: CONFIG 9, global shutter, single exposure, IR, subsampling x2, RAW8 0xa: CONFIG 10, global shutter, single exposure, IR, subsampling x2, RAW10 0xb: CONFIG 11, global shutter, single exposure, IR, subsampling x4, RAW8 0xc: CONFIG 12, global shutter, single exposure, IR, subsampling x4, RAW10 0xd: CONFIG 13, global shutter, single exposure, IR, subsampling x32, RAW8 0xe: CONFIG 14, global shutter, single exposure, IR, subsampling x32, RAW10 0xf: CONFIG 15, global shutter, single exposure, IR, smart upscale, RAW8 0x10: CONFIG 16, global shutter, single exposure, IR, smart upscale, RAW10 0x11: CONFIG 17, global shutter, split exposure, IR, smart upscale, RAW8 0x12: CONFIG 18, global shutter, split exposure, IR, smart upscale, RAW10 0x1A: CONFIG 26, rolling shutter, SDR, RGB-NIR, RAW8 0x1B: CONFIG 27, rolling shutter, SDR, RGB-NIR, RAW10 0x1C: CONFIG 28, rolling shutter, SDR, RGB-NIR, RAW12 0x1D: CONFIG 29, rolling shutter, SDR, RGB-NIR, RAW8 0x1E: CONFIG 30, rolling shutter, SDR, RGB, RAW10 0x1F: CONFIG 31, rolling shutter, SDR, RGB, RAW12 0x20: CONFIG 32, rolling shutter, HDR, RGB-NIR, RAW10 0x21: CONFIG 33, rolling shutter, HDR, RGB-NIR, RAW12 0x22: CONFIG 34, rolling shutter, HDR, RGB, RAW10 0x23: CONFIG 35, rolling shutter, HDR, RGB, RAW12

Table 9. Description of registers from STREAM_CTX0_STATIC group

Register name	Relative address	Register size	Reset value	Bits	Field name	Description
SENSOR_CONFIGURATION for monochrome versions	0x0000	4	0x13 for CTX0/2 0x23 for CTX1/3	31:0	VALUE	0x1: CONFIG 1, global shutter, single exposure, mono, RAW8 0x2: CONFIG 2, global shutter, single exposure, mono, RAW10 0x3: CONFIG 3, global shutter, split exposure, mono, RAW8 0x4: CONFIG 4, global shutter, split exposure, mono, RAW10 0x9: CONFIG 9, global shutter, single exposure, mono, subsampling x2, RAW8 0xa: CONFIG 10, global shutter, single exposure, mono, subsampling x2, RAW10 0xb: CONFIG 11, global shutter, single exposure, mono, subsampling x4, RAW8 0xc: CONFIG 12, global shutter, single exposure, mono, subsampling x4, RAW10 0xd: CONFIG 13, global shutter, single exposure, mono, subsampling x32, RAW8 0xe: CONFIG 14, global shutter, single exposure, mono, subsampling x32, RAW10 0x1A: CONFIG 26, rolling shutter, SDR, mono, RAW8 0x1B: CONFIG 27, rolling shutter, SDR, mono, RAW10 0x1C: CONFIG 28, rolling shutter, SDR, mono, RAW12 0x20: CONFIG 32, rolling shutter, HDR, mono, RAW10 0x21: CONFIG 33, rolling shutter, HDR, mono, RAW12

Table 10. Description of registers from STREAM_CTX0_STATIC group

Register name	Relative address	Register size	Reset value	Bits	Field name	Description
VIRTUAL_CHANNEL	0x0004	1	0x0	7:0	VALUE	Virtual channel ID for the ROIs of the context
FRAME_LENGTH	0x0006	2	0xA60	15:0	VALUE	Frame length duration in number of lines
ROI_SELECTION	0x0008	1	0x0	3	ROI_D	ROI D: 0x0: (DISABLE) 0x1: (ENABLE)
			0x0	2	ROI_C	ROI C: 0x0: (DISABLE) 0x1: (ENABLE)
			0x0	1	ROI_B	ROI B: 0x0: (DISABLE) 0x1: (ENABLE)
			1 for CTX0/2 0 for CTX1/3	0	ROI_A	ROI A: 0x0: (DISABLE) 0x1: (ENABLE)
GPIO_CTRL	0x0009	1	0x0	3	GPIO3	GPIO3: 0x0: (DISABLE) 0x1: (ENABLE)
			0x0	2	GPIO2	GPIO2: 0x0: (DISABLE) 0x1: (ENABLE)
			0x0	1	GPIO1	GPIO1: 0x0: (DISABLE) 0x1: (ENABLE)
			0x1	0	GPIO0	GPIO0: 0x0: (DISABLE) 0x1: (ENABLE)
DUSTER_CTRL	0x000A	1	0x1	3	NOISE_CORRECTION	Noise correction control: 0x0: (DISABLE) 0x1: (ENABLE)
			0x1	1:0	DYN_ENABLE	Pixel correction control: 0x0: (DISABLE) Disable dynamic correction 0x1: (AUTO) correction of singlets and couplets 0x2: (COUPLET) correction of couplets only
PWL_SEL	0x000B	1	0x0	7:0	VALUE	PWL_LUT_VALUE: 0x0: (DEFAULT_LUT) 0x1: (CUSTOM_LUT only for HDR)
EXPO_STAT_SELECTION	0x000C	1	0 for CTX0/2 1 for CTX1/3	0	SELECT	Statistics computation 0x0: (BEFORE_CFA) 0x1: (AFTER_CFA) - RGB-NIR version only
STAT_ROI_WIDTH_OFFSET	0x000E	2	0x0	15:0	VALUE	Statistics image area where the reference is the output image
STAT_ROI_HEIGHT_OFFSET	0x0010	2	0x0	15:0	VALUE	Statistics image area where the reference is the output image
STAT_ROI_WIDTH	0x0012	2	0xa00	15:0	VALUE	Statistics image area where the reference is the output image
STAT_ROI_HEIGHT	0x0014	2	0x7c0	15:0	VALUE	Statistics image area where the reference is the output image
CHANNEL_STAT_CFG	0x0028	1	0 for CTX0/2 2 for CTX1/3	7:0	CONFIG	Pixel type selection for statistics
HISTO_CFG	0x0029	1	0x0	7:0	CONFIG	Pixel type selection for Histograms
DARKCAL_CTRL	0x002C	1	0x0	7:0	VALUE	0x0: (INDEPENDENT_CHANNELS)

Register name	Relative address	Register size	Reset value	Bits	Field name	Description
						0x1:(GLOBAL_AVG) 0x2:(BYPASS_DARK_AVG)
DARKCAL_PEDESTAL	0x002E	2	0x20	11:0	VALUE	DARKCAL pedestal
DUSTER_NOISE_REDUC_BLEND	0x0030	1	0x10	7:0	VALUE	Gaussian noise filter blending range (with values from 0 to 16)

7 Description of registers from STREAM_CTX0_DYNAMIC group

There are four different DYNAMIC groups to configure the DYNAMIC parameters of the four available contexts.

Table 11. Dynamic groups

Group base address	Group name	Description
0x0C78	STREAM_CTX0_DYNAMIC	Context0 configuration can be live updated during streaming
0x0CA0	STREAM_CTX1_DYNAMIC	Context1 configuration can be live updated during streaming
0x0CC8	STREAM_CTX2_DYNAMIC	Context2 configuration can be live updated during streaming
0x0CF0	STREAM_CTX3_DYNAMIC	Context3 configuration can be live updated during streaming

The table below provides the registers relative address. It must be added to the group base address of the targeted context to get the absolute address.

Table 12. Description of registers from STREAM_CTX0_DYNAMIC group

Register name	Relative address	Register size	Reset value	Bits	Field name	Description
GROUP_PARAMETER_HOLD	0x0000	1	0x0	7:0	VALUE	GPH control for the dynamic current context. When set, it prevents the sensor from applying new GAIN and EXPOSURE settings: 0x00: (no HOLD) 0x01: (HOLD)
ANALOG_GAIN	0x0001	1	0x0	7:0	VALUE	0x00: (AnalogGain_AGAIN_1) 0x01: (AnalogGain_AGAIN_1_07) 0x02: (AnalogGain_AGAIN_1_14) 0x03: (AnalogGain_AGAIN_1_23) 0x04: (AnalogGain_AGAIN_1_33) 0x05: (AnalogGain_AGAIN_1_45) 0x06: (AnalogGain_AGAIN_1_6) 0x06: (AnalogGain_AGAIN_1_6) 0x07: (AnalogGain_AGAIN_1_78) 0x08: (AnalogGain_AGAIN_2) 0x09: (AnalogGain_AGAIN_2_29) 0x0A: (AnalogGain_AGAIN_2_67) 0x0B: (AnalogGain_AGAIN_3_2) 0x0C: (AnalogGain_AGAIN_4)
INTEGRATION_TIME_PRIMARY	0x0002	2	0x99	15:0	VALUE	Integration time in line equivalent: Long exposure in rolling shutter mode. Exposure of all pixels in global shutter single exposure mode. Exposure of RGB (or P1P2P3) pixels in global shutter split exposure mode.
RGB-NIR: INTEGRATION_TIME_IR MONOCHROME: INTEGRATION_TIME_P4	0x0004	2	0x99	15:0	VALUE	Integration time for the NIR pixel (or P4) in line equivalents. Only available for configurations using split exposure.
INTEGRATION_TIME_SHORT	0x0006	2	0x02 for CTX0/2 0x3C for CTX1/3	15:0	VALUE	Integration time in line equivalents. Only available for short exposure in rolling shutter, HDR mode.

Register name	Relative address	Register size	Reset value	Bits	Field name	Description
RGB-NIR: DIGITAL_GAIN_R MONOCHROME: DIGITAL_GAIN_P1	0x0008	2	0x1	12:8	INTEGER	Digital gain (integer part) for R channel or P1 for monochrome version
			0x00	7:0	FRACT	Digital gain (fractional part) for R channel or P1 for monochrome version
RGB-NIR: DIGITAL_GAIN_G MONOCHROME: DIGITAL_GAIN_P4	0x000A	2	0x1	12:8	INTEGER	Digital gain (integer part) for G channel or P4 for monochrome split pixel
			0x00	7:0	FRACT	Digital gain (fractional part) for G channel or P4 for monochrome split pixel
RGB-NIR: DIGITAL_GAIN_B MONOCHROME: DIGITAL_GAIN_P2	0x000C	2	0x1	12:8	INTEGER	Digital gain (integer part) for B channel or P2 for monochrome version
			0x00	7:0	FRACT	Digital gain (fractional part) for B channel or P2 for monochrome version
RGB-NIR: DIGITAL_GAIN_IR MONOCHROME: DIGITAL_GAIN_P3	0x000E	2	0x1	12:8	INTEGER	Digital gain (integer part) for IR channel or P3 for monochrome version
			0x00	7:0	FRACT	Digital gain (fractional part) for IR channel or P3 for monochrome version
DUSTER_DEF_COR_RATIO	0x0010	2	0x64	15:0	VALUE	Control of defective pixel correction intensity with a slider (0% to 200%). The default value is 100%. Higher values decrease the correction, lower values increase it. The slider controls both GS/RS long duster and RS short duster
DUSTER_NOISE_RED_RATIO	0x0012	2	0x64	15:0	VALUE	Control of noise reduction intensity with a slider (0% to 200%). The default value is 100%. Higher values increase the reduction, lower values decrease it. The slider multiplies the output of three noise reduction threshold dampers and controls both GS/RS long duster and RS short duster.

8 Description of registers from OTP_CTM_MIRROR group

Table 13. Description of registers from OTP_CTM_MIRROR group

Register name	Absolute address	Register size	Reset value	Bits	Field name	Description
I2C_ADDRESS	0x0EC4	4	0x0	31:24	I2C_KEY	I^2C key which must be set to 0xAA to allow new I^2C address programming
			0x0	22:16	I2C_DEVICEID_3	New I^2C device ID (without R/W bit)
			0x0	14:8	I2C_DEVICEID_2	New I^2C device ID (without R/W bit)
			0x0	6:0	I2C_DEVICEID_1	New I^2C device ID (without R/W bit)
CTM_AREA_n	0x0EC8 + 4xn (where n = 0 to 73)	296	0x0	31:0	DATA	Nonvolatile customer area

9 Description of registers from DEBUG group

Table 14. Description of registers from DEBUG group

Register name	Absolute address	Register size	Reset value	Bits	Field name	Description
HDR_MERGE_KNEE_1	0x105C	4	0xF3	31:0	VALUE	Value of the first knee point (95%): 0.95 x 2^(12 - 4)
HDR_MERGE_KNEE_2	0x1060	4	0xFA	31:0	VALUE	Value of the second knee point (98%): 0.98 x 2^(12 - 4)
DPHYTX_CTRL	0x108C	1	0x1	4	DPHYTX_CONT_CLK	MIPI clock lane continuous clock: 0x00: (DISABLED) 0x01: (ENABLED)
BOTTOM_STATUS_LINE_DISABLE	0x110C	1	0x0	7:0	VALUE	0x0: (ENABLE) Bottom status line present 0x1: (DISABLE) Bottom status line absent

10 Description of the PWL default values

The custom PWL is loaded during boot with the values below.

Register name	Absolute address	Register size	Reset value
PWL_ABSCISSA_0	0x940	4	0x0
PWL_ABSCISSA_1	0x944	4	0x1
PWL_ABSCISSA_2	0x948	4	0x2
PWL_ABSCISSA_3	0x94C	4	0x3
PWL_ABSCISSA_4	0x950	4	0x4
PWL_ABSCISSA_5	0x954	4	0x6
PWL_ABSCISSA_6	0x958	4	0x8
PWL_ABSCISSA_7	0x95C	4	0xb
PWL_ABSCISSA_8	0x960	4	0x11
PWL_ABSCISSA_9	0x964	4	0x19
PWL_ABSCISSA_10	0x968	4	0x26
PWL_ABSCISSA_11	0x96C	4	0x3a
PWL_ABSCISSA_12	0x970	4	0x55
PWL_ABSCISSA_13	0x974	4	0x7e
PWL_ABSCISSA_14	0x978	4	0xbc
PWL_ABSCISSA_15	0x97C	4	0x115
PWL_ABSCISSA_16	0x980	4	0x1a0
PWL_ABSCISSA_17	0x984	4	0x271
PWL_ABSCISSA_18	0x988	4	0x3a8
PWL_ABSCISSA_19	0x98C	4	0x57d
PWL_ABSCISSA_20	0x990	4	0x838
PWL_ABSCISSA_21	0x994	4	0xc52
PWL_ABSCISSA_22	0x998	4	0x1285
PWL_ABSCISSA_23	0x99C	4	0x1bee
PWL_ABSCISSA_24	0x9A0	4	0x2a43
PWL_ABSCISSA_25	0x9A4	4	0x3fe2
PWL_ABSCISSA_26	0x9A8	4	0x60d3
PWL_ABSCISSA_27	0x9AC	4	0x9286
PWL_ABSCISSA_28	0x9B0	4	0xddf2
PWL_ABSCISSA_29	0x9B4	4	0x150f0
PWL_ABSCISSA_30	0x9B8	4	0x1ffb2
PWL_ABSCISSA_31	0x9BC	4	0x309b3
PWL_ORDINATE_0	0x9C0	4	0x0
PWL_ORDINATE_1	0x9C4	4	0x2d40
PWL_ORDINATE_2	0x9C8	4	0x35c0
PWL_ORDINATE_3	0x9CC	4	0x3b80
PWL_ORDINATE_4	0x9D0	4	0x4000
PWL_ORDINATE_5	0x9D4	4	0x46c0

Register name	Absolute address	Register size	Reset value
PWL_ORDINATE_6	0x9D8	4	0x4c00
PWL_ORDINATE_7	0x9DC	4	0x5280
PWL_ORDINATE_8	0x9E0	4	0x5c00
PWL_ORDINATE_9	0x9E4	4	0x6540
PWL_ORDINATE_10	0x9E8	4	0x7040
PWL_ORDINATE_11	0x9EC	4	0x7d00
PWL_ORDINATE_12	0x9F0	4	0x8980
PWL_ORDINATE_13	0x9F4	4	0x9780
PWL_ORDINATE_14	0x9F8	4	0xa780
PWL_ORDINATE_15	0x9FC	4	0xb880
PWL_ORDINATE_16	0xA00	4	0xcc80
PWL_ORDINATE_17	0xA04	4	0xe240
PWL_ORDINATE_18	0xA08	4	0xfa40
PWL_ORDINATE_19	0xA0C	4	0x11500
PWL_ORDINATE_20	0xA10	4	0x13280
PWL_ORDINATE_21	0xA14	4	0x15340
PWL_ORDINATE_22	0xA18	4	0x17780
PWL_ORDINATE_23	0xA1C	4	0x1a040
PWL_ORDINATE_24	0xA20	4	0x1cd80
PWL_ORDINATE_25	0xA24	4	0x1ffc0
PWL_ORDINATE_26	0xA28	4	0x237c0
PWL_ORDINATE_27	0xA2C	4	0x275c0
PWL_ORDINATE_28	0xA30	4	0x2bac0
PWL_ORDINATE_29	0xA34	4	0x30780
PWL_ORDINATE_30	0xA38	4	0x35d00
PWL_ORDINATE_31	0xA3C	4	0x3bc00
PWL_GRADIANT_0	0xA40	4	0xf6a
PWL_GRADIANT_1	0xA44	4	0xd10
PWL_GRADIANT_2	0xA48	4	0xc70
PWL_GRADIANT_3	0xA4C	4	0xc20
PWL_GRADIANT_4	0xA50	4	0xbb0
PWL_GRADIANT_5	0xA54	4	0xb50
PWL_GRADIANT_6	0xA58	4	0xb15
PWL_GRADIANT_7	0xA5C	4	0xa95
PWL_GRADIANT_8	0xA60	4	0xa28
PWL_GRADIANT_9	0xA64	4	0x9b1
PWL_GRADIANT_10	0xA68	4	0x946
PWL_GRADIANT_11	0xA6C	4	0x8da
PWL_GRADIANT_12	0xA70	4	0x85d
PWL_GRADIANT_13	0xA74	4	0x808
PWL_GRADIANT_14	0xA78	4	0x787

Register name	Absolute address	Register size	Reset value
PWL_GRADIANT_15	0xA7C	4	0x726
PWL_GRADIANT_16	0xA80	4	0x6aa
PWL_GRADIANT_17	0xA84	4	0x63c
PWL_GRADIANT_18	0xA88	4	0x5d3
PWL_GRADIANT_19	0xA8C	4	0x559
PWL_GRADIANT_20	0xA90	4	0x4ff
PWL_GRADIANT_21	0xA94	4	0x476
PWL_GRADIANT_22	0xA98	4	0x415
PWL_GRADIANT_23	0xA9C	4	0x394
PWL_GRADIANT_24	0xAA0	4	0x329
PWL_GRADIANT_25	0xAA4	4	0x2b3
PWL_GRADIANT_26	0xAA8	4	0x23f
PWL_GRADIANT_27	0xAAC	4	0x1d4
PWL_GRADIANT_28	0xAB0	4	0x155
PWL_GRADIANT_29	0xAB4	4	0xf4
PWL_GRADIANT_30	0xAB8	4	0x6d
PWL_GRADIANT_31	0xABC	4	0x1a
PWL_EXPO_BIAS	0xAC0	4	0x0a

11 SYSTEM_WARNING and SYSTEM_ERROR list

-0x0000: No Error
-0x0001: Generic firmware error
-0x0004: UI Configuration Error
-0x0008 to 0x000e: MCU internal error
-0x0010 to 0x0027: Internal error
-0x0028 to 0x002e: Video timing internal error
-0x0030 to 0x0034: ISP internal error
-0x0038 to 0x003e: Output interface internal error
-0x0048 to 0x0052: Internal error
-0x0059 to 0x0060: Streaming error
-0x0100: System PLL lock failed, timed out
-0x0101: MIPI PLL lock failed, timed out
-0x0102: System PLL setup incorrect
-0x0103: MIPI PLL setup incorrect
-0x0104: External clock out of range
-0x0105: System PLL unlock detection time out
-0x0106: MIPI PLL unlock detection time out
-0x0500 to 0x050f: MCU Exceptions
-0x0800 to 0x080c: NVM internal error
-0x0900 to 0x0907: Video timing error
-0x0908: Video timing: GS RGB integration time too long: more than the frame length is programmed
-0x0909: Video timing: GS IR integration time too long: more than the frame length is programmed
-0x090a: Video timing: RS long integration time too long: more than the frame length is programmed
-0x090b: Video timing: RS short integration time too long: more than the frame length is programmed
-0x090c: Video timing: Negative value on VSYNC start delay or VSYNC end delay
-0x090d: Video timing: GS RGB or IR integration time too small. Minimum value applied
-0x0a0a: Pattern generator error
-0x0c00: Bad NVM parameters
-0x0c10: Invalid command
-0x0c11: Bottom status line generation error
-0x0c12: Device model error
-0x1300: Thermal sensor temperature read time out
-0x1301: Thermal sensor wrong data ready
-0x1900 to 0x1902: GPIO configuration error
-0x1e01: CSI transmission error EOF not received: no EOF marker at end of long packet transmission
-0x1e02: CSI transmission error EOF received early: EOF marker received while still expecting data.
-0x1e03: CSI transmission error - underflow / less data at input (info required)
-0x1e04: CSI transmission error - Lane desync error (info required)
-0x2600 to 0x2680: CHANNEL_STAT configuration error
-0x2700: Histogram incorrect ROI X/Y
-0xff0c: DARKCAL invalid configuration

Note: Other error codes not listed here, classified as internal error, can also be raised.

12 Acronyms and abbreviations

Table 15. **Acronyms and abbreviations**

Acronym	Definition
CLK	clock
CFA	color filter array
DT	data transfer
ECC	error correction code
FP	fixed point
FSM	finite state machine
GPH	gain, pulse, hold
GPIO	general-purpose input/output
GS	global shutter
HDR	high dynamic range
ISL	interrupt service routine/image status line
LUT	lookup table
MCU	microcontroller unit
MIPI	mobile industry processor interface
NVM	nonvolatile memory
OTP	one-time programmable
PLL	phase-locked loop
PWL	piecewise linear
PWM	pulse-width modulation
RAM	random-access memory
RGB	red, green, blue
ROI	region of interest
ROM	read-only memory
RS	rolling shutter
SDR	standard dynamic range
UI	user interface
VC	virtual channel
VT	video timing

Revision history

Table 16. **Document revision history**

Date	Version	Changes
7-Apr-2026	1	Initial release
20-Apr-2026	2	Table 12. Description of registers from STREAM_CTX0_DYNAMIC group: Updated description for DUSTER_DEF_COR_RATIO. Updated Section 11: SYSTEM_WARNING and SYSTEM_ERROR list.

Contents

1 Address group summary 2
2 Description of registers from STATUS group 3
3 Description of registers from CMD group 8
4 Description of registers from SENSOR_SETTINGS group 9
5 Description of registers from STREAM_STATIC group 10
6 Description of registers from STREAM_CTX0_STATIC group 14
7 Description of registers from STREAM_CTX0_DYNAMIC group 19
8 Description of registers from OTP_CTM_MIRROR group 21
9 Description of registers from DEBUG group 22
10 Description of the PWL default values 23
11 SYSTEM_WARNING and SYSTEM_ERROR list 26
12 Acronyms and abbreviations 27
Revision history 28

IMPORTANT NOTICE – READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice.

In the event of any conflict between the provisions of this document and the provisions of any contractual arrangement in force between the purchasers and ST, the provisions of such contractual arrangement shall prevail.

The purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgment.

The purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of the purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

If the purchasers identify an ST product that meets their functional and performance requirements but that is not designated for the purchasers' market segment, the purchasers shall contact ST for more information.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2026 STMicroelectronics – All rights reserved