



STUSB4531 register datasheet specifications

Introduction

Address blocks summary

Table 1. STUSB4531 address blocks

Address block base address	Size	Address block name
0x0000	0x0001	STUSB4531

1 STUSB4531 registers summary

Table 2. STUSB4531 registers list

Address offset	Register name	Bit fields
0x0000	Section 2.1: VID_LOW	[7:0] VID_7_0
0x0001	Section 2.2: VID_HIGH	[7:0] VID_15_8
0x0002	Section 2.3: PID_LOW	[7:0] PID_7_0
0x0003	Section 2.4: PID_HIGH	[7:0] PID_15_8
0x0004	Section 2.5: XID_0	[7:0] XID_7_0
0x0005	Section 2.6: XID_1	[7:0] XID_15_8
0x0006	Section 2.7: XID_2	[7:0] XID_23_16
0x0007	Section 2.8: XID_3	[7:0] XID_31_24
0x0008	Section 2.9: FW_REVISION	[7:0] FW_VERSION
0x0009	Section 2.10: HW_REVISION	[7:0] HW_VERSION
0x000A	Section 2.11: PD_REVISION	[7:4] PD_REV_MAJ [3:0] PD_REV_MIN
0x000B	Section 2.12: PD_VERSION	[7:4] PD_VER_MAJ [3:0] PD_VER_MIN
0x000C	Section 2.13: DEVICE_HW	[7:4] FULL_MASK_SET [3:0] METAL_FIX
0x0010	Section 2.14: ALERT_STATUS	[4] CONNECTION_STATUS_AL [3] HW_FAULT_STATUS_AL [2] PD_STATUS_AL [1] PRL_STATUS_AL [0] MONITORING_STATUS_AL
0x0011	Section 2.15: ALERT_STATUS_MASK	[4] CONNECTION_STATUS_AL_MASK [2] PD_STATUS_AL_MASK [1] PRL_STATUS_AL_MASK [0] MONITORING_STATUS_AL_MASK
0x0012	Section 2.16: PD_STATUS_EVENT	[7] TX_BUFFER_READY [2] AMS_STOPPED [1] TRANSITION_END [0] TRANSITION_WINDOW
0x0013	Section 2.17: PD_STATUS_EVENT_MASK	[7] TX_BUFFER_READY_MASK [2] AMS_STOPPED_MASK [1] TRANSITION_END_MASK [0] TRANSITION_WINDOW_MASK
0x0014	Section 2.18: MONITORING_TRANS	[4] VBUS_HIGH_TRANS [3] VBUS_LOW_TRANS [1] VBUS_VALID_TRANS [0] VBUS_VSAFE0V_TRANS
0x0015	Section 2.19: MONITORING_MASK	[4] VBUS_HIGH_MASK [3] VBUS_LOW_MASK [1] VBUS_VALID_AL_MASK

Address offset	Register name	Bit fields
		[0] VBUS_VSAFE0V_MASK
0x0016	Section 2.20: MONITORING_STATUS	[4] VBUS_HIGH_STATUS [3] VBUS_LOW_STATUS [1] VBUS_VALID [0] VBUS_VSAFE0V
0x0017	Section 2.21: PRL_TRANS	[7] PRL_TX_ERR [6] PRL_TX_DISCARD [3] PRL_MSG_SENT [2] PRL_MSG_RECEIVED [1] PRL_HR_DONE [0] PRL_HR_RECEIVED
0x0018	Section 2.22: PRL_STATUS_MASK	[7] PRL_TX_ERR_MASK [6] PRL_TX_DISCARD_MASK [3] PRL_MSG_SENT_MASK [2] PRL_MSG_RECEIVED_MASK [1] PRL_HR_DONE_MASK [0] PRL_HR_RECEIVED_MASK
0x0019	Section 2.23: VBUS_STATUS	[1] VBUS_EN_SNK
0x001A	Section 2.24: CC_STATUS	[7] PLUG_ORIENTATION [6] ATTACH_STATUS [5] LOOKING_4_CONNECTION [4] CONNECT_RESULT [3:2] CC2_STATE [1:0] CC1_STATE
0x001B	Section 2.25: PD_STATUS	[6] VCONN_SRC [5] VCONN_ON [0] DATA_ROLE
0x001C	Section 2.26: HW_FAULT_TRANS	[7] I2C_WATCHDOG [6] CS_OVP [1] TH_WARN_TRANS [0] TH_SHUTDOWN_TRANS
0x001D	Section 2.27: HW_FAULT_STATUS	[1] TH_WARN [0] TH_SHUTDOWN
0x001E	Section 2.28: GPIO_STATUS	[1:0] POWER_OK_STATUS
0x001F	Section 2.29: NVM_STATUS	[7] NVM_LOADED [6] NVM_END_OP [5:0] NVM_WRITE_STATUS
0x0020	Section 2.30: TYPEC_FSM	[3:0] TYPEC_FSM_STATE
0x0021	Section 2.31: PE_FSM	[7:0] PE_FSM_STATE
0x0022	Section 2.32: VBUS_FSM	[7:4] VBUS_CTRL_FSM_STATE [3:0] VBUS_FSM_STATE
0x0023	Section 2.33: MONITORING_DACH_STATUS	[15:5] VVAR_DACH
0x0025	Section 2.34: MONITORING_DACL_STATUS	[15:5] VVAR_DACL
0x0027	Section 2.35: CONNECTION_TRANS	[2] NVM_DOWNLOADED_AL

Address offset	Register name	Bit fields
		[1] CC_STATUS_AL [0] ATTACH_STATUS_AL
0x0028	Section 2.36: CONNECTION_MASK	[2] NVM_DOWNLOADED_AL_MASK [1] CC_STATUS_AL_MASK [0] ATTACH_STATUS_AL_MASK
0x0031	Section 2.37: COMMAND	[3:0] CMD
0x0032	Section 2.38: RX_MSG_DETECT	[6] CABLE_RESET_RX_EN [5] HARD_RESET_RX_EN [4] SOP_DBG2_RX_EN [3] SOP_DBG1_RX_EN [2] SOP2_RX_EN [1] SOP1_RX_EN [0] SOP_RX_EN
0x0033	Section 2.39: RESET_CTRL	[1] ERROR_RECOVERY_EN
0x0034	Section 2.40: VBUS_CTRL	[1] SINK_VBUS_EN
0x0035	Section 2.41: MONITORING_CTRL	[4] CV_CL_MODE [2] VBUS_HIGH_ENABLE [1] VBUS_LOW_ENABLE [0] VBUS_CTRL_LOW_MASK
0x0036	Section 2.42: MONITORING_DACH_CTRL	[15:5] VVAR_DACH_SEL [1] DACH_INPUT_SEL [0] COMPH_ENABLE_SEL
0x0038	Section 2.43: MONITORING_DACL_CTRL	[15:5] VVAR_DACL_SEL [1] DACL_INPUT_SEL [0] COMPL_ENABLE_SEL
0x003A	Section 2.44: MONITORING_SHIFT_CTRL	[5:4] SHIFT_H [1:0] SHIFT_L
0x003B	Section 2.45: VBUS_DISCHARGE_CTRL	[2] DISCH_CTRL_SEL [1] VBUS_VS_DISCH_EN [0] DISCH_EN
0x003C	Section 2.46: VBUS_DISCHARGE_TIME_CTRL	[7:3] DISCHARGE_TIME_TO_0V [2:0] DISCHARGE_TIME_TRANSITION
0x003D	Section 2.47: DEVICE_CTRL	[5] VBUS_CTRL_SW [2] WATCHDOG_EN
0x003E	Section 2.48: APPLI_CTRL	[7] DRS_AUTO_ACCEPT [5] PDO_0MA_MISMATCH [4] MISMATCH_5V [3] MISMATCH_PD [1] OPERATING_CURRENT_SEL [0] ABOVE_5V
0x003F	Section 2.49: DPM_CTRL	[7] VCONN_EN [6] VCONN_SWAP_2_ON [5] VCONN_SWAP_2_OFF [4] DR_SWAP_2_UFP

Address offset	Register name	Bit fields
		[3] DR_SWAP_2_DFP [2] BAT_PRES [1] BAT_SWP [0] VDM_SUPPORT
0x0040	Section 2.50: GPIO_CTRL	[7] SW_GPOD [1:0] POWER_OK
0x0041	Section 2.51: NVM_CUST_CTRL	[7] NVM_MODE [5:4] NVM_CUST_SECT [2:0] NVM_CUST_OPCODE
0x0050	Section 2.52: GPIO_SETTING	[2:0] GPIO_CONF
0x0051	Section 2.53: DEVICE_PDP	[7:0] PDP
0x0052	Section 2.54: NUM_PDO	[6:4] NUM_SRC_PDO [1:0] NUM_SNK_FIX_PDO
0x0053	Section 2.55: SNK_PDO_PARAMS	[7:6] VSAFE_5V_CURRENT [5:4] PDO3_VSEL [3:2] PDO2_VSEL [1] PDO3_CURRENT [0] PDO2_CURRENT
0x0054	Section 2.56: SNK_PDO_CAPABILITIES	[15:8] VSEL_VARIABLE_HIGH [7:6] VSEL_VARIABLE_LOW [5] EPR_CAPABLE [4] DRD_CAPABLE [2] USB_COM_CAPABLE [1] UNCONSTRAINED_POWER [0] HIGHER_CAPABILITY
0x0056	Section 2.57: ALGO	[7:6] SINK_FEATURE [4] PPS_PRIORITY [3:2] PPS_VOLTAGE_SELECTION
0x0057	Section 2.58: SNK_APDO_FILL_1	[7:0] MAX_VOLTAGE
0x0058	Section 2.59: SNK_APDO_FILL_2	[7:0] MIN_VOLTAGE
0x0059	Section 2.60: SNK_APDO_FILL_3	[6:0] MAX_CURRENT
0x005A	Section 2.61: DEVICE_SETTING	[1:0] DEV_SETTING
0x005C	Section 2.62: REQUEST_SRC_PDP	[5:4] SINK_MAX_PDP [3:2] SINK_OP_PDP [1:0] SINK_MIN_PDP
0x0060	Section 2.63: RX_BYTE_CNT	[5:0] RX_BYTE_COUNT
0x0061	Section 2.64: RX_FRAME_TYPE	[2:0] RX_TYPE
0x0062	Section 2.65: RX_HEADER	[15:0] RX_HEAD
0x0064	Section 2.66: RX_DATA_OBJ_224BITS	[7:0] RX_OBJ
0x0080	Section 2.67: PRT_TX_CTRL	[5:4] PRT_RETRY_MSG_CNT [2:0] PRT_TX_SOP_MSG
0x0081	Section 2.68: TX_BYTE_CNT	[7:0] TX_BYTE_COUNT
0x0082	Section 2.69: TX_HEADER	[15:0] TX_HEAD

Address offset	Register name	Bit fields
0x0084	Section 2.70: TX_DATA_OBJ_224BITS	[7:0] TX_OBJ
0x00A0	Section 2.71: DPM_SRC_PDO1	[31:0] SRC_PDO1
0x00A4	Section 2.72: DPM_SRC_PDO2	[31:0] SRC_PDO2
0x00A8	Section 2.73: DPM_SRC_PDO3	[31:0] SRC_PDO3
0x00AC	Section 2.74: DPM_SRC_PDO4	[31:0] SRC_PDO4
0x00B0	Section 2.75: DPM_SRC_PDO5	[31:0] SRC_PDO5
0x00B4	Section 2.76: DPM_SRC_PDO6	[31:0] SRC_PDO6
0x00B8	Section 2.77: DPM_SRC_PDO7	[31:0] SRC_PDO7
0x00BC	Section 2.78: DPM_RDO	[31:0] RDO
0x00C0	Section 2.79: DPM_ALGO_RESULT	[31:0] ALGO_RESULT
0x00C4	Section 2.80: DPM_SRC_PDO_NEGOCIATED	[31:0] SRC_PDO_NEGOCIATED

2 Registers description

2.1 VID_LOW

7	6	5	4	3	2	1	0
VID_7_0 [7:0]							
RW							

Address:	0x0000
Reset:	0x00
[7:0]	VID_7_0: NVM_INIT parameter: FTP_VID_7_0

2.2 VID_HIGH

7	6	5	4	3	2	1	0
VID_15_8 [7:0]							
RW							

Address:	0x0001
Reset:	0x00
[7:0]	VID_15_8: NVM_INIT parameter: FTP_VID_15_8

2.3 PID_LOW

7	6	5	4	3	2	1	0
PID_7_0 [7:0]							
RW							

Address:	0x0002
Reset:	0x00
[7:0]	PID_7_0: NVM_INIT parameter: FTP_PID_7_0

2.4 PID_HIGH

7	6	5	4	3	2	1	0
PID_15_8 [7:0]							
RW							

Address:	0x0003
Reset:	0x00
[7:0]	PID_15_8: NVM_INIT parameter: FTP_PID_15_8

2.5 XID_0

7	6	5	4	3	2	1	0
XID_7_0 [7:0]							
RW							

Address:	0x0004
Reset:	0x00
[7:0]	XID_7_0: NVM_INIT parameter: FTP_XID_7_0

2.6 XID_1

7	6	5	4	3	2	1	0
XID_15_8 [7:0]							
RW							

Address:	0x0005
Reset:	0x00
[7:0]	XID_15_8: NVM_INIT parameter: FTP_XID_15_8

2.7 **XID_2**

7	6	5	4	3	2	1	0
XID_23_16 [7:0]							
RW							

Address:	0x0006
Reset:	0x00
[7:0]	XID_23_16: NVM_INIT parameter: FTP_XID_23_16

2.8 XID_3

7	6	5	4	3	2	1	0
XID_31_24 [7:0]							
RW							

Address:	0x0007
Reset:	0x00
[7:0]	XID_31_24: NVM_INIT parameter: FTP_XID_31_24

2.9 FW_REVISION

7	6	5	4	3	2	1	0
FW_VERSION [7:0]							
RW							

Address:	0x0008
Reset:	0x00
[7:0]	FW_VERSION:

2.10 HW_REVISION

7	6	5	4	3	2	1	0
HW_VERSION [7:0]							
RW							

Address:	0x0009
Reset:	0x00
[7:0]	HW_VERSION: NVM_INIT parameter: FTP_HW_VERSION

2.11 PD_REVISION

7	6	5	4	3	2	1	0
PD_REV_MAJ [7:4]				PD_REV_MIN [3:0]			
RW				RW			

Address:	0x000A
Reset:	0x00
[7:4]	PD_REV_MAJ: Power delivery major revision figure: - 0x1: (PD_REV_MAJ_1) first major revision. - 0x2: (PD_REV_MAJ_2) second major revision. - 0x3: (PD_REV_MAJ_3) third major revision. NVM_INIT parameter: FTP_PD_REV_MAJ
[3:0]	PD_REV_MIN: Power delivery minor revision figure: - 0x0: (PD_REV_MIN_0) zero minor revision. - 0x1: (PD_REV_MIN_1) first minor revision. - 0x2: (PD_REV_MIN_2) second minor revision. - 0x3: (PD_REV_MIN_3) third minor revision. NVM_INIT parameter: FTP_PD_REV_MIN

2.12 PD_VERSION

7	6	5	4	3	2	1	0
PD_VER_MAJ [7:4]				PD_VER_MIN [3:0]			
RW				RW			

Address:	0x000B
Reset:	0x00
[7:4]	PD_VER_MAJ: Power delivery major version figure: - 0x1: (PD_VER_MAJ_1) first major version. - 0x2: (PD_VER_MAJ_2) second major version. - 0x3: (PD_VER_MAJ_3) third major version. NVM_INIT parameter: FTP_PD_VER_MAJ
[3:0]	PD_VER_MIN: Power delivery minor version figure: - 0x0: (PD_VER_MIN_0) zero minor version. - 0x1: (PD_VER_MIN_1) first minor version. - 0x2: (PD_VER_MIN_2) second minor version. - 0x3: (PD_VER_MIN_3) third minor version. NVM_INIT parameter: FTP_PD_VER_MIN

2.13 DEVICE_HW

7	6	5	4	3	2	1	0
FULL_MASK_SET [7:4]				METAL_FIX [3:0]			
R				R			

Address:	0x000C
Reset:	0x13
[7:4]	FULL_MASK_SET: Device HW version: full mask number.
[3:0]	METAL_FIX: Device HW version: metal fix mask number.

2.14 ALERT_STATUS

7	6	5	4	3	2	1	0
Reserved			CONNECTION_STATUS_AL	HW_FAULT_STATUS_AL	PD_STATUS_AL	PRL_STATUS_AL	MONITORING_STATUS_AL
			R	R	R	R	R

Address:	0x0010
Reset:	0x00
[4]	CONNECTION_STATUS_AL: CONNECTION_STATUS alert: - 0x0: (CONNECTION_STATUS_AL_CLR) alert cleared. - 0x1: (CONNECTION_STATUS_AL_SET) alert set.
[3]	HW_FAULT_STATUS_AL: HW_FAULT_STATUS alert: - 0x0: (HW_FAULT_STATUS_AL_CLR) alert cleared. - 0x1: (HW_FAULT_STATUS_AL_SET) alert set.
[2]	PD_STATUS_AL: PD_STATUS alert: - 0x0: (PD_STATUS_AL_CLR) alert cleared. - 0x1: (PD_STATUS_AL_SET) alert set.
[1]	PRL_STATUS_AL: PRL_STATUS alert: - 0x0: (PRL_STATUS_AL_CLR) alert cleared. - 0x1: (PRL_STATUS_AL_SET) alert set.
[0]	MONITORING_STATUS_AL: MONITORING_STATUS alert: - 0x0: (MONITORING_STATUS_AL_CLR) alert cleared. - 0x1: (MONITORING_STATUS_AL_SET) alert set.

2.15 ALERT_STATUS_MASK

7	6	5	4	3	2	1	0
Reserved			CONNECTION_STATUS_AL_MASK	Reserved	PD_STATUS_AL_MASK	PRL_STATUS_AL_MASK	MONITORING_STATUS_AL_MASK
			RW		RW	RW	RW

Address:	0x0011
Reset:	0xFF
[4]	CONNECTION_STATUS_AL_MASK: CONNECTION_STATUS_AL mask: - 0x0: (CONNECTION_STATUS_AL_MASK_DIS) mask disabled. - 0x1: (CONNECTION_STATUS_AL_MASK_EN) mask enabled. NVM_INIT parameter: FTP_CONNECTION_STATUS_AL_MASK
[2]	PD_STATUS_AL_MASK: PD_STATUS_AL mask: - 0x0: (PD_STATUS_AL_MASK_DIS) mask disabled. - 0x1: (PD_STATUS_AL_MASK_EN) mask enabled. NVM_INIT parameter: FTP_PD_STATUS_AL_MASK
[1]	PRL_STATUS_AL_MASK: PRL_STATUS_AL mask: - 0x0: (PRL_STATUS_AL_MASK_DIS) mask disabled. - 0x1: (PRL_STATUS_AL_MASK_EN) mask enabled. NVM_INIT parameter: FTP_PRT_STATUS_AL_MASK
[0]	MONITORING_STATUS_AL_MASK: MONITORING_STATUS_AL mask: - 0x0: (MON_STATUS_AL_MASK_DIS) mask disabled. - 0x1: (MON_STATUS_AL_MASK_EN) mask enabled. NVM_INIT parameter: FTP_MONITORING_STATUS_MASK

2.16 PD_STATUS_EVENT

7	6	5	4	3	2	1	0
TX_BUFFER_READY	Reserved				AMS_STOPPED	TRANSITION_END	TRANSITION_WINDOW
RC					RC	RC	RC

Address:	0x0012
Reset:	0x00
[7]	TX_BUFFER_READY: Tx buffer is finished to be written by PE: - 0x0: (TX_BUFFER_READY_OFF) no event. - 0x1: (TX_BUFFER_READY_ON) event happened.
[2]	AMS_STOPPED: AMS ongoing stopped by PE. - 0x0: (AMS_STOPPED_CLR) no event. - 0x1: (AMS_STOPPED_SET) event happened.
[1]	TRANSITION_END: PS ready message was received power transition is ended. - 0x0: (TRANSITION_END_CLR) no event. - 0x1: (TRANSITION_END_SET) event happened.
[0]	TRANSITION_WINDOW: Request Message was accepted power transition will start. - 0x0: (TRANSITION_WINDOW_CLR) no event. - 0x1: (TRANSITION_WINDOW_SET) event happened.

2.17 PD_STATUS_EVENT_MASK

7	6	5	4	3	2	1	0
TX_BUFFER_READY_MASK	Reserved				AMS_STOPPED_MASK	TRANSITION_END_MASK	TRANSITION_WINDOW_MASK
RW					RW	RW	RW

Address:	0x0013
Reset:	0x87
[7]	TX_BUFFER_READY_MASK: TX_BUFFER_READY mask. - 0x0: (TX_BUFFER_READY_MASK_DIS) mask disabled. - 0x1: (TX_BUFFER_READY_MASK_EN) mask enabled. NVM_INIT parameter: FTP_TX_BUFFER_READY_MASK
[2]	AMS_STOPPED_MASK: AMS stopped event is masked. - 0x0: (AMS_STOPPED_MASK_DIS) mask disabled. - 0x1: (AMS_STOPPED_MASK_EN) mask enabled. NVM_INIT parameter: FTP_AMS_STOPPED_MASK
[1]	TRANSITION_END_MASK: PS ready message event is masked. - 0x0: (TRANSITION_END_MASK_DIS) mask disabled. - 0x1: (TRANSITION_END_MASK_EN) mask enabled. NVM_INIT parameter: FTP_TRANSITION_END_MASK
[0]	TRANSITION_WINDOW_MASK: Resquest Message event is masked. - 0x0: (TRANSITION_WINDOW_MASK_DIS) mask disabled. - 0x1: (TRANSITION_WINDOW_MASK_EN) mask enabled. NVM_INIT parameter: FTP_TRANSITION_WINDOW_MASK

2.18 MONITORING_TRANS

7	6	5	4	3	2	1	0
Reserved			VBUS_HIGH_TRANS	VBUS_LOW_TRANS	Reserved	VBUS_VALID_TRANS	VBUS_VSAFE0V_TRANS
			RC	RC		RC	RC

Address:	0x0014
Reset:	0x00
[4]	VBUS_HIGH_TRANS: Transition on VBUS_HIGH_STATUS bit reported: - 0x0: (VBUS_HIGH_TRANS_CLR) No transition. - 0x1: (VBUS_HIGH_TRANS_SET) Transition occurred on VBUS_HIGH_STATUS bit.
[3]	VBUS_LOW_TRANS: Transition on VBUS_LOW_STATUS bit reported: - 0x0: (VBUS_LOW_TRANS_CLR) No transition. - 0x1: (VBUS_LOW_TRANS_SET) Transition occurred on VBUS_LOW_STATUS bit.
[1]	VBUS_VALID_TRANS: Transition on VBUS_VALID bit reported: - 0x0: (VBUS_VALID_TRANS_CLR) No transition. - 0x1: (VBUS_VALID_TRANS_SET) Transition occurred on VBUS_VALID bit.
[0]	VBUS_VSAFE0V_TRANS: Transition on VBUS_VSAFE0V bit reported: - 0x0: (VBUS_VSAFE0V_TRANS_CLR) No transition. - 0x1: (VBUS_VSAFE0V_TRANS_SET) Transition occurred on VBUS_VSAFE0V bit.

2.19 MONITORING_MASK

7	6	5	4	3	2	1	0
Reserved			VBUS_HIGH_MASK	VBUS_LOW_MASK	Reserved	VBUS_VALID_AL_MASK	VBUS_VSAFE0V_MASK
			RW	RW		RW	RW

Address:	0x0015
Reset:	0xFF
[4]	VBUS_HIGH_MASK: VBUS_HIGH transition is masked. - 0x0: (VBUS_HIGH_MASK_DIS) mask disabled. - 0x1: (VBUS_HIGH_MASK_EN) mask enabled.
[3]	VBUS_LOW_MASK: VBUS_LOW transition is masked. - 0x0: (VBUS_LOW_MASK_DIS) mask disabled. - 0x1: (VBUS_LOW_MASK_EN) mask enabled.
[1]	VBUS_VALID_AL_MASK: VBUS_VALID transition is masked. - 0x0: (VBUS_VALID_MASK_DIS) mask disabled. - 0x1: (VBUS_VALID_MASK_EN) mask enabled.
[0]	VBUS_VSAFE0V_MASK: VBUS_VSAFE0V transition is masked. - 0x0: (VBUS_VSAFE0V_MASK_DIS) mask disabled. - 0x1: (VBUS_VSAFE0V_MASK_EN) mask enabled.

2.20 MONITORING_STATUS

7	6	5	4	3	2	1	0
Reserved			VBUS_HIGH_STATUS	VBUS_LOW_STATUS	Reserved	VBUS_VALID	VBUS_VSAFE0V
			R	R		R	R

Address:	0x0016
Reset:	0x00
[4]	VBUS_HIGH_STATUS: Vbus high threshold comparator status : - 0x0: (VBUS_HIGH_OK) VBUS below high threshold. - 0x1: (VBUS_HIGH_KO) VBUS above high threshold (Over voltage condition).
[3]	VBUS_LOW_STATUS: VBUS_LOW status updated during VBUS_READY transtion from HIGH to LOW. - 0x0: (VBUS_LOW_OK) VBUS above low threshold. - 0x1: (VBUS_LOW_KO) VBUS below low threshold (Under voltage condition).
[1]	VBUS_VALID: VBUS compare to 2V9 threshold in falling and 4V01 in rising: - 0x0: (VBUS_BELOW_2V9) VBUS below 2V9. - 0x1: (VBUS_ABOVE_4V01) VBUS above 4V01.
[0]	VBUS_VSAFE0V: - 0x0: (VBUS_VSAFE0V_KO) VBUS is above 0.6V on VBUS_SENSE input pin. - 0x1: (VBUS_VSAFE0V_OK) VBUS is below 0.6V on VBUS_SENSE input pin.

2.21 PRL_TRANS

7	6	5	4	3	2	1	0
PRL_TX_ERR	PRL_TX_DISCARD	Reserved		PRL_MSG_SENT	PRL_MSG_RECEIVED	PRL_HR_DONE	PRL_HR_RECEIVED
RC	RC			RC	RC	RC	RC

Address:	0x0017
Reset:	0x00
[7]	PRL_TX_ERR: TX error on the Protocol Layer. - 0x0: (TX_ERROR_CLR) no event. - 0x1: (TX_ERROR_SET) event happened.
[6]	PRL_TX_DISCARD: TX message discarded at the Protocol Layer. - 0x0: (TX_DISCARD_CLR) no event. - 0x1: (TX_DISCARD_SET) event happened.
[3]	PRL_MSG_SENT: Message sent from the Protocol Layer when GoodCRC is received. - 0x0: (MSG_NOT_SENT) no event. - 0x1: (MSG_SENT) event happened.
[2]	PRL_MSG_RECEIVED: Message is received. - 0x0: (MSG_NOT_RECEIVED) no event. - 0x1: (MSG_RECEIVED) event happened.
[1]	PRL_HR_DONE: PD hardreset executed (hardware reset has to be completed to set the flag). - 0x0: (HR_NOT_DONE) no event. - 0x1: (HR_DONE) event happened.
[0]	PRL_HR_RECEIVED: PD hardreset request coming from RX. - 0x0: (HR_NOT_RECEIVED) no event. - 0x1: (HR_RECEIVED) event happened.

2.22 PRL_STATUS_MASK

7	6	5	4	3	2	1	0
PRL_TX_ERR_MASK	PRL_TX_DISCARD_MASK	Reserved		PRL_MSG_SENT_MASK	PRL_MSG_RECEIVED_MASK	PRL_HR_DONE_MASK	PRL_HR_RECEIVED_MASK
RW	RW			RW	RW	RW	RW

Address:	0x0018
Reset:	0xFF
[7]	PRL_TX_ERR_MASK: TX error on the Protocol Layer is masked. - 0x0: (TX_ERROR_MASK_DIS) mask disabled. - 0x1: (TX_ERROR_MASK_EN) mask enabled.
[6]	PRL_TX_DISCARD_MASK: TX message discarded at the Protocol Layer is masked. - 0x0: (TX_DISCARD_MASK_DIS) mask disabled. - 0x1: (TX_DISCARD_MASK_EN) mask enabled.
[3]	PRL_MSG_SENT_MASK: Message sent from the Protocol Layer when GoodCRC is received is masked. - 0x0: (MSG_SENT_MASK_DIS) mask disabled. - 0x1: (MSG_SENT_MASK_EN) mask enabled.
[2]	PRL_MSG_RECEIVED_MASK: Message is received is masked. - 0x0: (MSG_RECEIVED_MASK_DIS) mask disabled. - 0x1: (MSG_RECEIVED_MASK_EN) mask enabled.
[1]	PRL_HR_DONE_MASK: PD hardreset executed interrupt is masked. - 0x0: (HR_DONE_MASK_DIS) mask disabled. - 0x1: (HR_DONE_MASK_EN) mask enabled.
[0]	PRL_HR_RECEIVED_MASK: PD hardreset request coming from RX is masked. - 0x0: (HR_RECEIVED_MASK_DIS) mask disabled. - 0x1: (HR_RECEIVED_MASK_EN) mask enabled.

2.23 VBUS_STATUS

7	6	5	4	3	2	1	0
Reserved						VBUS_EN_SNK	Reserved
						R	

Address:	0x0019
Reset:	0x00
[1]	VBUS_EN_SNK: sink power switch status. - 0x0: (VBUS_EN_SNK_OPEN) VBUS_EN_SNK switch open. - 0x1: (VBUS_EN_SNK_CLOSE) VBUS_EN_SNK switch close.

2.24 CC_STATUS

7	6	5	4	3	2	1	0
PLUG_ORIENTATION	ATTACH_STATUS	LOOKING_4_CONNECTION	CONNECT_RESULT	CC2_STATE [3:2]		CC1_STATE [1:0]	
R	R	R	R	R		R	

Address:	0x001A
Reset:	0x00
[7]	PLUG_ORIENTATION: Plug orientation: - 0x0: (PLUG_DIRECT) direct orientation. - 0x1: (PLUG_REVERSE) reverse orientation.
[6]	ATTACH_STATUS: Attachment flag: - 0x0: (DEV_UNATTACHED) device unattached. - 0x1: (DEV_ATTACHED) device attached.
[5]	LOOKING_4_CONNECTION: - 0x0: (LOOKING_4_CONNECTION_OFF) The device is not actively looking for a connection. A transition from '1' to '0' indicates a potential connection has been found. - 0x1: (LOOKING_4_CONNECTION_ON) The device is looking for a connection.
[4]	CONNECT_RESULT: - 0x1: (DEV_RD) The device is presenting Rd.
[3:2]	CC2_STATE: if (CONNECT_RESULT = 1). This field returns b00 if (LOOKING_4_CONNECTION=1). - 0x0: (SNK_OPEN) SNK.Open (below maximum vRa). - 0x1: (SNK_DEFAULT) SNK.Default (Above minimum vRd-Connect). - 0x2: (SNK_POWER_1_5) SNK.Power1.5 (Above minimum vRd-Connect) Detect Rp 1.5A. - 0x3: (SNK_POWER_3_0) SNK.Power3.0 (Above minimum vRd-Connect) Detects Rp 3.0A.
[1:0]	CC1_STATE: if (CONNECT_RESULT = 1). This field returns b00 if (LOOKING_4_CONNECTION=1). - 0x0: (SNK_OPEN) SNK.Open (below maximum vRa). - 0x1: (SNK_DEFAULT) SNK.Default (Above minimum vRd-Connect). - 0x2: (SNK_POWER_1_5) SNK.Power1.5 (Above minimum vRd-Connect) Detect Rp 1.5A. - 0x3: (SNK_POWER_3_0) SNK.Power3.0 (Above minimum vRd-Connect) Detects Rp 3.0A.

2.25 PD_STATUS

7	6	5	4	3	2	1	0
Reserved	VCONN_SRC	VCONN_ON	Reserved				DATA_ROLE
	R	R					R

Address:	0x001B
Reset:	0x00
[6]	VCONN_SRC: Device is vconn source: - 0x0: (VCONN_SRC_OFF) Device is not the vconn source. - 0x1: (VCONN_SRC_ON) Device is the vconn source.
[5]	VCONN_ON: Vconn applied on CC line. - 0x0: (VCONN_OFF) Vconn supply is not detected on CC line. - 0x1: (VCONN_ON) Vconn supply is detected on CC line.
[0]	DATA_ROLE: Data role: - 0x0: (DR_UFP) UFP. - 0x1: (DR_DFP) DFP.

2.26 HW_FAULT_TRANS

7	6	5	4	3	2	1	0
I2C_WATCHDOG	CS_OVP	Reserved				TH_WARN_TRANS	TH_SHUTDOWN_TRANS
RC	RC					RC	RC

Address:	0x001C
Reset:	0x00
[7]	I2C_WATCHDOG: I2C communication event: - 0x0: (I2C_COM_OK) I2C communication OK. - 0x1: (I2C_COM_KO) I2C communication KO.
[6]	CS_OVP: CC lines overvoltage event: - 0x0: (CS_OVP_OK) CC lines voltage OK. - 0x1: (CS_OVP_KO) CC lines voltage KO.
[1]	TH_WARN_TRANS: Thermal warning event: - 0x0: (TH_WARN_EVENT_OK) device temperature stays under the warning threshold. - 0x1: (TH_WARN_EVENT_KO) device temperature has crossed the warning threshold.
[0]	TH_SHUTDOWN_TRANS: Thermal shutdown event: - 0x0: (TH_SD_EVENT_OK) device temperature stays under the shutdown threshold. - 0x1: (TH_SD_EVENT_KO) device temperature has crossed the shutdown threshold.

2.27 HW_FAULT_STATUS

7	6	5	4	3	2	1	0
Reserved						TH_WARN	TH_SHUTDOWN
						R	R

Address:	0x001D
Reset:	0x00
[1]	TH_WARN: Thermal warning status: - 0x0: (TH_WARN_OK) device temperature under the warning threshold. - 0x1: (TH_WARN_KO) device temperature over the warning threshold.
[0]	TH_SHUTDOWN: Thermal shutdown status: - 0x0: (TH_SD_OK) device temperature under the shutdown threshold. - 0x1: (TH_SD_KO) device temperature over the shutdown threshold.

2.28 GPIO_STATUS

7	6	5	4	3	2	1	0
Reserved						POWER_OK_STATUS [1:0]	
						R	

Address:	0x001E
Reset:	0x00
[1:0]	POWER_OK_STATUS: SNK_PDO accepted in the power negotiation : - 0x0: (POWER_OK1_STAT) fix SNK PDO1 (5V). - 0x1: (POWER_OK2_STAT) fix SNK PDO2. - 0x2: (POWER_OK3_STAT) fix SNK PDO3. - 0x3: (POWER_OK4_STAT) variable or PSS SNK PDO.

2.29 NVM_STATUS

7	6	5	4	3	2	1	0
NVM_LOADED	NVM_END_OP	NVM_WRITE_STATUS [5:0]					
R	R	R					

Address:	0x001F
Reset:	0x00
[7]	NVM_LOADED: Device NVM data load in registers: - 0x0: (NO_NVM_LOAD) load not yet done. - 0x1: (NVM_LOAD_DONE) load completed.
[6]	NVM_END_OP: NVM operation status: - 0x0: (NVM_OP_ONGOING) the operation is on going. - 0x1: (NVM_OP_ENDED) the operation is finished.
[5:0]	NVM_WRITE_STATUS: Verify result after last write operation. Each bit represents 1 sector (bit 0 => sector 0 ... bit 5 => sector 5).

2.30 TYPEC_FSM

7	6	5	4	3	2	1	0
Reserved				TYPEC_FSM_STATE [3:0]			
				R			

Address:	0x0020
Reset:	0x00
[3:0]	TYPEC_FSM_STATE: TypeC FSM states: - 0x0: (TYPEC_UNATTACHED_SNK) TYPEC_UNATTACHED_SNK state. - 0x1: (TYPEC_ATTACHWAIT_SNK) TYPEC_ATTACHWAIT_SNK state. - 0x2: (TYPEC_UNATTACHEDWAIT) TYPEC_UNATTACHEDWAIT state. - 0x3: (TYPEC_ATTACHED_SNK) TYPEC_ATTACHED_SNK state. - 0x4: (TYPEC_DEB_ACC_SNK) TYPEC_DEB_ACC_SNK state. - 0xD: (TYPEC_ERRORRECOVERY) TYPEC_ERRORRECOVERY state. - 0xE: (TYPEC_UNATTACHED) TYPEC_UNATTACHED state.

2.31 PE_FSM

7	6	5	4	3	2	1	0
PE_FSM_STATE [7:0]							
R							

Address:	0x0021
Reset:	0x00
[7:0]	PE_FSM_STATE: PE FSM states: - 0x00: (PE_INIT) PE_INIT state. - 0x01: (PE_SOFT_RESET) PE_SOFT_RESET state. - 0x02: (PE_HARD_RESET) PE_HARD_RESET state. - 0x03: (PE_SEND_HARD_RESET) PE_SEND_HARD_RESET state. - 0x04: (PE_SEND_SOFT_RESET_1) PE_SEND_SOFT_RESET_1 state. - 0x05: (PE_SEND_SOFT_RESET_2) PE_SEND_SOFT_RESET_2 state. - 0x06: (PE_BIST_CARRIER_MODE) PE_BIST_CARRIER_MODE state. - 0x07: (PE_BIST_TEST_MODE) PE_BIST_TEST_MODE state. - 0x08: (PE_HARD_RESET_SHUTDOWN) PE_HARD_RESET_SHUTDOWN state. - 0x09: (PE_SNK_STARTUP) PE_SNK_STARTUP state. - 0x0A: (PE_SNK_DISCOVERY) PE_SNK_DISCOVERY state. - 0x0B: (PE_SNK_WAIT_FOR_CAPABILITIES) PE_SNK_WAIT_FOR_CAPABILITIES state. - 0x0C: (PE_SNK_EVALUATE_CAPABILITIES) PE_SNK_EVALUATE_CAPABILITIES state. - 0x0D: (PE_SNK_SELECT_CAPABILITIES_1) PE_SNK_SELECT_CAPABILITIES_1 state. - 0x0E: (PE_SNK_SELECT_CAPABILITIES_2) PE_SNK_SELECT_CAPABILITIES_2 state. - 0x0F: (PE_SNK_TRANSITION_SINK) PE_SNK_TRANSITION_SINK state. - 0x10: (PE_SNK_READY) PE_SNK_READY state. - 0x11: (PE_SNK_GET_SOURCE_CAP) PE_SNK_GET_SOURCE_CAP state. - 0x12: (PE_SNK_READY_SENDING) PE_SNK_READY_SENDING state. - 0x13: (PE_DRS_EVALUATE_DR_SWAP) PE_DRS_EVALUATE_DR_SWAP state. - 0x14: (PE_DRS_CHANGE_TO_DRP) PE_DRS_CHANGE_TO_DRP state. - 0x15: (PE_DRS_REJECT_DR_SWAP) PE_DRS_REJECT_DR_SWAP state. - 0x16: (PE_DRS_ACCEPT_DR_SWAP) PE_DRS_ACCEPT_DR_SWAP state. - 0x17: (PE_DRS_SEND_DR_SWAP) PE_DRS_SEND_DR_SWAP state. - 0x18: (PE_VCS_SEND_SWAP) PE_VCS_SEND_SWAP state. - 0x19: (PE_VCS_WAIT_FOR_VCONN) PE_VCS_WAIT_FOR_VCONN state. - 0x1A: (PE_VCS_TURN_ON_VCONN) PE_VCS_TURN_ON_VCONN state. - 0x1B: (PE_VCS_REJECT_VCONN_SWAP) PE_VCS_REJECT_VCONN_SWAP state. - 0x1C: (PE_VCS_EVALUATE_SWAP) PE_VCS_EVALUATE_SWAP state. - 0x1D: (PE_VCS_ACCEPT_SWAP) PE_VCS_ACCEPT_SWAP state. - 0x1E: (PE_VCS_TURN_OFF_VCONN) PE_VCS_TURN_OFF_VCONN state. - 0x1F: (PE_VCS_SEND_PS_RDY) PE_VCS_SEND_PS_RDY state.

2.32 VBUS_FSM

7	6	5	4	3	2	1	0
VBUS_CTRL_FSM_STATE [7:4]				VBUS_FSM_STATE [3:0]			
R				R			

Address:	0x0022
Reset:	0x00
[7:4]	VBUS_CTRL_FSM_STATE: VBUS control FSM states: - 0x0: (VBUS_OFF) VBUS_OFF state. - 0x1: (VBUS_IDLE) VBUS_IDLE state. - 0x2: (VBUS_CHANGE) VBUS_CHANGE state. - 0x3: (VBUS_UP_WAIT) VBUS_UP_WAIT state. - 0x4: (VBUS_UP_TRANS) VBUS_UP_TRANS state. - 0x5: (VBUS_DOWN_WAIT) VBUS_DOWN_WAIT state. - 0x6: (VBUS_DOWN_TRANS) VBUS_DOWN_TRANS state. - 0x7: (VBUS_RESTORE) VBUS_RESTORE state. - 0x8: (VBUS_HARDRESET) VBUS_HARDRESET state.
[3:0]	VBUS_FSM_STATE: VBUS monitoring FSM states: - 0x0: (VMON_OFF) VMON_OFF state. - 0x1: (VMON_STEADY) VMON_STEADY state. - 0x2: (VMON_TRANS_LOW) VMON_TRANS_LOW state. - 0x3: (VMON_TRANS_HIGH) VMON_TRANS_HIGH state. - 0x4: (VMON_HR) VMON_HR state. - 0x5: (VMON_DISCH) VMON_DISCH state. - 0x6: (VMON_CHECK_VBUS) VMON_CHECK_VBUS state. - 0x7: (VMON_TRANS_LOW_CHECK) VMON_TRANS_LOW_CHECK state. - 0x8: (VMON_FIRST_STEP_WAIT) VMON_FIRST_STEP_WAIT state. - 0x9: (VMON_PSRDY_DEBOUNCE) VMON_PSRDY_DEBOUNCE state. - 0xA: (VMON_UNATTACH) VMON_UNATTACH state. - 0xB: (VMON_DETACH) VMON_DETACH state. - 0xC: (VMON_HR_END) VMON_HR_END state. - 0xD: (VMON_GOTOERRORRECOVERY) VMON_GOTOERRORRECOVERY state.

2.33 MONITORING_DACH_STATUS

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VVAR_DACH [15:5]											Reserved				
R															

Address:	0x0023
Reset:	0x0000
[15:5]	VVAR_DACH: Image of the DACH bits [10:0] input code without the hardware compensation (trimming).

2.34 MONITORING_DACL_STATUS

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VVAR_DACL [15:5]											Reserved				
R															

Address:	0x0025
Reset:	0x0000
[15:5]	VVAR_DACL: Image of the DACL bits [10:0] input code without the hardware compensation (trimming).

2.35 CONNECTION_TRANS

7	6	5	4	3	2	1	0
Reserved					NVM_DOWNLOADED_AL	CC_STATUS_AL	ATTACH_STATUS_AL
					RC	RC	RC

Address:	0x0027
Reset:	0x00
[2]	NVM_DOWNLOADED_AL: NVM_DOWNLOADED alert: - 0x0: (NVM_DOWNLOADED_AL_CLR) alert cleared. - 0x1: (NVM_DOWNLOADED_AL_SET) alert set.
[1]	CC_STATUS_AL: CC_STATUS alert (transition occurred on bits [3:0] of CC_STATUS register): - 0x0: (CC_STATUS_AL_CLR) alert cleared. - 0x1: (CC_STATUS_AL_SET) alert set.
[0]	ATTACH_STATUS_AL: ATTACH_STATUS alert: - 0x0: (ATTACH_STATUS_AL_CLR) alert cleared. - 0x1: (ATTACH_STATUS_AL_SET) alert set.

2.36 CONNECTION_MASK

7	6	5	4	3	2	1	0
Reserved					NVM_DOWNLOADED_AL_MASK	CC_STATUS_AL_MASK	ATTACH_STATUS_AL_MASK
					RW	RW	RW

Address:	0x0028
Reset:	0xFF
[2]	NVM_DOWNLOADED_AL_MASK: NVM_DOWNLOADED_AL mask: - 0x0: (NVM_DOWNLOADED_AL_MASK_DIS) mask disabled. - 0x1: (NVM_DOWNLOADED_AL_MASK_EN) mask enabled. NVM_INIT parameter: FTP_NVM_DOWNLOADED_AL_MASK
[1]	CC_STATUS_AL_MASK: CC_STATUS_AL mask: - 0x0: (CC_STATUS_AL_MASK_DIS) mask disabled. - 0x1: (CC_STATUS_AL_MASK_EN) mask enabled. NVM_INIT parameter: FTP_CC_STATUS_AL_MASK
[0]	ATTACH_STATUS_AL_MASK: ATTACH_STATUS_AL mask: - 0x0: (ATTACH_STATUS_AL_MASK_DIS) mask disabled. - 0x1: (ATTACH_STATUS_AL_MASK_EN) mask enabled. NVM_INIT parameter: FTP_ATTACH_STATUS_AL_MASK

2.37 COMMAND

7	6	5	4	3	2	1	0
Reserved				CMD[3:0]			
				RW			

Address:	0x0031
Reset:	0x00
[3:0]	CMD: Software command : - 0x1: (TX_SEND_MSG) request the send of a message already present in the Tx buffer registers. - 0x2: (IGNORE_RX_MSG) ignore received message (Tx buffer discarded). - 0x9: (BYPASS_AMS) force Send message without checking TxOK.

2.38 RX_MSG_DETECT

7	6	5	4	3	2	1	0
Reserved	CABLE_RESET_RX_EN	HARD_RESET_RX_EN	SOP_DBG2_RX_EN	SOP_DBG1_RX_EN	SOP2_RX_EN	SOP1_RX_EN	SOP_RX_EN
	RW	RW	RW	RW	RW	RW	RW

Address:	0x0032
Reset:	0x21
[6]	CABLE_RESET_RX_EN: Cable Reset signaling detection. - 0x0: (CABLE_RESET_NOT_DET) PRT does not detect Cable Reset signaling (default). - 0x1: (CABLE_RESET_DET) PRT detects Cable Reset signaling.
[5]	HARD_RESET_RX_EN: HardReset signaling detection. - 0x0: (HARD_RESET_NOT_DET) PRT does not detect HardReset signaling. - 0x1: (HARD_RESET_DET) PRT detects HardReset signaling (default).
[4]	SOP_DBG2_RX_EN: SOP_DBG" message detection. - 0x0: (SOP_DBG2_NOT_DET) PRT does not detect SOP_DBG" message (default). - 0x1: (SOP_DBG2_DET) PRT detects SOP_DBG" message.
[3]	SOP_DBG1_RX_EN: SOP_DBG' message detection. - 0x0: (SOP_DBG1_NOT_DET) PRT does not detect SOP_DBG' message (default). - 0x1: (SOP_DBG1_DET) PRT detects SOP_DBG' message.
[2]	SOP2_RX_EN: SOP" message detection. - 0x0: (SOP2_NOT_DET) PRT does not detect SOP" message (default). - 0x1: (SOP2_DET) PRT detects SOP" message.
[1]	SOP1_RX_EN: SOP' message detection. - 0x0: (SOP1_NOT_DET) PRT does not detect SOP' message (default). - 0x1: (SOP1_DET) PRT detects SOP' message.
[0]	SOP_RX_EN: SOP message detection. - 0x0: (SOP_NOT_DET) PRT does not detect SOP message. - 0x1: (SOP_DET) PRT detects SOP message (default).

2.39 RESET_CTRL

7	6	5	4	3	2	1	0
Reserved						ERROR_RECOVERY_EN	Reserved
						RW	

Address:	0x0033
Reset:	0x00
[1]	ERROR_RECOVERY_EN: Error recovery forced: - 0x0: (ERRORRECOVERY_DIS) Error recovery is released. - 0x1: (ERRORRECOVERY_EN) Error recovery is forced.

2.40 VBUS_CTRL

7	6	5	4	3	2	1	0
Reserved						SINK_VBUS_EN	Reserved
						RW	

Address:	0x0034
Reset:	0x00
[1]	SINK_VBUS_EN: sink power switch control when VBUS_CTRL_SW = 1. - 0x0: (SINK_VBUS_EN_OPEN) force VBUS_EN_SNK switch open. - 0x1: (SINK_VBUS_EN_CLOSE) force VBUS_EN_SNK switch close.

2.41 MONITORING_CTRL

7	6	5	4	3	2	1	0
Reserved			CV_CL_MODE	Reserved	VBUS_HIGH_ENABLE	VBUS_LOW_ENABLE	VBUS_CTRL_LOW_MASK
			RW		RW	RW	RW

Address:	0x0035
Reset:	0x06
[4]	CV_CL_MODE: CV/CL mode: - 0x0: (CV_MODE) CV mode. - 0x1: (CL_MODE) CL mode.
[2]	VBUS_HIGH_ENABLE: Vbus high comparator enabled when register driven is selected (MONITORING_DACH_CTRL_0.COMPH_ENABLE_SEL field): - 0x0: (VBUSHIGH_COMP_DIS) Vbus high DAC + comparator is disabled. - 0x1: (VBUSHIGH_COMP_EN) Vbus high DAC + comparator is enabled.
[1]	VBUS_LOW_ENABLE: Vbus low comparator enable when register driven is selected (MONITORING_DACL_CTRL_0.COMPL_ENABLE_SEL field): - 0x0: (VBUSLOW_COMP_DIS) Vbus low DAC + comparator is disabled. - 0x1: (VBUSLOW_COMP_EN) Vbus low DAC + comparator is enabled.
[0]	VBUS_CTRL_LOW_MASK: vbus_low info is masked: - 0x0: (VBUSLOW_MASK_DIS) vbus_low info is not masked to vbus switch control. - 0x1: (VBUSLOW_MASK_EN) vbus_low info is masked to vbus switch control. NVM_INIT parameter: FTP_VBUS_CTRL_LOW_MASK

2.42 MONITORING_DACH_CTRL

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VVAR_DACH_SEL [15:5]										Reserved			DACH_INPUT_SEL		COMPH_ENABLE_SEL
RW													RW		RW

Address:	0x0036
Reset:	0x0000
[15:5]	VVAR_DACH_SEL: DACH bits [10:0] input code.
[1]	DACH_INPUT_SEL: DACH input selection: - 0x0: (DACH_IN_FROM_DIG) input from digital calculation (default). - 0x1: (DACH_IN_FROM_REG) input from register.
[0]	COMPH_ENABLE_SEL: Comparator + DAC high enable selection: - 0x0: (COMPH_EN_FROM_DIG) enable driven by digital (default). - 0x1: (COMPH_EN_FROM_REG) enable driven by register only.

2.43 MONITORING_DACL_CTRL

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VVAR_DACL_SEL [15:5]											Reserved			DACL_INPUT_SEL	COMPL_ENABLE_SEL
RW														RW	RW

Address:	0x0038
Reset:	0x0000
[15:5]	VVAR_DACL_SEL: DACL bits [10:0] input code.
[1]	DACL_INPUT_SEL: DACL input selection: - 0x0: (DACL_IN_FROM_DIG) input from digital calculation (default). - 0x1: (DACL_IN_FROM_REG) input from register.
[0]	COMPL_ENABLE_SEL: Comparator low enable selection: - 0x0: (COMPL_EN_FROM_DIG) enable driven by digital (Default). - 0x1: (COMPL_EN_FROM_REG) enable driven by register only.

2.44 MONITORING_SHIFT_CTRL

7	6	5	4	3	2	1	0
Reserved		SHIFT_H [5:4]		Reserved		SHIFT_L [1:0]	
		RW				RW	

Address:	0x003A
Reset:	0x00
[5:4]	SHIFT_H: Value of the shift to be added to the high threshold. - 0x0: (SHIFT_1_10) DACH * 1.10 (default). - 0x1: (SHIFT_1_15) DACH * 1.15. - 0x2: (SHIFT_1_20) DACH * 1.20. - 0x3: (RESERVED) Reserved. NVM_INIT parameter: FTP_SHIFT_H
[1:0]	SHIFT_L: Value of the shift to be added to the low threshold. - 0x0: (SHIFT_0_95) DACL * 0.95 (default). - 0x1: (SHIFT_0_90) DACL * 0.90. - 0x2: (SHIFT_0_85) DACL * 0.85. - 0x3: (SHIFT_1_00) DACL * 1.00. NVM_INIT parameter: FTP_SHIFT_L

2.45 VBUS_DISCHARGE_CTRL

7	6	5	4	3	2	1	0
Reserved					DISCH_CTRL_SEL	VBUS_VS_DISCH_EN	DISCH_EN
					RW	RW	RW

Address:	0x003B
Reset:	0x00
[2]	DISCH_CTRL_SEL: Discharge control selection: - 0x0: (DISCH_CTRL_FSM) Discharge is controlled by FSM. - 0x1: (DISCH_CTRL_REG) Discharge is controlled by registers.
[1]	VBUS_VS_DISCH_EN: VBUS discharge enable: - 0x0: (VBUS_DISCH_DIS) Disable the forced assertion of VBUS_VS_DISCH pin. - 0x1: (VBUS_DISCH_EN) Force the assertion of VBUS_VS_DISCH pin.
[0]	DISCH_EN: VSRC discharge enable: - 0x0: (DISCH_DIS) Disable the forced assertion of DISCH pin. - 0x1: (DISCH_EN) Force the assertion of DISCH pin.

2.46 VBUS_DISCHARGE_TIME_CTRL

7	6	5	4	3	2	1	0
DISCHARGE_TIME_TO_0V [7:3]					DISCHARGE_TIME_TRANSITION [2:0]		
RW					RW		

Address:	0x003C
Reset:	0x00
[7:3]	DISCHARGE_TIME_TO_0V: Discharge time from any contract to 0V - 665 ms is the default in standard by 35ms step, target is evaluated after each step. NVM_INIT parameter: FTP_DISCHARGE_TIME_TO_0V
[2:0]	DISCHARGE_TIME_TRANSITION: Discharge time from any contract to the next one - 280ms is the default in standard by 35ms step, target is evaluated after each step. Discharge cycle = field value + 3. NVM_INIT parameter: FTP_DISCHARGE_TIME_TRANSITION

2.47 DEVICE_CTRL

7	6	5	4	3	2	1	0
Reserved		VBUS_CTRL_SW	Reserved		WATCHDOG_EN	Reserved	
		RW			RW		

Address:	0x003D
Reset:	0xC0
[5]	VBUS_CTRL_SW: VBUS Switch enable: This bit is cleared on all detach event. - 0x0: (VBUS_CTRL_SW_DIS) VBUS Switch is managed by HW (Default). - 0x1: (VBUS_CTRL_SW_EN) VBUS Switch is managed by SW.
[2]	WATCHDOG_EN: watchdog function enable: - 0x0: (I2C_WDG_DIS) function disable (Default). - 0x1: (I2C_WDG_EN) function enable (2s watchdog timer starts as soon as Alert pin is asserted).

2.48 APPLI_CTRL

7	6	5	4	3	2	1	0
DRS_AUTO_ACCEPT	Reserved	PDO_0MA_MISMATCH	MISMATCH_5V	MISMATCH_PD	Reserved	OPERATING_CURRENT_SEL	ABOVE_5V
RW		RW	RW	RW		RW	RW

Address:	0x003E
Reset:	0xC0
[7]	DRS_AUTO_ACCEPT: Data role swap automatic accept: - 0x0: (DRS_AUTO_ACCEPT_DIS) Data role swap auto accept is disabled. - 0x1: (DRS_AUTO_ACCEPT_EN) Data role swap auto accept is enabled (default).
[5]	PDO_0MA_MISMATCH: - 0x0: (PDO_0MA_MISMATCH_DIS) No specific management of Vsink en path whatever requested current value. - 0x1: (PDO_0MA_MISMATCH_EN) Power path is Opened when source pdp offer is 0. NVM_INIT parameter: FTP_PDO_0MA_MISMATCH
[4]	MISMATCH_5V: - 0x0: (MISMATCH_5V_DIS) Power path is closed on TypeC. - 0x1: (MISMATCH_5V_EN) Power path is closed if Type C src current >= I PDO1. NVM_INIT parameter: FTP_MISMATCH_5V
[3]	MISMATCH_PD: - 0x0: (MISMATCH_PD_DIS) if current does not fit with PDO(n), check PDO(n-1) till PDO1. - 0x1: (MISMATCH_PD_EN) if current does not fit with PDO(n), make request with current in line with PDO(n) source and set mismatch bit. NVM_INIT parameter: FTP_MISMATCH_PD
[1]	OPERATING_CURRENT_SEL: - 0x0: (OP_CUR_SEL_DIS) Feature disabled - see datasheet for operating and max current fields in Request message. - 0x1: (OP_CUR_SEL_EN) Feature enabled - request message (RDO) will include in both operating current field (ie. bits 19 to 10) and maximum operating current field (i.e. bits 9 to 0) the source PDO current. NVM_INIT parameter: FTP_OPERATING_CURRENT_SEL
[0]	ABOVE_5V: - 0x0: (ABOVE_5V_DIS) Feature disabled. - 0x1: (ABOVE_5V_EN) Feature enabled - VBUS_EN_SNK activated only when PD explicit contract available using fix Sink PDO2 or fix Sink PDO3 or Sink Variable PDO or APDO PPS, when voltage requested is greater than 5V. NVM_INIT parameter: FTP_ABOVE_5V

2.49 DPM_CTRL

7	6	5	4	3	2	1	0
VCONN_EN	VCONN_SWAP_2_ON	VCONN_SWAP_2_OFF	DR_SWAP_2_UFP	DR_SWAP_2_DFP	BAT_PRES	BAT_SWP	VDM_SUPPORT
RW	RW	RW	RW	RW	RW	RW	RW

Address:	0x003F
Reset:	0x00
[7]	VCONN_EN: Vconn supply enable: - 0x0: (VCONN_DIS) the Vconn supply is disable. - 0x1: (VCONN_EN) the Vconn supply is enable. NVM_INIT parameter: FTP_VCONN_EN
[6]	VCONN_SWAP_2_ON: Vconn swap request to enable vconn: - 0x0: (VCONN_SWAP_2_ON_DIS) this Vconn swap is not supported. - 0x1: (VCONN_SWAP_2_ON_EN) this Vconn swap is supported. NVM_INIT parameter: FTP_VCONN_SWAP_2_ON
[5]	VCONN_SWAP_2_OFF: Vconn swap request to disable Vconn: - 0x0: (VCONN_SWAP_2_OFF_DIS) this Vconn swap is not supported. - 0x1: (VCONN_SWAP_2_OFF_EN) this Vconn swap is supported. NVM_INIT parameter: FTP_VCONN_SWAP_2_OFF
[4]	DR_SWAP_2_UFP: Data role swap request to UFP: - 0x0: (DR_SWAP_2_UFP_DIS) this data role swap is not supported. - 0x1: (DR_SWAP_2_UFP_EN) this data role swap is supported. NVM_INIT parameter: FTP_DR_SWAP_2_UFP
[3]	DR_SWAP_2_DFP: Data role swap request to DFP: - 0x0: (DR_SWAP_2_DFP_DIS) this data role swap is not supported. - 0x1: (DR_SWAP_2_DFP_EN) this data role swap is supported. NVM_INIT parameter: FTP_DR_SWAP_2_DFP
[2]	BAT_PRES: Battery in the application: - 0x0: (BAT_PRES_DIS) No Battery in application. - 0x1: (BAT_PRES_EN) Battery in application. NVM_INIT parameter: FTP_BAT_PRES
[1]	BAT_SWP: Battery swappable: - 0x0: (BAT_SWP_DIS) one fix Battery. - 0x1: (BAT_SWP_EN) one swappable Battery. NVM_INIT parameter: FTP_BAT_SWP
[0]	VDM_SUPPORT: VDM message support: - 0x0: (VDM_DIS) VDM message is not supported. - 0x1: (VDM_EN) VDM Message is supported.

	NVM_INIT parameter: FTP_VDM_SUPPORT
--	-------------------------------------

2.50 GPIO_CTRL

7	6	5	4	3	2	1	0
SW_GPOD		Reserved				POWER_OK [1:0]	
RW						RW	

Address:	0x0040
Reset:	0x00
[7]	SW_GPOD: GPOD pad value: - 0x0: (SW_GPOD_0) GPOD pad at 0. - 0x1: (SW_GPOD_1) GPOD pad at 1.
[1:0]	POWER_OK: SNK_PDO accepted in the power negotiation with the RDO calculated by MCU: - 0x0: (POWER_OK1) fix SNK PDO1 (5V). - 0x1: (POWER_OK2) fix SNK PDO2. - 0x2: (POWER_OK3) fix SNK PDO3. - 0x3: (POWER_OK4) variable or PPS SNK PDO.

2.51 NVM_CUST_CTRL

7	6	5	4	3	2	1	0
NVM_MODE	Reserved	NVM_CUST_SECT [5:4]		Reserved	NVM_CUST_OPCODE [2:0]		
RW		RW			RW		

Address:	0x0041
Reset:	0x00
[7]	NVM_MODE: Put the chip in NVM mode (bit writable only when device is unattached or PS READY): - 0x0: (MAIN_MODE) chip in main mode. - 0x1: (NVM_MODE) Chip in NVM mode.
[5:4]	NVM_CUST_SECT: Customer sectors: - 0x0: (CUST_SECT_0) customer sector 0. - 0x1: (CUST_SECT_1) customer sector 1. - 0x2: (CUST_SECT_2) customer sector 2. - 0x3: (CUST_SECT_3) customer sector 3.
[2:0]	NVM_CUST_OPCODE: Customer NVM operations: - 0x0: (NOP) No Operation. - 0x1: (READ_CUST) Read. - 0x2: (WRITE_CUST) Write. - 0x3: (WRITE_FUNC_REG) copy functional registers to NVM. - 0x4: (WRITE_2_FUNC_REG) copy NVM to the functional registers.

2.52 GPIO_SETTING

7	6	5	4	3	2	1	0
Reserved					GPIO_CONF [2:0]		
					R		

Address:	0x0050
Reset:	0x00
[2:0]	GPIO_CONF: - 0x0: (GPIO_CONF_0) GPIO conf 0. - 0x1: (GPIO_CONF_1) GPIO conf 1. - 0x2: (GPIO_CONF_2) GPIO conf 2. - 0x3: (GPIO_CONF_3) GPIO conf 3. - 0x4: (GPIO_CONF_4) GPIO conf 4. NVM_INIT parameter: FTP_GPIO_CONF

2.53 DEVICE_PDP

7	6	5	4	3	2	1	0
PDP[7:0]							
RW							

Address:	0x0051
Reset:	0x00
[7:0]	PDP: Device PDP in 0.5 watt. PDP[0] is ignored if PDP[7:1] > 10W. NVM_INIT parameter: FTP_PDP

2.54 NUM_PDO

7	6	5	4	3	2	1	0
Reserved	NUM_SRC_PDO [6:4]			Reserved		NUM_SNK_FIX_PDO [1:0]	
	R					RW	

Address:	0x0052
Reset:	0x00
[6:4]	NUM_SRC_PDO: Number of SRC PDO received by the device.
[1:0]	NUM_SNK_FIX_PDO: NUM_SNK_PDO defines the number of Sink fix PDOs. NVM_INIT parameter: FTP_NUM_SNK_FIX_PDO

2.55 SNK_PDO_PARAMS

7	6	5	4	3	2	1	0
VSAFE_5V_CURRENT [7:6]		PDO3_VSEL [5:4]		PDO2_VSEL [3:2]		PDO3_CURRENT	PDO2_CURRENT
RW		RW		RW		RW	RW

Address:	0x0053
Reset:	0x00
[7:6]	VSAFE_5V_CURRENT: Current at 5V: - 0x0: (VSAFE_5V_CURRENT_DEFAULT) PDP/5 is clamped at Default current. - 0x1: (VSAFE_5V_CURRENT_1A5) PDP/5 is clamped at 1.5 A. - 0x2: (VSAFE_5V_CURRENT_3A) PDP/5 is clamped at 3A. - 0x3: (VSAFE_5V_CURRENT_5A) PDP/5 is clamped at 5A. NVM_INIT parameter: FTP_VSAFE_5V_CURRENT
[5:4]	PDO3_VSEL: Fix Sink PDO3 VOLTAGE: - 0x0: (PDO3_VVAR) Vsel_Variable[9:0]. - 0x1: (PDO3_9V) 9V. - 0x2: (PDO3_15V) 15V. - 0x3: (PDO3_20V) 20V. NVM_INIT parameter: FTP_PDO3_VSEL
[3:2]	PDO2_VSEL: Fix Sink PDO2 VOLTAGE: - 0x0: (PDO2_VVAR) Vsel_Variable[9:0]. - 0x1: (PDO2_9V) 9V. - 0x2: (PDO2_15V) 15V. - 0x3: (PDO2_20V) 20V. NVM_INIT parameter: FTP_PDO2_VSEL
[1]	PDO3_CURRENT: Fix Sink PDO3 current: - 0x0: (PDO3_3A) PDP/PDO3 Clamped to 3 A. - 0x1: (PDO3_5A) PDP/PDO3 Clamped to 5 A. NVM_INIT parameter: FTP_PDO3_CURRENT
[0]	PDO2_CURRENT: Fix Sink PDO2 current: - 0x0: (PDO2_3A) PDP/PDO2 Clamped to 3A. - 0x1: (PDO2_5A) PDP/PDO2 Clamped to 5 A. NVM_INIT parameter: FTP_PDO2_CURRENT

2.56 SNK_PDO_CAPABILITIES

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VSEL_VARIABLE_HIGH [15:8]								VSEL_VARIABLE_LOW [7:6]		EPR_CAPABLE	DRD_CAPABLE	Reserved	USB_COM_CAPABLE	UNCONSTRAINED_POWER	HIGHER_CAPABILITY
										RW	RW		RW	RW	RW

Address:	0x0054
Reset:	0x0000
[15:8]	VSEL_VARIABLE_HIGH: VSEL_VARIABLE_HIGH voltage by 200mV step. NVM_INIT parameter: FTP_VSEL_VARIABLE_HIGH
[7:6]	VSEL_VARIABLE_LOW: VSEL_VARIABLE_LOW voltage by 50mV step. NVM_INIT parameter: FTP_VSEL_VARIABLE_LOW
[5]	EPR_CAPABLE: Information needed to fill b22 in request message. - 0x0: (SPR) SPR_capable. - 0x1: (EPR) EPR_capable.
[4]	DRD_CAPABLE: DRD capability. - 0x0: (SINGLE_DR) Single data role. - 0x1: (DUAL_DR) Dual role possible. NVM_INIT parameter: FTP_DRD_CAPABLE
[2]	USB_COM_CAPABLE: USB communication capability. - 0x0: (NO_USB_DATA) No USB data. - 0x1: (USB_DATA) USB data. NVM_INIT parameter: FTP_USB_COM_CAPABLE
[1]	UNCONSTRAINED_POWER: Unconstrained Power bit used in messaging. - 0x0: (UNCONST_POWER_CLR) not unconstrained power. - 0x1: (UNCONST_POWER_SET) unconstrained power. NVM_INIT parameter: FTP_UNCONSTRAINED_POWER
[0]	HIGHER_CAPABILITY: Higher capability. - 0x0: (FUNC_5V) full functionality achieved at Vsafe5V. - 0x1: (FUNC_HIGHER_5V) full functionality not achieved at Vsafe5V. NVM_INIT parameter: FTP_HIGHER_CAPABILITY

2.57 ALGO

7	6	5	4	3	2	1	0
SINK_FEATURE [7:6]		Reserved	PPS_PRIORITY	PPS_VOLTAGE_SELECTION [3:2]		Reserved	
RW			RW	RW			

Address:	0x0056
Reset:	0x00
[7:6]	SINK_FEATURE: Sink PDO types. - 0x0: (FIX_PDOS) only fix PDOs. - 0x1: (FIX_VAR_PDOS) Fix PDOs + Variable PDO. - 0x2: (FIX_PPS_PDOS) Fix PDOs + APDO_PPS. - 0x3: (FIX_VAR_PPS_PDOS) Fix PDOs +Variable PDO + PPS (Variable is inherited from PPS APDO). NVM_INIT parameter: FTP_SINK_FEATURE
[4]	PPS_PRIORITY: PPS is selected if matching range is found. - 0x0: (NO_PPS) no APDO PPS usage. - 0x1: (PPS_FIRST) APDO_PPS then PDP is maximized using VAR and/or fix. NVM_INIT parameter: FTP_PPS_PRIORITY
[3:2]	PPS_VOLTAGE_SELECTION: Voltage selected for PPS. - 0x0: (MIN_VOLTAGE) Min voltage. - 0x1: (MID_VOLTAGE) Mid voltage. - 0x2: (MAX_VOLTAGE) Max voltage. - 0x3: (SEL_VOLTAGE) SNK_PDO_CAPABILITIES[15:7] (VSEL_VARIABLE[9:1]). NVM_INIT parameter: FTP_AVS_PPS_VOLTAGE_SELECTION

2.58 SNK_APDO_FILL_1

7	6	5	4	3	2	1	0
MAX_VOLTAGE [7:0]							
RW							

Address:	0x0057
Reset:	0x00
[7:0]	MAX_VOLTAGE: maximum Voltage in 100mV increment. NVM_INIT parameter: FTP_MAX_VOLTAGE

2.59 SNK_APDO_FILL_2

7	6	5	4	3	2	1	0
MIN_VOLTAGE [7:0]							
RW							

Address:	0x0058
Reset:	0x00
[7:0]	MIN_VOLTAGE: minimum Voltage in 100mV increment. NVM_INIT parameter: FTP_MIN_VOLTAGE

2.60 SNK_APDO_FILL_3

7	6	5	4	3	2	1	0
Reserved	MAX_CURRENT [6:0]						
	RW						

Address:	0x0059
Reset:	0x00
[6:0]	MAX_CURRENT: Maximum current in 50mA increment. NVM_INIT parameter: FTP_MAX_CURRENT

2.61 DEVICE_SETTING

7	6	5	4	3	2	1	0
Reserved						DEV_SETTING [1:0]	
						R	

Address:	0x005A
Reset:	0x00
[1:0]	DEV_SETTING: HW configuration. - 0x1: (SNK_PD) Sink only PD.

2.62 REQUEST_SRC_PDP

7	6	5	4	3	2	1	0
Reserved		SINK_MAX_PDP [5:4]		SINK_OP_PDP [3:2]		SINK_MIN_PDP [1:0]	
		RW		RW		RW	

Address:	0x005C
Reset:	0x00
[5:4]	SINK_MAX_PDP: Sink Maximum PDP field value of the sink capabilities extended message. - 0x0: (SNK_MAX_DEVICE) Device PDP. - 0x1: (SNK_MAX_16W) 16W PDP. - 0x2: (SNK_MAX_28W) 28W PDP. - 0x3: (SNK_MAX_46W) 46W PDP. NVM_INIT parameter: FTP_SINK_MAX_PDP
[3:2]	SINK_OP_PDP: Sink Operational PDP field value of the sink capabilities extended message. - 0x0: (SNK_OP_DEVICE) Device PDP. - 0x1: (SNK_OP_16W) 16W PDP. - 0x2: (SNK_OP_28W) 28W PDP. - 0x3: (SNK_OP_46W) 46W PDP. NVM_INIT parameter: FTP_SINK_OP_PDP
[1:0]	SINK_MIN_PDP: Sink Minimum PDP field value of the sink capabilities extended message. - 0x0: (SNK_MIN_DEVICE) Device PDP. - 0x1: (SNK_MIN_16W) 16W PDP. - 0x2: (SNK_MIN_28W) 28W PDP. - 0x3: (SNK_MIN_46W) 46W PDP. NVM_INIT parameter: FTP_SINK_MIN_PDP

2.63 RX_BYTE_CNT

7	6	5	4	3	2	1	0
Reserved		RX_BYTE_COUNT [5:0]					
		R					

Address:	0x0060
Reset:	0x00
[5:0]	RX_BYTE_COUNT: numbers of byte in reception buffer including header.

2.64 RX_FRAME_TYPE

7	6	5	4	3	2	1	0
Reserved					RX_TYPE [2:0]		
					R		

Address:	0x0061
Reset:	0x00
[2:0]	RX_TYPE: RX_TYPE Received SOP* Message: - 0x0: (RX_SOP) Received SOP. - 0x1: (RX_SOP1) Received SOP'. - 0x2: (RX_SOP2) Received SOP". - 0x3: (RX_SOP_DBG1) Received SOP_DBG'. - 0x4: (RX_SOP_DBG2) Received SOP_DBG". - 0x6: (RX_CBL_RST) Received Cable Reset.

2.65 RX_HEADER

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_HEAD [15:0]															
R															

Address:	0x0062
Reset:	0x0000
[15:0]	RX_HEAD: Rx message header.

2.66 RX_DATA_OBJ_224BITS

7	6	5	4	3	2	1	0
RX_OBJ [7:0]							
R							

Address:	0x0064
Reset:	0x00
[7:0]	RX_OBJ : Rx data message of 224 bits length max.

2.67 PRT_TX_CTRL

7	6	5	4	3	2	1	0
Reserved		PRT_RETRY_MSG_CNT [5:4]		Reserved		PRT_TX_SOP_MSG [2:0]	
		RW				RW	

Address:	0x0080
Reset:	0x00
[5:4]	PRT_RETRY_MSG_CNT: Retry counter: - 0x0: (NO_RETRY) No message retry is required. - 0x1: (RETRY_1) Automatically retry message transmission once. - 0x2: (RETRY_2) Automatically retry message transmission twice. - 0x3: (RETRY_3) Automatically retry message transmission three times.
[2:0]	PRT_TX_SOP_MSG: Transmit SOP* message: - 0x0: (TX_SOP) Transmit SOP. - 0x1: (TX_SOP1) Transmit SOP'. - 0x2: (TX_SOP2) Transmit SOP". - 0x3: (TX_SOP_DBG1) Transmit SOP_DBG'. - 0x4: (TX_SOP_DBG2) Transmit SOP_DBG". - 0x5: (TX_HARD_RST) Transmit Hard Reset. - 0x6: (TX_CBL_RST) Transmit Cable Reset.

2.68 TX_BYTE_CNT

7	6	5	4	3	2	1	0
TX_BYTE_COUNT [7:0]							
RW							

Address:	0x0081
Reset:	0x00
[7:0]	TX_BYTE_COUNT: numbers of byte in transmission buffer including header.

2.69 TX_HEADER

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX_HEAD [15:0]															
RW															

Address:	0x0082
Reset:	0x0000
[15:0]	TX_HEAD: Tx message header.

2.70 TX_DATA_OBJ_224BITS

7	6	5	4	3	2	1	0
TX_OBJ [7:0]							
RW							

Address:	0x0084
Reset:	0x00
[7:0]	TX_OBJ : Tx data message of 224 bits length max.

2.71 DPM_SRC_PDO1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SRC_PDO1 [31:0]																															
RW																															

Address:	0x00A0
Reset:	0x0001 9000
[31:0]	SRC_PDO1: Source Power Data Object 1.

2.72 DPM_SRC_PDO2

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SRC_PDO2 [31:0]																															
RW																															

Address:	0x00A4
Reset:	0x00000000
[31:0]	SRC_PDO2: Source Power Data Object 2.

2.73 DPM_SRC_PDO3

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SRC_PDO3 [31:0]																															
R																															

Address:	0x00A8
Reset:	0x00000000
[31:0]	SRC_PDO3: Source Power Data Object 3.

2.74 DPM_SRC_PDO4

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SRC_PDO4 [31:0]																															
R																															

Address:	0x00AC
Reset:	0x00000000
[31:0]	SRC_PDO4: Source Power Data Object 4.

2.75 DPM_SRC_PDO5

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SRC_PDO5 [31:0]																															
R																															

Address:	0x00B0
Reset:	0x00000000
[31:0]	SRC_PDO5: Source Power Data Object 5.

2.76 DPM_SRC_PDO6

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SRC_PDO6 [31:0]																															
R																															

Address:	0x00B4
Reset:	0x00000000
[31:0]	SRC_PDO6: Source Power Data Object 6.

2.77 DPM_SRC_PDO7

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SRC_PDO7 [31:0]																															
R																															

Address:	0x00B8
Reset:	0x00000000
[31:0]	SRC_PDO7 : Source Power Data Object 7.

2.78 DPM_RDO

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDO[31:0]																															
R																															

Address:	0x00BC
Reset:	0x1000 0000
[31:0]	RDO: RDO registered when request is accepted.

2.79 DPM_ALGO_RESULT

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ALGO_RESULT [31:0]																															
R																															

Address:	0x00C0
Reset:	0x00000000
[31:0]	ALGO_RESULT: RDO registered when PDO algo end.

2.80 DPM_SRC_PDO_NEGOCIATED

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SRC_PDO_NEGOCIATED [31:0]																															
R																															

Address:	0x00C4
Reset:	0x0001 9000
[31:0]	SRC_PDO_NEGOCIATED: Source Power Data Object relative to the DPM_RDO.

3 References

- STUSB4531 datasheet
- USB Power Delivery specification: <https://www.usb.org/document-library/usb-power-delivery>
- USB Type-C cable and connector specification: <https://www.usb.org/document-library/usb-type-cr-cable-and-connector-specification-release-24>

Revision history

Table 3. Document revision history

Date	Version	Changes
07-Jan-2026	1	Initial release.

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