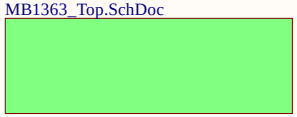
Nucleo144 H7 SMPS with STLINK V3

MB1363

H7A3ZIQ

Table of contents

U_MB1363_Top
MB1363_Top.SchDoc



Legend

General comment such as function title, configuration, ...

Text to be added to silkscreen.

Warning text.

Notes to generate the board layout.

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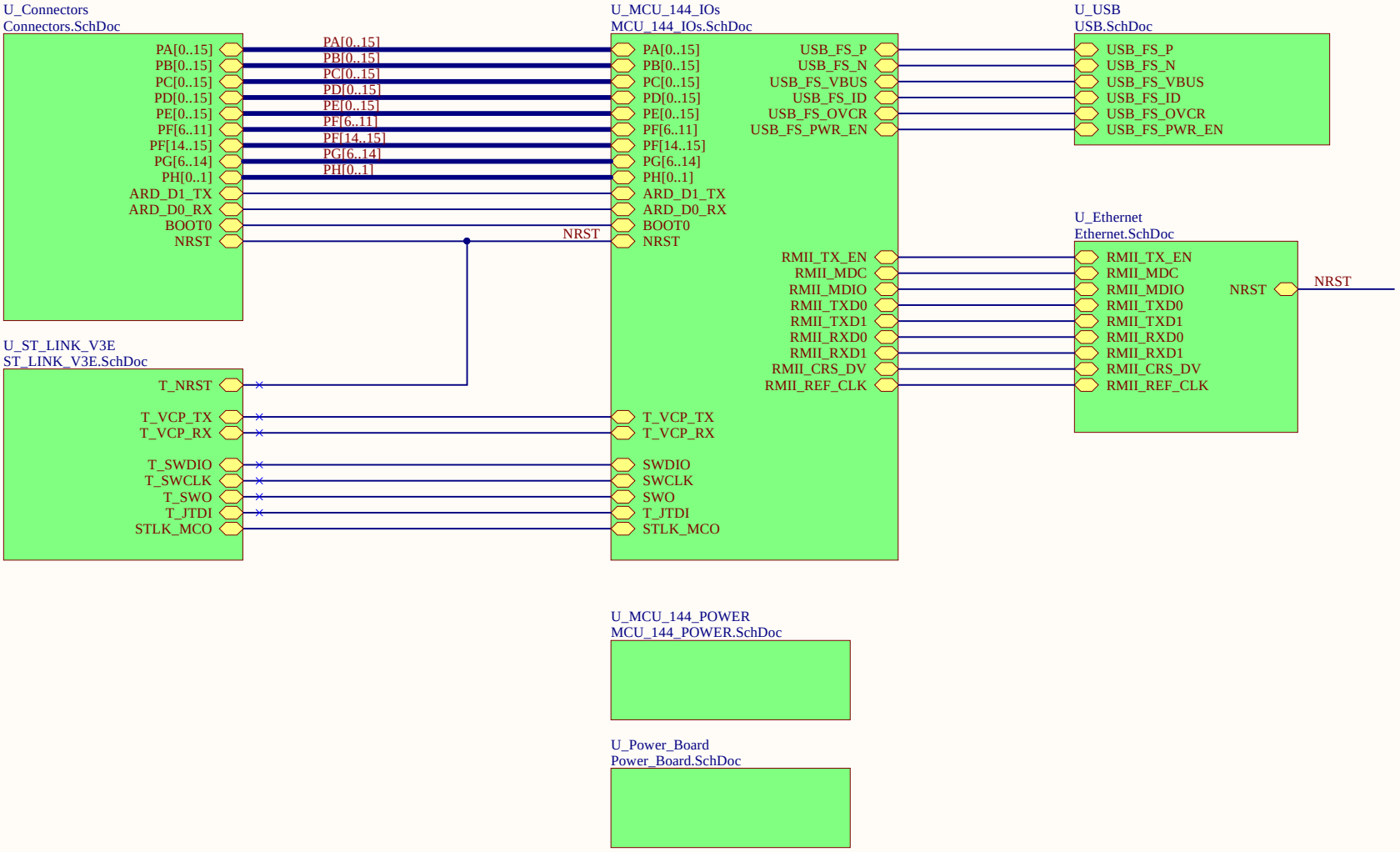
Title: **Project overview**		
Project: **Nucleo144 H7 SMPS with STLINK V3**		
Variant: H7A3ZIQ		
Revision: D-01		Reference: MB1363
Size: A4	Date: 24-OCT-19	Sheet: 1 of 9

life.augmented



Title: **MB1363 Top: hierarchical view**		
Project: **Nucleo144 H7 SMPS with STLINK V3**		
Variant: H7A3ZIQ		
Revision: D-01		Reference: MB1363
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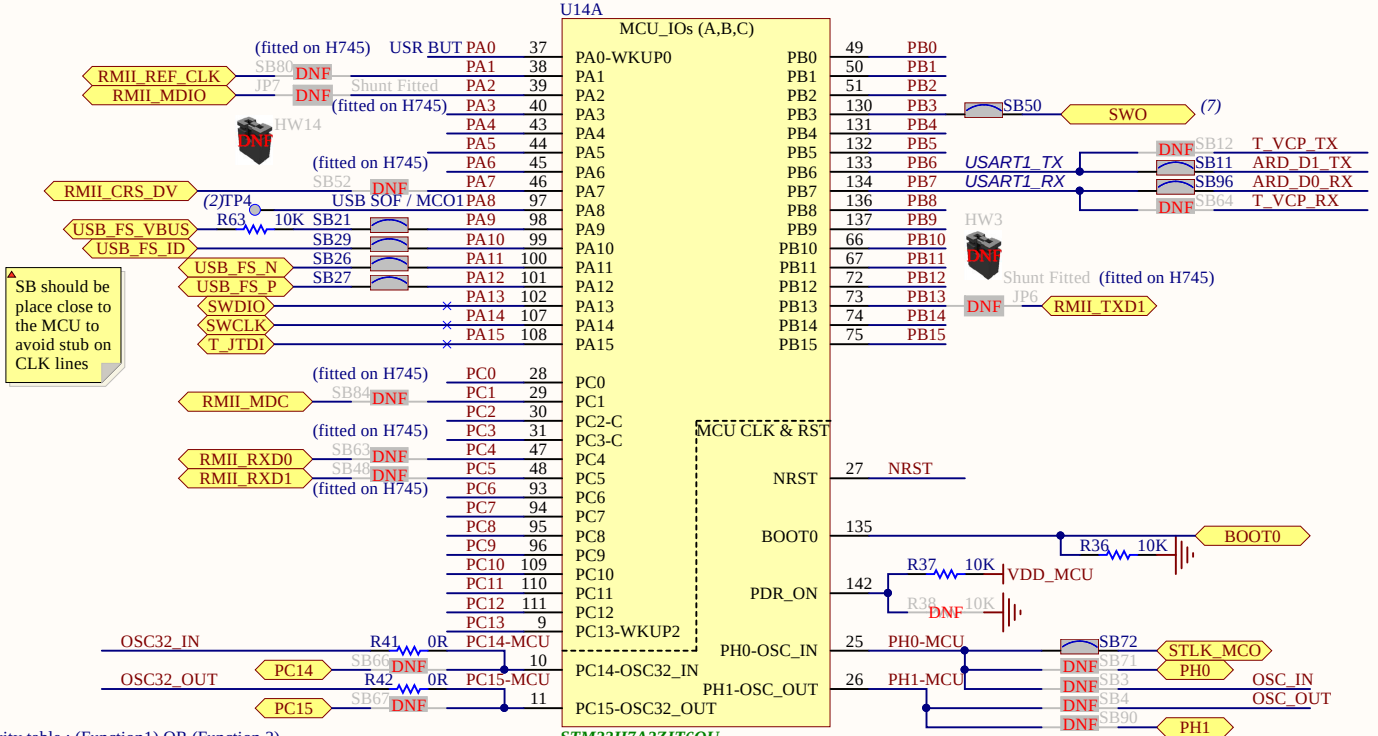
MCU IO CLK and RST

U14A

MCU_IOs (A,B,C)



SB should be place close to the MCU to avoid stub on CLK lines

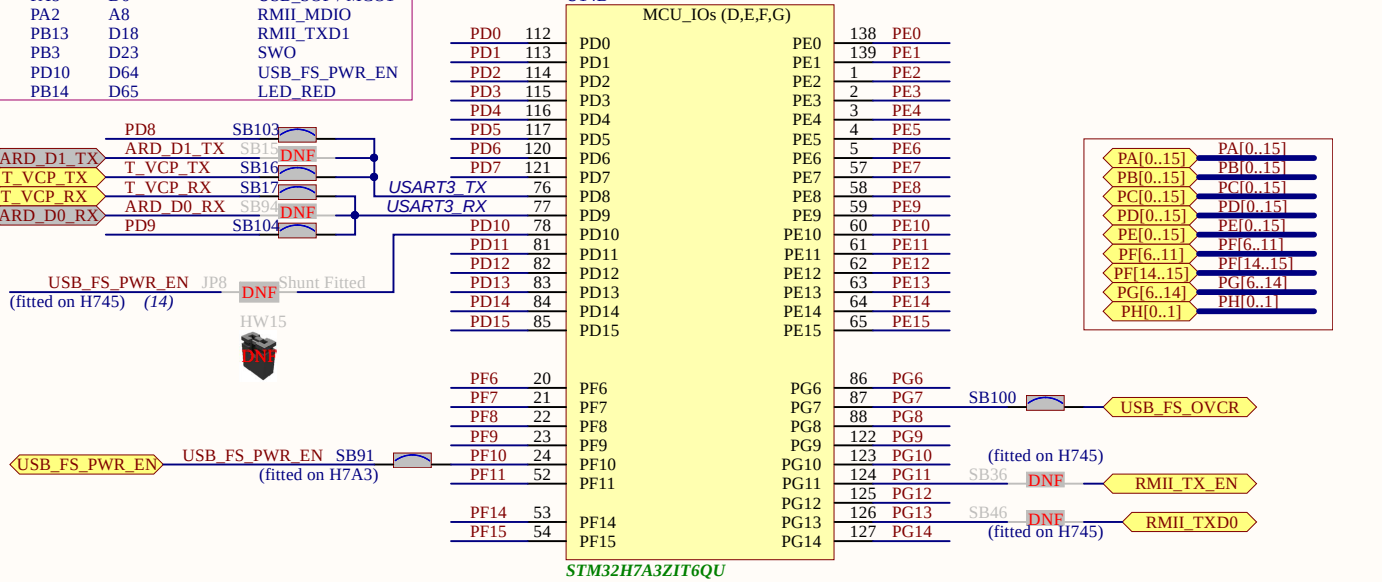
STM32H7A3ZIT6QU

Exlusivity table : (Function1) OR (Function 2)

I/O		ARDUINO / ZIO	OTHER
(2)	PA8	D6	USB_SOF / MCO1
(5)	PA2	A8	RMII_MDIO
(6)	PB13	D18	RMII_TXD1
(7)	PB3	D23	SWO
(14)	PD10	D64	USB_FS_PWR_EN
(15)	PB14	D65	LED_RED

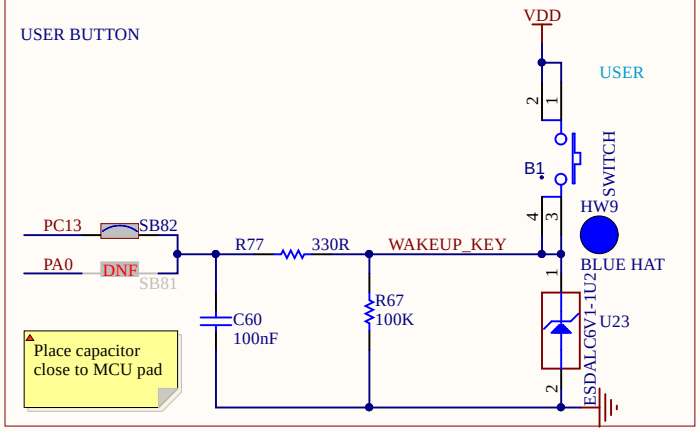
U14B

MCU_IOs (D,E,F,G)

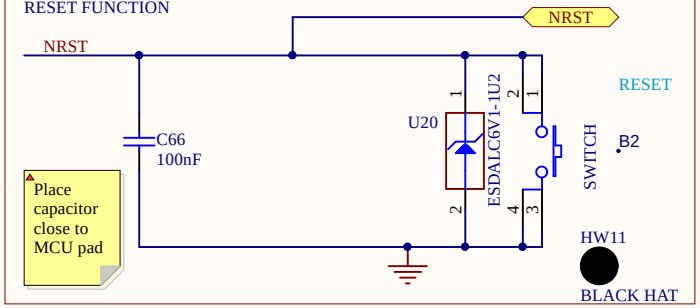


STM32H7A3ZIT6QU

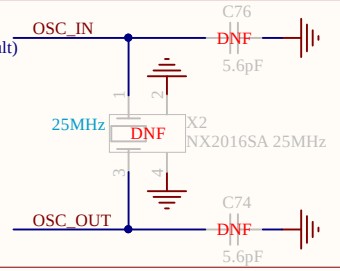
USER BUTTON



RESET FUNCTION

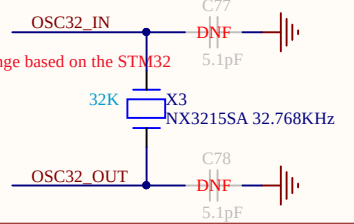


EXTERNAL HSE CLK
(OPTIONAL : not fitted by default)



EXTERNAL LSE CLK

C77 and C78 value can change based on the STM32



Title: **MCU 144 I/Os**		
Project: **Nucleo144 H7 SMPS with STLINK V3**		
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MCU PWR SUPPLIES

IDD Measurement
VDD — IDD — JP4 — VDD_MCU
Shunt Fitted
HW12

U14C
MCU_PWR

VDD_MCU	71	VDD_1	
	106	VDD_2	
	13	VDD_3	
	19	VDD_4	
	32	VDD_5	
	42	VDD_7	
	56	VDD_10	
	79	VDD_15	
	129	VDD_27	
	144	VDD_29	
	92	VDD_30	
	7	VDD_33	
		VSS_1	69
		VSS_2	104
		VSS_3	12
		VSS_4	18
		VSS_5	33
		VSS_7	41
		VSS_10	55
		VSS_13	141
		VSS_15	80
		VSS_24	118
		VSS_27	128
		VSS_30	89
		VSS_33	6
VDD_SMPS_IN	16	VDDSD	
VDD_SMPS_OUT	15	VLXSD	
VFBSD	17	VFBSD	
		VSSSD	14
VCAP	68	VCAP1	
	103	VCAP2	
	140	VCAP3	
VDD_LDO	70	VDDLDO_1	
	105	VDDLDO_2	
	143	VDDLDO_3	
3V3 — SB18	90	VDD50_USB	
3V3 — SB19	91	VDD33_USB_1	
VDD_MCU — SB32	119	VDD_MMC_1	
		VSSA	34
	36	VDDA	
VREFP	35	VREFP	
VDD_MCU — SB83	8	VBAT	

VBAT
SB68
AGND
STM32H7A3ZIT6QU

VDD_MCU — R40 0R — VDDA
DNF C62 100nF — DNF C61 100nF
R39 0R

SMPS MCU Supply Config

Supply Config 1 : LDO only (SMPS OFF, LDO ON)

Disconnect 3V3_SMPS_IN from 3V3_MCU
Connect 3V3_SMPS_IN to GND
Connect VDD_SMPS_IND_OUT to GND
Connect VDD_LDO to 3V3_MCU
2 x 2.2uF near VCAP plans/pins

VDD_MCU — SB25 DNF — VDD_LDO
VFBSD — R33 DNF 0R
VDD_SMPS_IN — SB74 DNF

2x2.2uF instead of 2x100nF near VCAP pins / plan

Supply Config 2 : Internal SMPS only (SMPS ON, LDO OFF)

Default config

Connect VDD_SMPS_IN to VDD_MCU
Connect VDD_SMPS_IND_OUT to VCAP1/2/3

VCAP — R35 0R — VFBSD

VDD_MCU — SB92 — VDD_SMPS_IN
Cin near VDDSD pin
Cin — C68 10uF — C65 10uF — VSSSD

VDD_SMPS_OUT — L1 2.2uH, 1.2A *L* — VDD_SMPS_IND_OUT — SB79 — 1V2_MCU — SB75 — VCAP
C64 220pF *Cfilt*
Cfilt & L near VLXSD
C75 10uF *Cout*
COUT near L
near VCAP pins / plan
C58 100nF — C54 100nF

1V2_MCU — SB76 — VDD_LDO

Supply Config 3 : SMPS & LDO cascaded (SMPS & LDO ON)

Compared to config 2 :
Disconnect VDD_SMPS_IND_OUT from VCAP
Connect VDD_SMPS_IND_OUT to VDD_LDO
Add 2x100nF near VDDLDO pins/plans
Add 2x2.2uF near VCAP pins/plans (see config 1)

VDD_LDO — R34 DNF 0R — VFBSD
2x100nF near VDDLDO pins / plan
VDD_LDO — C51 100nF — C53 100nF

Supply Config 5 : external SMPS

Disconnect 1V2_MCU from VDD_SMPS_IND_OUT
Connect 1V2_MCU to 1V2_VOUTCORE (Connectors page)

MCU DECAPS

Ceramic capacitor (Low ESR, ESR<1ohm)

capa near balls

VDD_MCU — C67 4.7uF C0603 — C59 100nF — C52 100nF — C55 100nF — C49 100nF — C47 100nF — C46 100nF — C56 100nF — C57 100nF — C50 100nF — C48 100nF

VBAT — C63 1uF

VDDA — C72 1uF — C73 100nF — AGND
VREFP — C69 1uF — C71 100nF — AGND

SB61 — AGND

Title: **MCU 144 POWER**		
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EXTENSION CONNECTORS, MCU INTERFACES

MORPHO CONNECTOR LEFT SIDE

Put the IO in BOTTOM side

CN11 — Header 35x2 (DNF)

	PC10	PC11	
	PC12	PD2	
VDD	BOOT0	5V_EXT	
	PF6		
	PF7	IOREF	
	PA13	NRST	
	PA14	3V3	
	PA15	5V	
	PB7		
	PC13	VIN	
	PC14		
	PC15	PA0	
	PH0	PA1	
	PH1	PA4	
		PB0	
VBAT	PC2	PC1	
	PC3	PC0	
	PD4	PD3	
	PD5		
	PD6		
	PD7	PE2	
	PE3	PE4	
		PE5	
		PF8	
	PD1	PF9	
	PD0		
	PE1	PE6	
	PG9		
	PG12	PG10	
		PG13	
	PD9	PG11	

CN16 — GND — HW1

Top buses

IOREF, 3V3 (SB24 DNF), VDD (SB14)

PA[0..15], PB[0..15], PC[0..15], PD[0..15], PE[0..15], PF[0..11], PF[6..11], PF[14..15], PG[6..14], PH[0..1]

NRST, BOOT0

Exlusivity table : (Function1) OR (Function 2)

I/O	ARDUINO / ZIO	OTHER
(1)	PB5	D11 / D22 / D70
(2)	PA8	D6
(3)	PG12	D7
(4)	PG9	D8
(5)	PA2	A8
(6)	PB13	D18
(7)	PB3	D23
(8)	PB2	D27 / D72
(9)	PE2	D31 / D56
(10)	PC9	D44
(11)	PG10	D49
(12)	PG8	D50
(13)	PE6	D59 / D38
(14)	PD10	D64
(15)	PB14	D65

ZIO CONNECTOR ARDUINO UNO COMPATIBLE

Arduino Uno compatible

CN8 — Socket 8x2_N144_ARD

	NC	SDMMC_C8	D43	SDMMC_D0		
IOREF	IOREF	SDMMC_C9	D44	SDMMC_D1/SAI2_EXTCLK (10)		
NRST	NRST	SDMMC_C10	D45	SDMMC_D2		
3V3	3V3	SDMMC_C11	D46	SDMMC_D3		
5V	5V	SDMMC_C12	D47	SDMMC_CK		
GND	GND	SDMMC_D2	D48	SDMMC_CMD		
GND	GND	IO	D49	SB30	PG10	(11)
VIN	VIN	IO	D50	SB31	PG8	(12)

Arduino Uno compatible

CN7 — Socket 10x2_N144_ARD

I2S_A_MCK	D16	PC6	I2S_A	D15 SCL		PB8	I2C_A_SCL	
I2S_A_SD	D17	PB15	I2S_A	D14 SDA		PB9	I2C_A_SDA	
(6)(fitted on H7A3) I2S_A_CK	D18	PB13	SB8	I2S_A	VREFP			
I2S_A_WS	D19	PB12	I2S_A	GND				
I2S_B_WS	D20	PA15	I2S_B	D13 SCK		PA5	SPI_A_SCK	
I2S_B_MCK	D21	PC7	I2S_B	D12 MISO		PA6	SPI_A_MISO	
(1) I2S_B_SD/SPI_B_MOSI	D22	PB5	SB53 SPI_B	I2S_B	D11 MOSI/PWM		SPI_A_MOSI/TIM_E_PWM1	(1)
(7) I2S_B_CK/SPI_B_SCK	D23	PB3	SB49 SPI_B	I2S_B	D10 CS/PWM	PD14	SPI_A_CS/TIM_B_PWM3	
SPI_B_NSS	D24	PA4	SPI_B	D9 PWM		PD15	TIMER_B_PWM2	
SPI_B_MISO	D25	PB4	SPI_B	D8	SB41	PG9	(4)	
					DNF SB57	PB5	(fitted on H745)	
					SB56	PA7	(fitted on H7A3)	

VREFP, C70 100nF, SB60, AGND

CN9 — Socket 15x2_N144_ARD

A0	PA3	A0	USART	PD7	D51	USART_B_SCLK
A1	PC0	A1	USART	PD6	D52	USART_B_RX
A2	PC3	A2	USART	PD5	D53	USART_B_TX
A3	PB1	A3	USART	PD4	D54	USART_B_RTS
A4 PC2	SB69	A4 D14 SDA	USART	PD3	D55	USART_B_CTS
A5 PF11	SB40	A5 D15 SCL	GND			
I2C_A_SDA D14	PB9 DNF SB62					
I2C_A_SCL D15	PB8 DNF SB39					
(8) COMP1_INP D72	PB2 DNF SB44	COMP	SAI_A	SB88	PE2	D56 SAI_A_MCLK (9)
COMP2_INP D71	PE9	COMP	SAI_A	PE4	D57	SAI_A_FS
(1) I2C_B_SMBA D70	PB5 DNF SB55	I2C_B	SAI_A	PE5	D58	SAI_A_SCK
I2C_B_SCL D69	PF14	I2C_B	SAI_A	SB86	PE6	D59 SAI_A_SD(13)
I2C_B_SDA D68	PF15	I2C_B	SAI_B	PE3	D60	SAI_B_SD
		GND	SAI_B	PF8	D61	SAI_B_SCK
CAN_RX D67	PD0	CAN	SAI_B	PF7	D62	SAI_B_MCLK
CAN_TX D66	PD1	CAN	SAI_B	PF9	D63	SAI_B_FS
(15) IO D65	PB14	IO	IO	SB99	PD10	D64 IO (14)
					(fitted on H7A3)	

(fitted on H745) A6 PF6 DNF SB73
(fitted on H7A3) A6 PC1 SB70
(fitted on H745) A7 PF10 DNF SB93
(fitted on H7A3) A7 PC5 SB58
(5) A8 PA2 SB78 (fitted on H7A3)

AGND, VDDA

CN10 — Socket 17x2_N144_ARD

AVDD		D7		SB45	PG12	(3)
AGND		D6 PWM	PE11	SB28	PA8	TIMER_A_PWM1 (2)
GND		D5 PWM	PE14			TIMER_A_PWM2
ADC_A_IN A6	ADC	D4	PE13			TIMER_A_PWM3
ADC_B_IN A7	ADC	D3 PWM	PG14			
ADC_C_IN A8	ADC	D2	PB6	LPUART1_TX		ARD_D1_TX
QSPI_CS D26	PG6 QSPI	D1 TX	PB7	LPUART1_RX		ARD_D0_RX
(8) QSPI_CLK D27	PB2 SB51 QSPI	D0 RX				
	GND	PWM	PE8	D42	TIMER_A_PWM1N	
QSPI_BK1_IO3 D28	PD13 QSPI	TIMER	PE7	D41	TIMER_A_ETR	
QSPI_BK1_IO1 D29	PD12 QSPI	GND				
QSPI_BK1_IO0 D30	PD11 QSPI	PWM	PE10	D40	TIMER_A_PWM2N	
(9) QSPI_BK1_IO2 D31 PE2	SB87 QSPI	PWM	PE12	D39	TIMER_A_PWM3N	
	GND	TIMER	SB85	PE6	D38 TIMER_A_BKIN2 (13)	
TIMER_C_PWM1 D32 PA0	SB89 PWM	TIMER	PE15	D37	TIMER_A_BKIN1	
TIMER_D_PWM1 D33	PB0 PWM	PWM	PB10	D36	TIMER_C_PWM2	
TIMER_B_ETR D34	PE0 TIMER	PWM	PB11	D35	TIMER_C_PWM3	

EXTERNAL SMPS SELECTION

CN6 — Jumper_Header_4x2

(12) PG8	SB34	SMPS_V1	3V3		
(4) PG9	SB35	SMPS_EN	VOUTVDD		
(11) PG10	SB33	SMPS_SW	DNF	1V2_VOUTCORE	1V2_MCU
(3) PG12	SB42	SMPS_PG		SB95 DNF	

USER LED 1 : ARD_D13_LED

Curr=5mA, Lum=25%

D13 PA5 SB65 DNF — PB0 SB54 — R76 47K — R71 100K — Q1 NPN SOT23 — LD1 GREEN — R28 270R — 3V3

USER LED 2

Curr=3mA, Lum=26%

PE1 — R74 47K — R72 100K — Q2 NPN SOT23 — LD2 YELLOW — R27 470R — 3V3

USER LED 3

Curr=4mA, Lum=25%

(15) PB14 — R75 47K — R73 100K — Q3 NPN SOT23 — LD3 RED — R26 360R — 3V3

MORPHO CONNECTOR RIGHT SIDE

FOR X-NUCLEO-IHMXXM1 MOTOR CTRL COMPATIBILITY

(USB)	PA11	SB22 DNF		MORPH_R_14
(BKIN2)	PE6	SB10 DNF		
	PB14	SB37		MORPH_R_28
(BKIN1)	PE15	SB38 DNF		
	PB5	SB59		MORPH_R_29
(DAC)	PA4	SB77 DNF		
	PB13	SB43		MORPH_R_30
(TIM1_CH1N)	PE8	SB47 DNF		
(USB)	PA12	SB23 DNF		MORPH_R_12

Put the IO in BOTTOM side

SBxx to avoid stub of SDMMC & USB signals

CN12 — Header 35x2 (DNF)

PC9	DNF SB9	SB20	DNF	PC8
	PB8	PC6		
	PB9	PC5		5V_USB_STLK
		PD8		
	PA5	MORPH_R_12		
	PA6	MORPH_R_14		
	PA7	PB12		
	PB6	PB11		
	PC7			
	PA9	PB2		
	PA8	PB1		
	PB10	PB15		
	PB4	MORPH_R_28		
MORPH_R_29		MORPH_R_30		
	PB3			AGND
	PA10	PC4		
	PA2			
	PA3			
		PE8		
	PD13	PF10		
	PD12	PE7		
	PD11	PD14		
	PE10	PD15		
	PE12	PF14		
	PE14	PE9		
	PE15			
	PE13	PE11		
		PF15		
PG14		PF11		
		PE0		
	PD10	PG8		
	PG7			
		PG6		

CN15 — GND — HW2

Title:	**Connectors**
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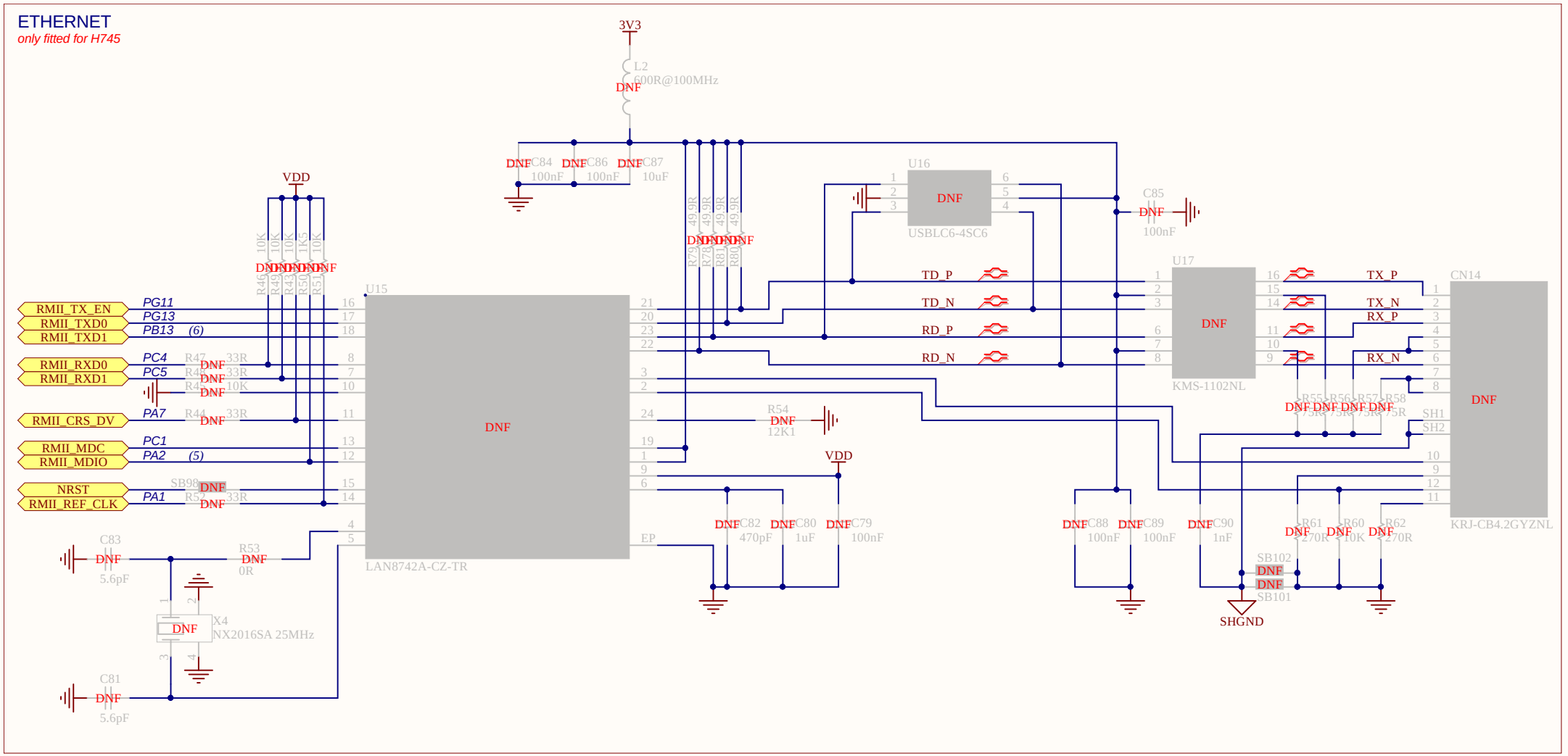

Title: **Ethernet PHY with RJ45 connector**		
Project: **Nucleo144 H7 SMPS with STLINK V3**		
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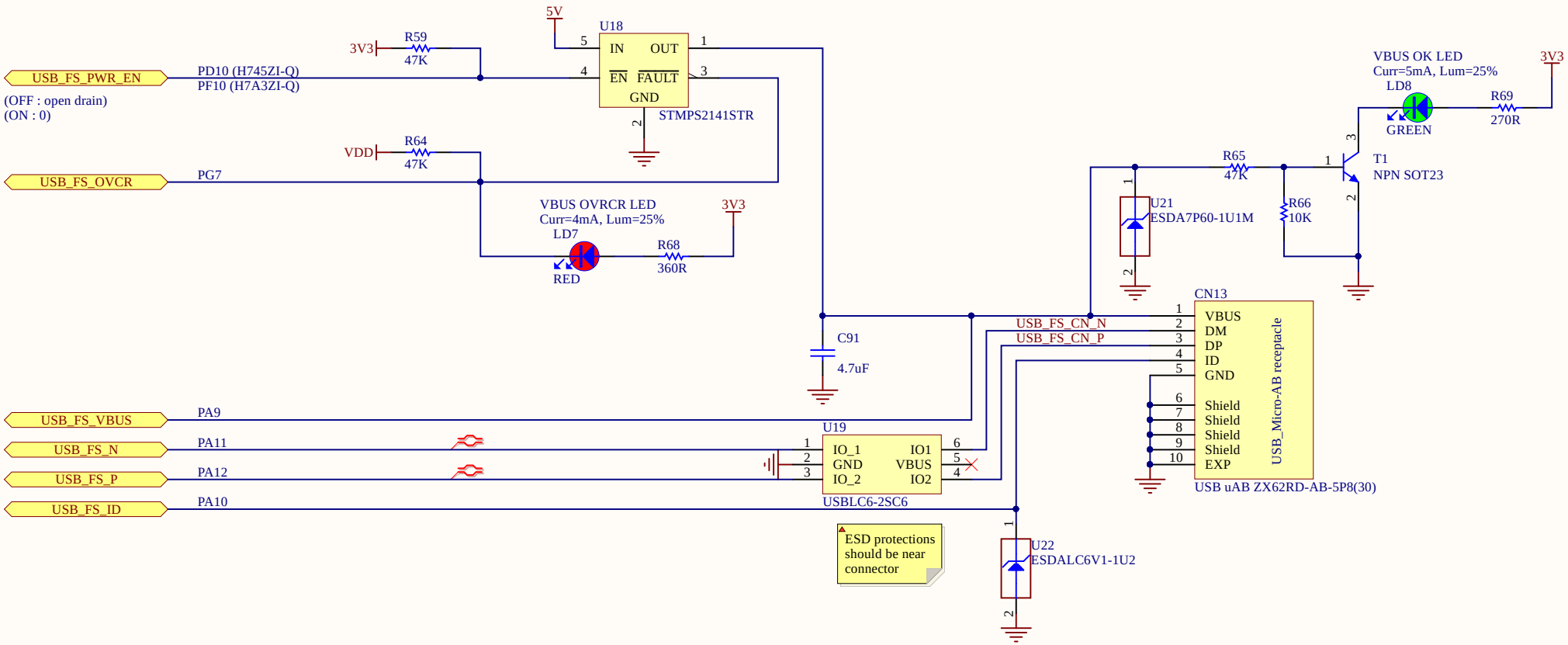
USB FS



Title: **USB**		
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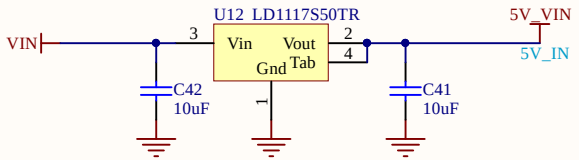
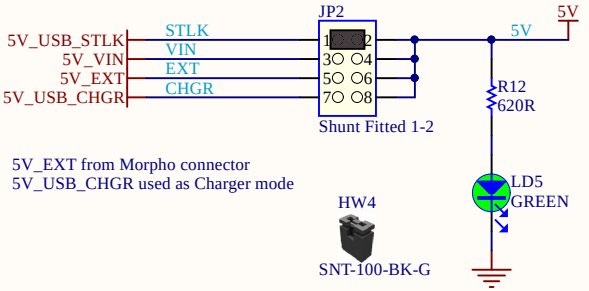
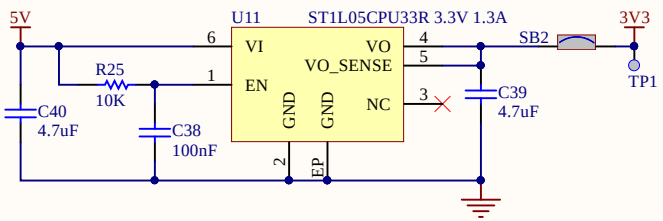
VIN / 5V PWR



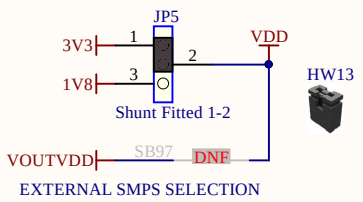
5V PWR SELECTION



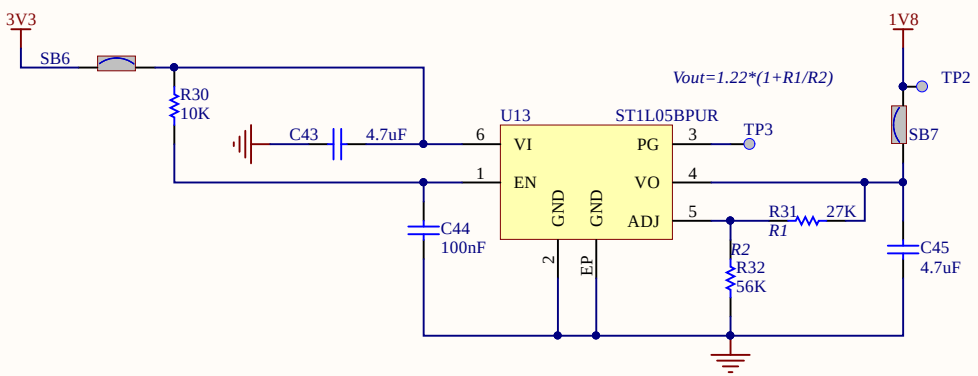
3V3 PWR



3V3/1V8 SELECTION



1V8 PWR



Title: **MAIN POWER 5V / 3V3 / 1V8**		
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STLINK_MCU

DFU CONNECTOR

CN2

Header 4x1

DNF

Connector must be on the border of the PCB

The routing of the tracks must be done on continuity from ST-LINK to 47ohm resistors and from resistors to Target MCU to avoid stub noises and EMC approach. (47ohm resistors must be very close to STDC14)

3V3_STLK

U7A

STLK_SWDIO A15

STLK_SWCLK A14

USB_DEV_HS_N R14

USB_DEV_HS_P R15

G1 H1

J1

D6

C6

J14 J15

STLK_SWDIO/PA13

STLK_SWCLK/PA14

USB_DEV_HS_N/PB14

USB_DEV_HS_P/PB15

OSC_IN/PH0

OSC_OUT/PH1

NRST

BOOT0

PDR_ON

V12_OTGPHY

REXT_OTGPHY

T_SW_DIR/PA7 R3

T_SWDIO_IN/PH7 N12 T_SWDIO_IN level shifter 1V8/3V3

T_SWDIOa/PF9 L2 T_SWDIOa level shifter 1V8/3V3

T_SWCLK/PH6 M11 T_SWCLKa

T_SWO/PD2 D12 T_SWOa level shifter 1V8/3V3

STLK_VCP_RX/PG9 C10 STLK_VCP_RX level shifter 1V8/3V3

STLK_VCP_TX/PG14 A7 STLK_VCP_TX

GNDDetect/PG5 K13 GNDDetect

T_VCC AIN/PA0 N3

T_PWR_EXT/PB1 R4 T_PWR_EXT

T_PWR_EN/PB0 R5 T_PWR_EN

STLK_LED/PA10 D15 LED_STLK

STLK_MCO/PA8 F15

T_NRST/PA6 P3 T_NRSTa

HW_TYP_0/PI4 D4

HW_TYP_1/PI5 C4

R11 47R T_SWCLK T_SWCLK

R23 47R T_VCP_RX T_VCP_RX

R20 4K7 R18 4K7 VDD

R15 2K7 R14 4K7 5V

R5 100R C5 20pF STLK_MCO STLK_MCO

R29 47R JP3 Shunt Fitted T_NRST T_NRST

HW6

HSE CLK STLINK

3V3_STLK

X1 VDD OUT EN GND

NZ2520SH 25MHz

R24 10K

R21 100R

C37 100nF

JP1 Shunt not fitted

NRST

C28 100nF

C7 2.2uF R6 3K

ST-LINK POWER

3V3_STLK

U7B

VDD VSS VDDA VREF+ VBAT BYPASS-REG VCAP1 VCAP2

R22 10K

C13 2.2uF C12 2.2uF

ST-LINKV3E_SWD

STDC14 Receiver

CN5

VDD KEY GNDDetect T_VCP_RX

T_SWDIO T_SWCLK T_SWO T_JTDI T_NRST T_VCP_TX

R17 100R

MIPI10 on STDC14 footprint

Specific constraints for T_SWDIO and T_SWCLK (must be same length and must be Shielded).

ESD PROTECTIONS

U4 STLK_SWDIO

U3 ESDALC6V1-1U2 STLK_SWCLK

ESDALC6V1-1U2

U8 T_SWDIO T_SWCLK T_SWO T_JTDI

ESDALC6V1W5

U24 T_NRST T_VCP_TX T_VCP_RX

ESDALC6V1W5

T_JTDI

Pin attributions on ESD can be swapped for layout optimisation

LED STLK

LD4 Red Green

R9 330R LED_STLK

R8 330R

3V3_STLK

LD_BICOLOR_CMS

3V3_STLK

C34 C8 C33 C22 C17 C15 C9 C10 100nF

3V3_STLK

C21 C25 C14 C30 C29 C31 C32 C11 100nF

3V3_STLK

C35 4.7uF C36 1uF C16 100nF

ST-LINK USB CONNECTOR

5V_USB_CHGR

C6 100pF

U6 ESDA7P60-1U1M

Capacitor close to pin 1

Matched Net Lengths [Tolerance = 2.5mm]

Impedance Constraint [Min = 85.00 Max = 95.00]

CN1 STLK

USB_Micro-B receptacle

VBUS DM DP ID GND Shield Shield Shield Shield EXP EXP

USB_DEV_HS_CN_N USB_DEV_HS_CN_P

USB

U5 NC D- D+ GND D- D+

ECMF02-2AMX6

USB_DEV_HS_N USB_DEV_HS_P

USB_uB_105017-0001

SW LEVEL SHIFTER FOR MCU_1V8

MCU_1V8/3V3

ST_LINK_3V3

VDD C26 100nF C27 100nF 3V3_STLK

U10 VccB VccA B1 A1 B2 A2 DIR GND

SN74LVC2T45DCUT

T_SWDIO T_SWO

T_SWDIO 47R R10 T_SWDIOa

T_SWO 47R R13

T_SWDIO_IN T_SWOa

SB5 DNF

R70 100R DNF

MCU_1V8/3V3

ST_LINK_3V3

VDD C4 100nF C2 100nF 3V3_STLK

U1 VccB VccA B1 A1 B2 A2 DIR GND

SN74LVC2T45DCUT

VDD R4 100K

T_VCP_TX T_VCP_TX 47R R3

STLK_VCP_RX

SB13 DNF

5V ST-LINK PROTECTION

5V_USB_CHGR

5V_USB_STLK

U2 STMPS2151STR IN OUT EN FAULT GND

T_PWR_EN

C3 1uF R2 1K R1 100K R7 10K C1 1uF

LD6 RED

ST-LINK POWER 3V3 / 150mA

3.3 Volts ST-LINK

5V_VIN 5V_EXT 5V_USB_CHGR

BAT60JFILM D1 D2 D3

U9 LD3985M33R Vin Vout INH GND BYPASS

3V3_STLK

C18 1uF C20 100nF C19 10nF C23 1uF C24 100nF

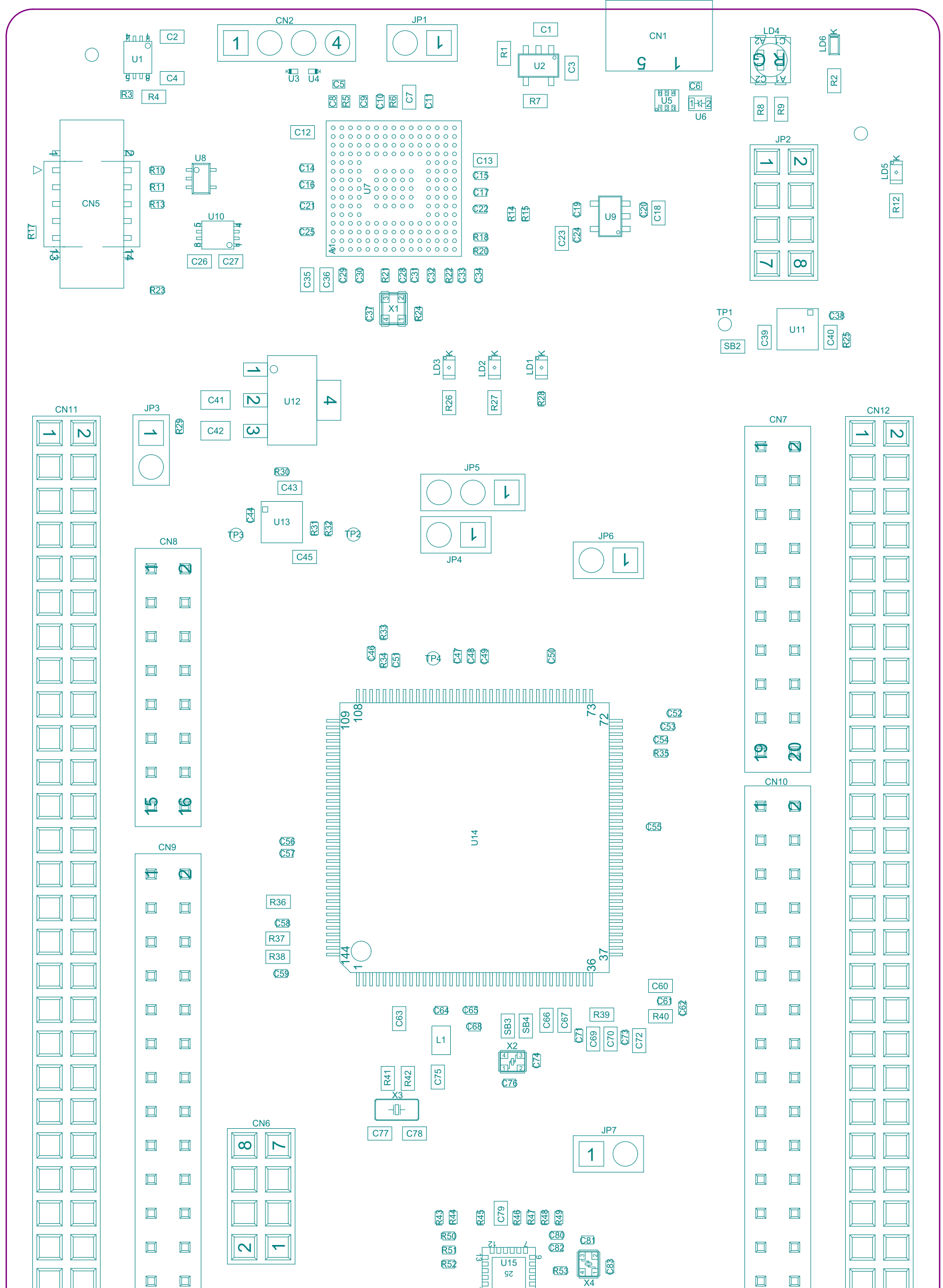
GND

CN3 Header 2x1 16mm HW7

CN4 Header 2x1 16mm HW8

Title: **STLINK_V3E**			
Project: **Nucleo144 H7 SMPS with STLINK V3**			
Variant: H7A3ZIQ			
Revision: D-01		Reference: MB1363	
Size: A3	Date: 24-OCT-19	Sheet: 9 of 9	

life.augmented



Project: Nucleo144 H7 SMPS with STLINK V3	
Layer: M14-Top Assembly	Gerber: .GM14
Variant: [No Variations]	Ref: MB1363
Date: 24-OCT-19	Rev: D

CN4

CN3

SB13

D1 K

D2 K

D3 K

SB5

R70

U24

Q1 Q2 Q3

R71 R72 R73

R76 R74 R75

SB6

SB7

SB8

SB11 SB12

SB9

SB10

SB14

SB24

SB15 SB16 SB103 SB17

SB18 SB19 SB20

SB21 SB22 SB23

SB25

SB26 SB27

SB31

SB34

SB28 SB29

SB32

SB35

SB30

SB33

SB36

SB37 SB38

SB43

SB47

SB51

SB54

SB58

SB63

SB65

SB77

SB78

SB80

SB40

SB44

SB48

SB52

SB56

SB62

SB39

SB41

SB45

SB49

SB53

SB57

SB42

SB46

SB50

SB55

SB59

SB64

SB60 SB61

SB68 SB69 SB70 SB71 SB72 SB73 SB74 SB75 SB76 SB66 SB67

SB79

SB81

SB89

SB93

SB94

SB96

SB84 SB90

SB91

SB92

SB82 SB83

R77

SB85 SB86

SB87 SB88

SB95

SB97

SB104

SB98

R78 R79 R80 R81

SB99

SB100

CN15

1

CN16

1

SB102

SB101

Project: Nucleo144 H7 SMPS with STLINK V3	
Layer: M15-Bottom Assembly	Gerber:.GM15
Variant: [No Variations]	Ref: MB1363
Date: 24-OCT-19	Rev: D