STM32G5 MC Discovery control board

MB2070

Table of contents

Sheet 1: Project overview (this page)

Sheet 2: Top

Sheet 3: STM32 microcontroller IOs

Sheet 4: Clock and user interface

Sheet 5: STM32 microcontroller power

Sheet 6: MC Connector V2

Sheet 7: STMorpho MC

Sheet 8: POSENC1

Sheet 9: POSENC2

Sheet 10: Power

Sheet 11: STLINK-V3EC

Sheet 12: External Debug Interface

Sheet 13: Mechanical

Legend

General comment such as function title, configuration, ...

Text to be added to silkscreen.

Warning text.

Notes to generate the board layout.

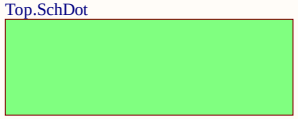
Open Platform License Agreement

The Open Platform License Agreement (“Agreement”) is a binding legal contract between you ("You") and STMicroelectronics International N.V. (“ST”), a company incorporated under the laws of the Netherlands acting for the purpose of this Agreement through its Swiss branch 39, Chemin du Champ des Filles, 1228 Plan-les-Ouates, Geneva, Switzerland.

By using the enclosed reference designs, schematics, PC board layouts, and documentation, in hardcopy or CAD tool file format (collectively, the “Reference Material”), You are agreeing to be bound by the terms and conditions of this Agreement. Do not use the Reference Material until You have read and agreed to this Agreement terms and conditions. The use of the Reference Material automatically implies the acceptance of the Agreement terms and conditions.

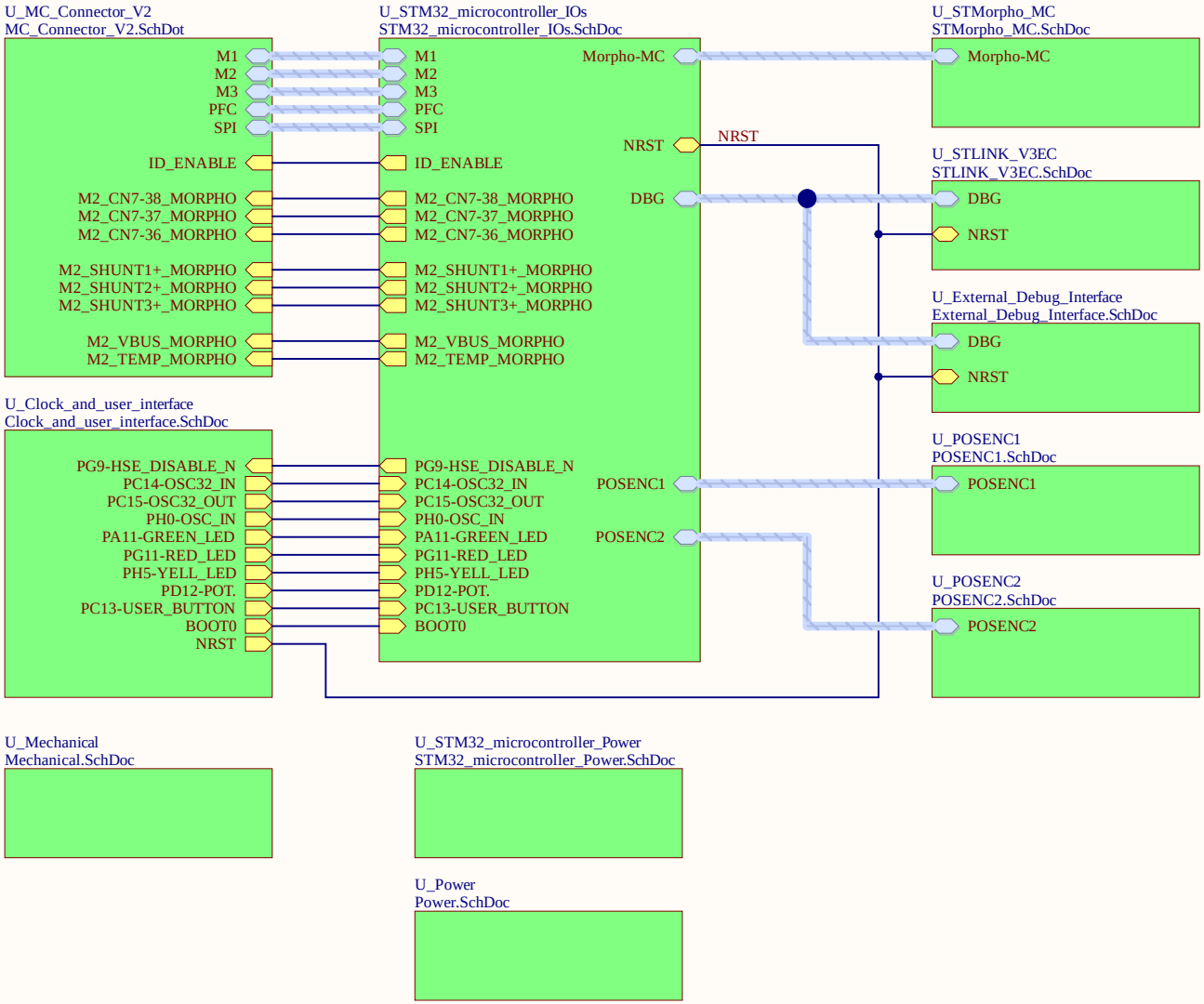
The complete Open Platform License Agreement can be found on www.st.com/opla.

U_Top
Top.SchDot



Title: **Project Overview**			
Project: **STM32G5 MC Discovery control board**			
Variant: G564QE			
Revision: B-02		Reference: MB2070	
Size: A4	Date: 05-JUN-26	Sheet: 1 of 13	

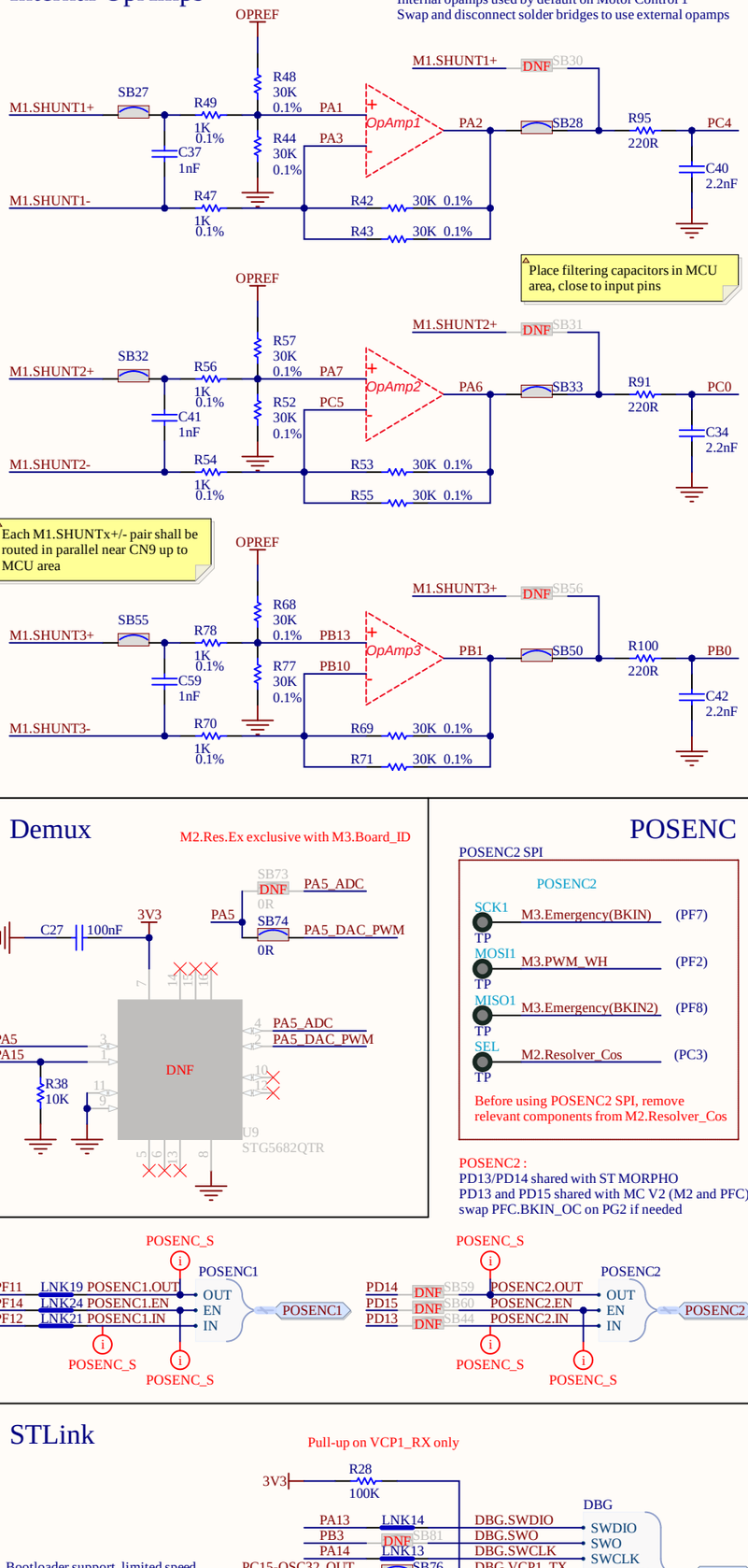
These 8 links connect some STMorpho signals from MCU_IOs page to each relevant input pin filter of MC_Connector_V2 page



Title: **Top**		
Project: **STM32G5 MC Discovery control board**		
Variant: G564QE		
Revision: B-02		Reference: MB2070
Size: A4	Date: 05-JUN-26	Sheet: 2 of 13

Internal OpAmps

Internal opamps used by default on Motor Control 1
Swap and disconnect solder bridges to use external opamps



Demux

M2.Res.Ex exclusive with M3.Board_ID

POSENC

POSENC2 SPI

Before using POSENC2 SPI, remove relevant components from M2.Resolver_Cos

POSENC2 :
PD13/PD14 shared with ST MORPHO
PD13 and PD15 shared with MC V2 (M2 and PFC)
swap PFC.BKIN_OC on PG2 if needed

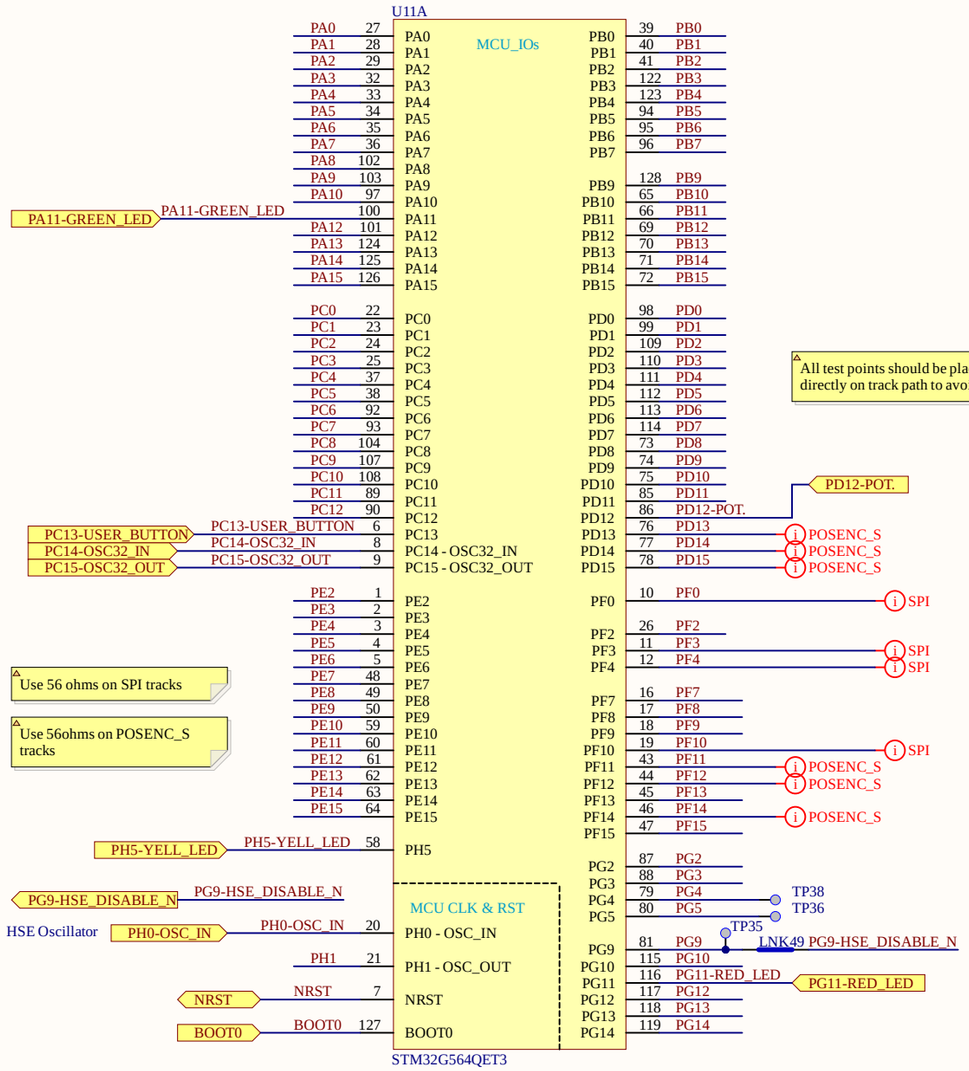
STLink

Pull-up on VCP1_RX only

Bootloader support, limited speed
Bootloader support, limited speed
No Bootloader, maximum speed
No Bootloader, maximum speed

Use internal pull-up on DBG.VCP2_RX if necessary

STM32 microcontroller



All test points should be placed directly on track path to avoid stubs

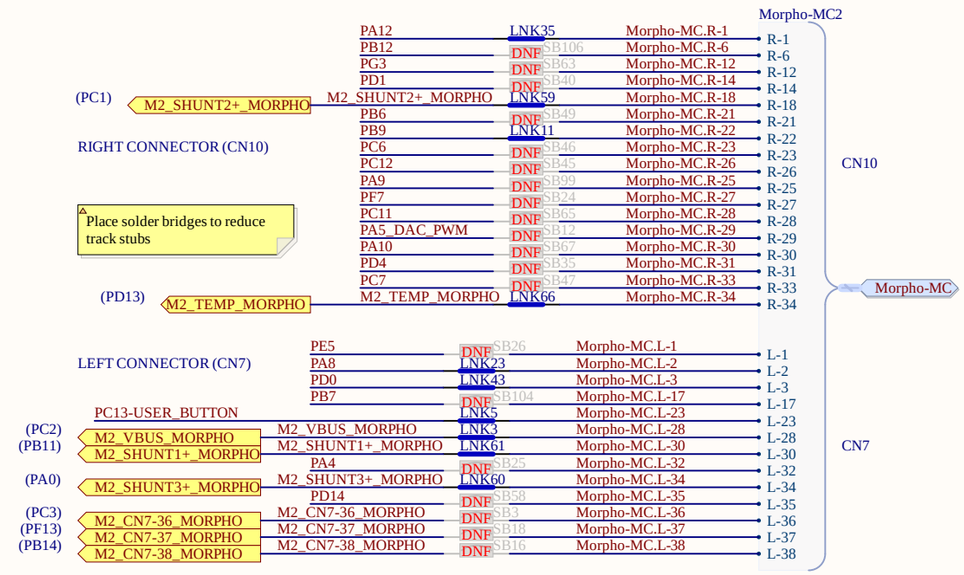
Use 56 ohms on SPI tracks

Use 56ohms on POSENC_S tracks

ST MORPHO Motor Control 2

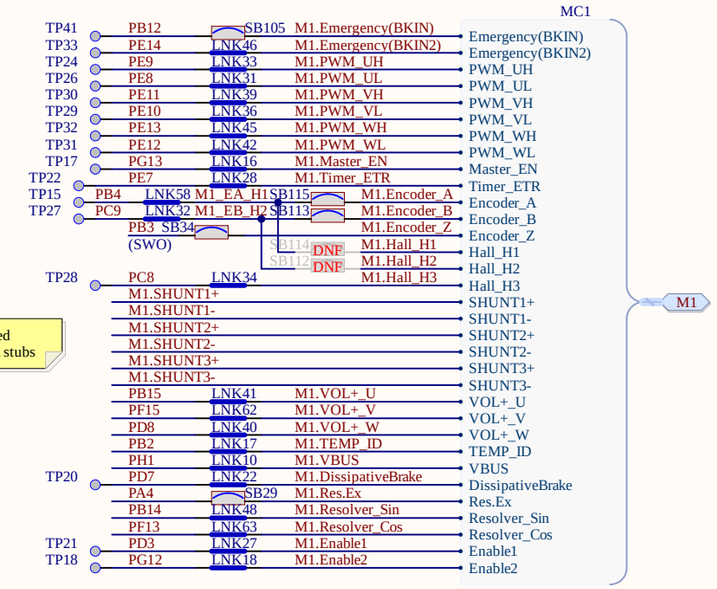
MC2 is shared between ST MORPHO and MC V2 connectors
Connect Solder bridges accordingly

Solder bridges to reduce stubs between STMorpho MC and MC Connector V2
LNKxx for non critical signals (or to allow good Harnesses at compilation when link to other page)

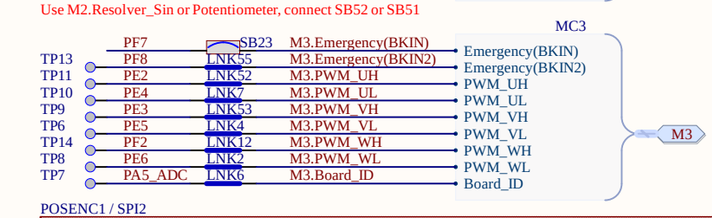


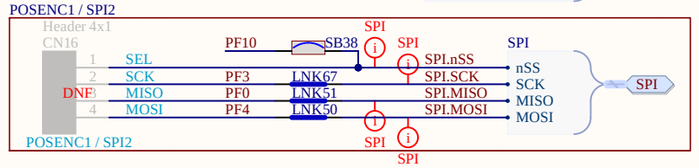
MotorControl Connector V2

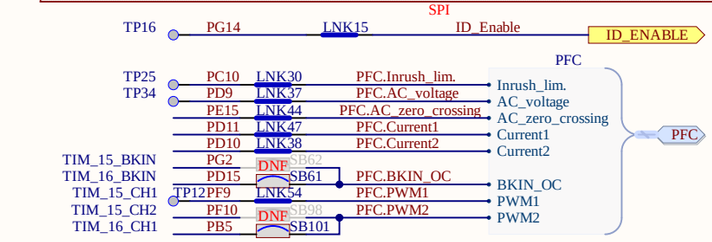
LNKxx to allow good Harnesses at compilation
Solder bridges to reduce stubs
10 Solder bridges to isolate Encoder/Hall signals on PCIE



Use M2.Resolver_Sin or Potentiometer, connect SB52 or SB51





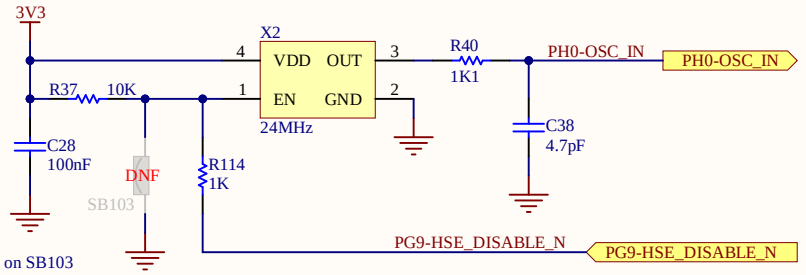


Title: **STM32 microcontroller IOs**		
Project: **STM32G5 MC Discovery control board**		
Variant: G564QE		
Revision: B-02		Reference: MB2070
Size: A3	Date: 05-JUN-26	Sheet: 3 of 13

Clock and user interface

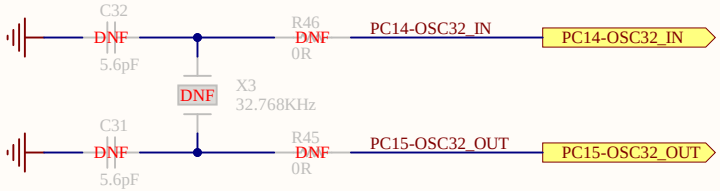
HSE Oscillator

Use HSE Analog low swing input mode

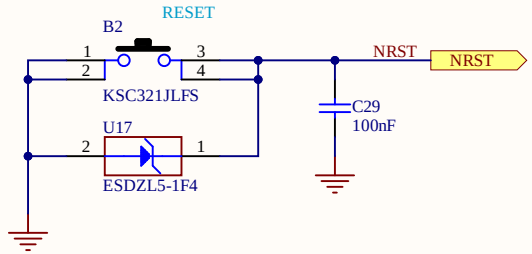


To disable HSE oscillator:
either use PG9 , either move R114 on SB103

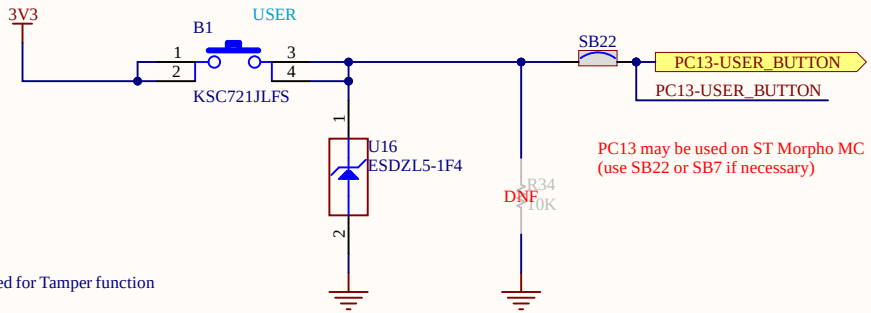
LSE Crystal



Reset button



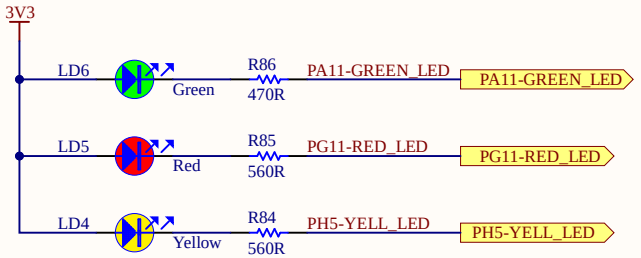
User button



PC13 may be used on ST Morpho MC (use SB22 or SB7 if necessary)

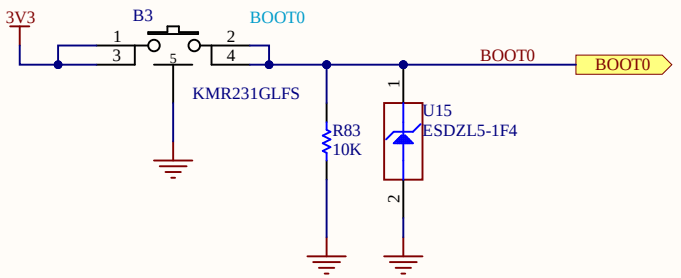
10k resistor only needed for Tamper function

User LEDs

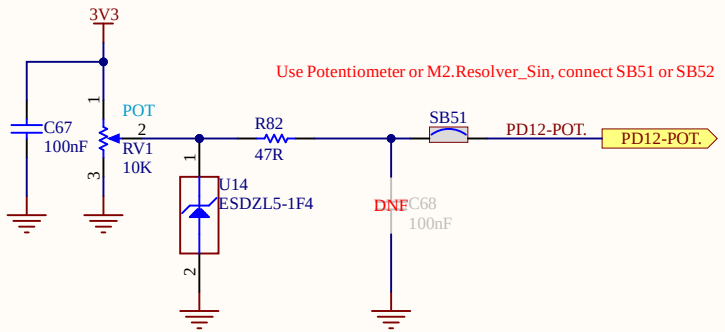


Boot0

PB PRESSED DURING RESET (1) = BOOTLOADER
DEFAULT (0) = INTERNAL FLASH



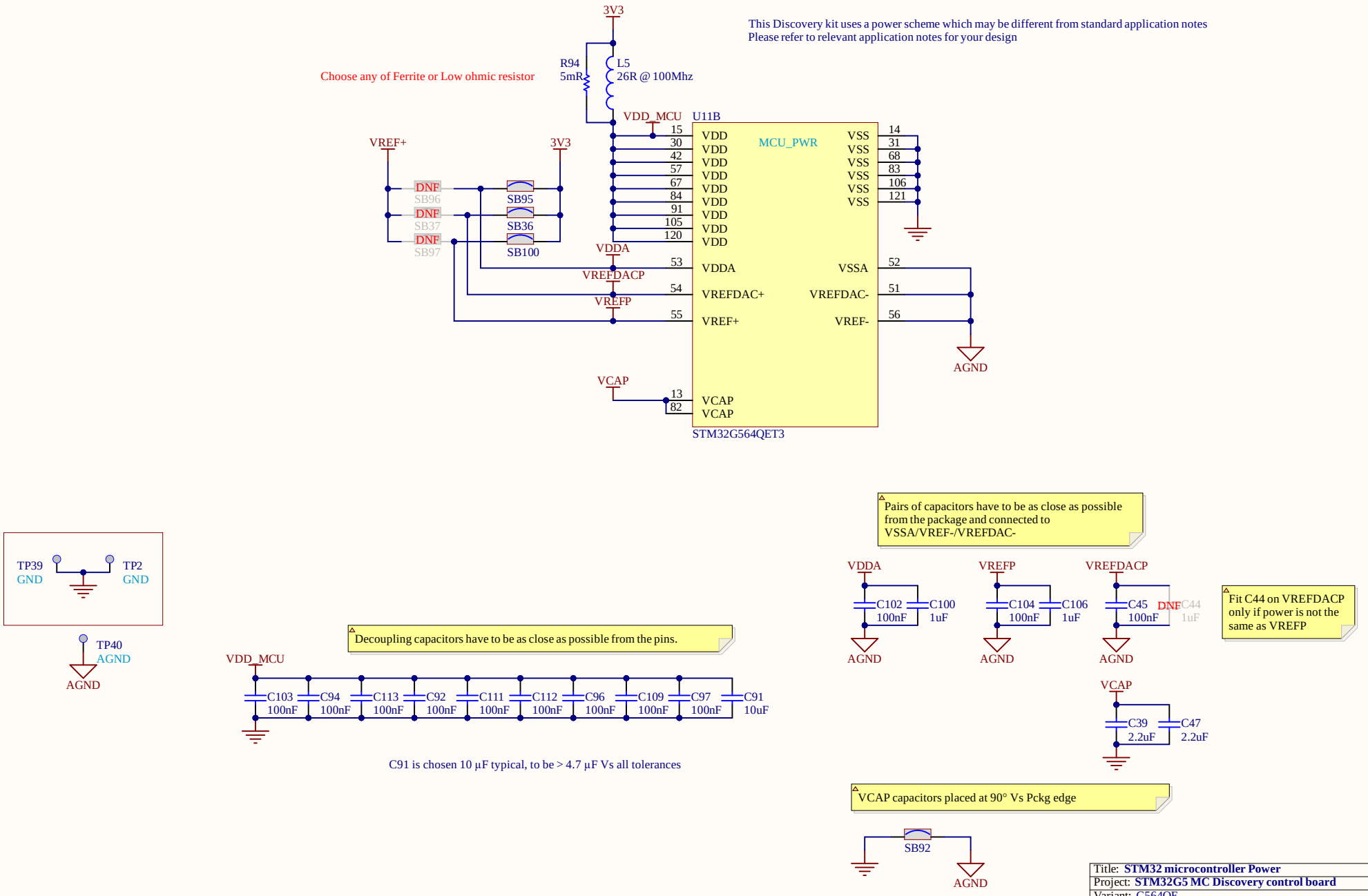
Potentiometer



Use Potentiometer or M2.Resolver_Sin, connect SB51 or SB52

Title: **Clock and user interface**		
Project: **STM32G5 MC Discovery control board**		
Variant: G564QE		
Revision: B-02		Reference: MB2070
Size: A4	Date: 05-JUN-26	Sheet: 4 of 13

STM32 microcontroller Power



Title: **STM32 microcontroller Power**		
Project: **STM32G5 MC Discovery control board**		
Variant: G564QE		
Revision: B-02		Reference: MB2070
Size: A4	Date: 05-JUN-26	Sheet: 5 of 13

MotorControl Connector V2

MC2 is shared between ST MORPHO and MC V2 connectors

IMPORTANT NOTE: Before using any Motor Control V2 PCIE expansion board, please refer to relevant user manual to check if some HW specific configuration are needed

Optional stitching capacitor for return current path on 3V3/GND, to be placed close to SPI2 / POSENC signals layer change and close to 3V3 track/plan and GND plan

3V3 — DNF C115 100nF

MC1

M1 ←
- Emergency(BKIN) — M1.Emergency(BKIN)
- Emergency(BKIN2) — M1.Emergency(BKIN2)
- PWM_UH — M1.PWM_UH
- PWM_UL — M1.PWM_UL
- PWM_VH — M1.PWM_VH
- PWM_VL — M1.PWM_VL
- PWM_WH — M1.PWM_WH
- PWM_WL — M1.PWM_WL
- Master_EN — M1.Master_EN
- Timer_ETR — M1.Timer_ETR
- Encoder_A — M1.Encoder_A
- Encoder_B — M1.Encoder_B
- Encoder_Z — M1.Encoder_Z
- Hall_H1 — M1.Hall_H1
- Hall_H2 — M1.Hall_H2
- Hall_H3 — M1.Hall_H3
- SHUNT1+ — M1.SHUNT1+
- SHUNT1- — M1.SHUNT1-
- SHUNT2+ — M1.SHUNT2+
- SHUNT2- — M1.SHUNT2-
- SHUNT3+ — M1.SHUNT3+
- SHUNT3- — M1.SHUNT3-
- VOL+_U — M1.VOL+_U
- VOL+_V — M1.VOL+_V
- VOL+_W — M1.VOL+_W
- TEMP_ID — M1.TEMP_ID
- VBUS — M1.VBUS
- DissipativeBrake — M1.DissipativeBrake
- Res.Ex — M1.Res.Ex
- Resolver_Sin — M1.Resolver_Sin
- Resolver_Cos — M1.Resolver_Cos
- Enable1 — M1.Enable1
- Enable2 — M1.Enable2

MC2 is shared between ST MORPHO and MC V2 connectors

MC2

M2 ←
- Emergency(BKIN) — M2.Emergency(BKIN)
- Emergency(BKIN2) — M2.Emergency(BKIN2)
- PWM_UH — M2.PWM_UH
- PWM_UL — M2.PWM_UL
- PWM_VH — M2.PWM_VH
- PWM_VL — M2.PWM_VL
- PWM_WH — M2.PWM_WH
- PWM_WL — M2.PWM_WL
- Master_EN — M2.Master_EN
- Timer_ETR — M2.Timer_ETR
- Encoder_A — M2.Encoder_A
- Encoder_B — M2.Encoder_B
- Encoder_Z — M2.Encoder_Z
- Hall_H1 — M2.Hall_H1
- Hall_H2 — M2.Hall_H2
- Hall_H3 — M2.Hall_H3
- SHUNT1+ — M2.SHUNT1+
- SHUNT2+ — M2.SHUNT2+
- SHUNT3+ — M2.SHUNT3+
- TEMP_ID — M2.TEMP_ID
- VBUS — M2.VBUS
- DissipativeBrake — M2.DissipativeBrake
- Res.Ex — M2.Res.Ex
- Resolver_Sin — M2.Resolver_Sin
- Resolver_Cos — M2.Resolver_Cos

MC3

M3 ←
- Emergency(BKIN) — M3.Emergency(BKIN)
- Emergency(BKIN2) — M3.Emergency(BKIN2)
- PWM_UH — M3.PWM_UH
- PWM_UL — M3.PWM_UL
- PWM_VH — M3.PWM_VH
- PWM_VL — M3.PWM_VL
- PWM_WH — M3.PWM_WH
- PWM_WL — M3.PWM_WL
- Board_ID — M3.Board_ID

SPI

SPI ←
- nSS — SPI.nSS
- SCK — SPI.SCK
- MISO — SPI.MISO
- MOSI — SPI.MOSI

ID_ENABLE — ID_Enable

PFC

PFC ←
- AC_voltage — PFC.AC_voltage
- AC_zero_crossing — PFC.AC_zero_crossing
- Current1 — PFC.Current1
- Current2 — PFC.Current2
- BKIN_OC — PFC.BKIN_OC
- Inrush_lim. — PFC.Inrush_lim.
- PWM1 — PFC.PWM1
- PWM2 — PFC.PWM2

CN9A

SPI2_NSS (PF10)	SPI.nSS	A01	A01 B01	B01	SPI.MISO	SPI2_MISO (PF0)	
SPI2_SCK (PF3)	SPI.SCK	A02	A02 B02	B02	SPI.MOSI	SPI2_MOSI (PF4)	
		A03	A03 B03	B03			
		A04	A04 B04	B04			
P5V can power MB2070 with 1.5A max	P5V	A05	A05 B05	B05	P5V	P5V can power MB2070 with 1.5A max	
3V3 is supplied to MC V2 (500 mA max)		A06	A06 B06	B06	VREF+	VREF+ not used by default (pages 3 & 10)	
		A07	A07 B07	B07			
(PG14)	ID_Enable	A08	A08 B08	B08			
		A09	A09 B09	B09			
		A10	A10 B10	B10			
		A11	A11 B11	B11			
TIM_1_BKIN (PB12)	M1.Emergency(BKIN)	A12	A12 B12	B12	M1.Emergency(BKIN2)	TIM_1_BKIN2 (PE14)	
TIM_1_CH1 (PE9)	M1.PWM_UH	A13	A13 B13	B13	M1.PWM_UL	TIM_1_CH1N (PE8)	
TIM_1_CH2 (PE11)	M1.PWM_VH	A14	A14 B14	B14	M1.PWM_VL	TIM_1_CH2N (PE10)	
TIM_1_CH3 (PE13)	M1.PWM_WH	A15	A15 B15	B15	M1.PWM_WL	TIM_1_CH3N (PE12)	
GPIO (PG13)	M1.Master_EN	A16	A16 B16	B16	M1.Encoder_A	TIM_3_CH1 (PB4)	
TIM_1_ETR (PE7)	M1.Timer_ETR	A17	A17 B17	B17	M1.Encoder_B	TIM_3_CH2 (PC9)	
TIM_3_CH1 (PB4)	M1.Hall_H1	A18	A18 B18	B18	M1.Encoder_Z	TIM_3_ETR (PB3)	
TIM_3_CH2 (PC9)	M1.Hall_H2	A19	A19 B19	B19	M1.Hall_H3	TIM_3_CH3 (PC8)	
		A20	A20 B20	B20			
OPAMP1_IN0+ or COMP1_IN1+ (PA1) or ADC_2_IN5 (PC4)	M1.SHUNT1+	A21	A21 B21	B21	M1.SHUNT1-	OPAMP1_IN0- (PA3)	
OPAMP2_IN0+ or COMP2_IN1+ (PA7) or ADC_12_IN6 (PC0)	M1.SHUNT2+	A22	A22 B22	B22	M1.SHUNT2-	OPAMP2_IN1- (PC5)	
OPAMP3_IN1+ or COMP5_IN1+ (PB13) or ADC_1_IN15 (PB0)	M1.SHUNT3+	A23	A23 B23	B23	M1.SHUNT3-	OPAMP3_IN1- (PB10)	
and ADC_3_IN12 (PB0)		A24	A24 B24	B24			
ADC_2_IN15 (PB15)	M1_VOL+_U_C	A25	A25 B25	B25			
ADC_1_IN0 (PF15)	M1_VOL+_V_C	A26	A26 B26	B26			
ADC_3_IN6 (PD8)	M1_VOL+_W_C	A27	A27 B27	B27			
ADC_2_IN12 (PB2)	M1_TEMP_ID_C	A28	A28 B28	B28	M1.Res.Ex	DAC_1_OUT1 (PA4)	
ADC_2_IN10 (PH1)	M1_VBUS_C	A29	A29 B29	B29	M1_Resolver_Sin_C	ADC_1_IN5 (PB14)	
TIM9_CH1 or GPIO (PD7)	M1.DissipativeBrake	A30	A30 B30	B30	M1_Resolver_Cos_C	ADC_2_IN0 (PF13)	
		A31	A31 B31	B31			
		A32	A32 B32	B32			
ADC_3_IN15 (PD9)	AC_voltage_C	A33	A33 B33	B33	AC_zero_crossing_C	ADC_3_IN2 (PE15)	
ADC_3_IN8 (PD11)	PFC_Current1_C	A34	A34 B34	B34	PFC_Current2_C	ADC_3_IN7 (PD10)	
TIM_15/16_BKIN (PG2/PD15)	PFC.BKIN_OC	A35	A35 B35	B35	PFC.Inrush_lim.	GPIO (PC10)	
TIM_15_CH1 (PF9)	PFC.PWM1	A36	A36 B36	B36	PFC.PWM2	TIM_15_CH2/16_CH1 (PF10/PB5)	
TIM_8_BKIN (PD2)	M2.Emergency(BKIN)	A37	A37 B37	B37	M2.Emergency(BKIN2)	TIM_8_BKIN2 (PD1)	
TIM_8_CH1 (PC6)	M2.PWM_UH	A38	A38 B38	B38	M2.PWM_UL	TIM_8_CH1N (PA10)	
TIM_8_CH2 (PB6)	M2.PWM_VH	A39	A39 B39	B39	M2.PWM_VL	TIM_8_CH2N (PC11)	
TIM_8_CH3 (PC7)	M2.PWM_WH	A40	A40 B40	B40	M2.PWM_WL	TIM_8_CH3N (PC12)	
GPIO (PA8)	M2.Master_EN	A41	A41 B41	B41	M2.Encoder_A	TIM_2_CH1 (PB7)	

PCIE-Gold Finger-X16

CN9B

TIM_8_ETR (PG3)	M2.Timer_ETR	A42	A42 B42	B42	M2.Encoder_B	TIM_2_CH2 (PD4)	
TIM_2_CH1 (PB7)	M2.Hall_H1	A43	A43 B43	B43	M2.Encoder_Z	TIM_2_ETR (PA9)	
TIM_2_CH2 (PD4)	M2.Hall_H2	A44	A44 B44	B44	M2.Hall_H3	TIM_2_CH3 (PA9)	
		A45	A45 B45	B45			
ADC_12_IN14 (PB11)	M2_SHUNT1+_C	A46	A46 B46	B46			
ADC_12_IN7 (PC1)	M2_SHUNT2+_C	A47	A47 B47	B47			
ADC_12_IN1 (PA0)	M2_SHUNT3+_C	A48	A48 B48	B48			
		A49	A49 B49	B49			
ADC_1_IN5 (PB14)	M2_VOL+_U_C	A50	A50 B50	B50			
ADC_2_IN0 (PF13)	M2_VOL+_V_C	A51	A51 B51	B51			
ADC_12_IN9 (PC3)	M2_VOL+_W_C	A52	A52 B52	B52			
ADC_3_IN10 (PD13)	M2_TEMP_ID_C	A53	A53 B53	B53	M2.Res.Ex	DAC_2_OUT1 (PA5)	
ADC_12_IN8 (PC2)	M2_VBUS_C	A54	A54 B54	B54	M2_Resolver_Sin_C	ADC_3_IN9 (PD12)	
TIM9_CH2 or GPIO (PG10)	M2.DissipativeBrake	A55	A55 B55	B55	M2_Resolver_Cos_C	ADC_12_IN9 (PC3)	
		A56	A56 B56	B56			
TIM_20_BKIN (PF7)	M3.Emergency(BKIN)	A57	A57 B57	B57	M3.Emergency(BKIN2)	TIM_20_BKIN2 (PF8)	
TIM_20_CH1 (PE2)	M3.PWM_UH	A58	A58 B58	B58	M3.PWM_UL	TIM_20_CH1N (PE4)	
TIM_20_CH2 (PE3)	M3.PWM_VH	A59	A59 B59	B59	M3.PWM_VL	TIM_20_CH2N (PE5)	
TIM_20_CH3 (PF2)	M3.PWM_WH	A60	A60 B60	B60	M3.PWM_WL	TIM_20_CH3N (PE6)	
		A61	A61 B61	B61			
		A62	A62 B62	B62			
		A63	A63 B63	B63			
		A64	A64 B64	B64			
		A65	A65 B65	B65			
ADC_1_IN5 (PB14)	M3_SHUNT1+_C	A66	A66 B66	B66			
ADC_12_IN9 (PC3)	M3_SHUNT2+_C	A67	A67 B67	B67			
ADC_2_IN0 (PF13)	M3_SHUNT3+_C	A68	A68 B68	B68			
		A69	A69 B69	B69			
		A70	A70 B70	B70			
		A71	A71 B71	B71			
		A72	A72 B72	B72			
ADC_2_IN13 (PA5)	M3.Board_ID	A73	A73 B73	B73			
		A74	A74 B74	B74			
		A75	A75 B75	B75			
		A76	A76 B76	B76			
		A77	A77 B77	B77	M1.Enable1	GPIO (PD3)	
		A78	A78 B78	B78	M1.Enable2	GPIO (PG12)	
		A79	A79 B79	B79			
		A80	A80 B80	B80			
		A81	A81 B81	B81			
		A82	A82 B82	B82			

PCIE-Gold Finger-X16

Many critical analogue signals on this page require to be routed referenced to GND plan (above or below), at least for their most important length. List : PFC signals, Mx_VOLy+ signals, Mx_SHUNTy+/- signals (considering signals from MC V2 connector up to MCU connection).

M3.Board_ID is not active by default
M3.Board_ID is exclusive with M2.Res.Ex
Check Solder bridge configuration on MCU_IOs page (Demux)

M1.SHUNTx+/- pairs shall be routed in parallel from CN9 up to MCU area

M1_VOL+_U_C — R108 220R — M1.VOL+_U; R109 DNF 0R; C105 100pF
M1_VOL+_V_C — R105 220R — M1.VOL+_V; R104 DNF 0R; C99 100pF
M1_VOL+_W_C — R113 220R — M1.VOL+_W; R111 DNF 0R; C107 100pF

M1_TEMP_ID_C — R101 220R — M1.TEMP_ID; C43 2.2nF
M1_VBUS_C — R93 220R — M1.VBUS; C35 2.2nF

To use resolvers on M1 and M2, open SB17/SB21/SB6, and close SB14/SB20/SB5
To use Motor3 current sense, open SB17/SB21/SB6, and close SB15/SB19/SB4

M1_Resolver_Sin_C — SB14 DNF — M2_CN7-38_MORPHO — M2_CN7-38_MORPHO
M2_VOL+_U_C — SB17 — R66 220R — M1.Resolver_Sin (PB14)
M3_SHUNT1+_C — SB15 DNF — R64 DNF 0R; C49 100pF

M1_Resolver_Cos_C — SB20 DNF — M2_CN7-37_MORPHO — M2_CN7-37_MORPHO
M2_VOL+_V_C — SB21 — R102 220R — M1.Resolver_Cos (PF13)
M3_SHUNT3+_C — SB19 DNF — R103 DNF 0R; C98 100pF

M2_Resolver_Cos_C — SB5 DNF — M2_CN7-36_MORPHO — M2_CN7-36_MORPHO
M2_VOL+_W_C — SB6 — R39 220R — M2.Resolver_Cos (PC3)
M3_SHUNT2+_C — SB4 DNF — R41 DNF 0R; C36 100pF

Filtering capacitors may be placed either top or bottom, depending on the proximity with MCU, layout constraints and power plan

To improve filtering effect, it is necessary to connect MCU pin on all filtering capacitors' pad first (valid for all filtering capacitors of this page).

Ensure all the Solder bridges of this page (and solder bridges connected on M2_CN7-xx_MORPHO) are placed on PCB in order to avoid too long stubs at common connection point.

To use filters for ST Morpho signals, refer also to relevant solder bridges of MCU_IOs page

SB91 / SB77 / SB83 / SB110 / SB11 for M2 by default

M2_SHUNT1+_C — SB91 — R107 220R — M2.SHUNT1+ (PB11); M1_VOL+_U_C — DNF — R110 DNF 0R; C108 2.2nF
M2_SHUNT1+_MORPHO — DNF SB93 — DNF SB89

M2_SHUNT2+_C — SB77 — R97 220R — M2.SHUNT2+ (PC1); M1_VOL+_V_C — DNF — R98 DNF 0R; C93 2.2nF
M2_SHUNT2+_MORPHO — DNF SB87 — DNF SB82

M2_SHUNT3+_C — SB83 — R96 220R — M2.SHUNT3+ (PA0); M1_VOL+_W_C — DNF — R99 DNF 0R; C95 2.2nF
M2_SHUNT3+_MORPHO — DNF SB86 — DNF SB85

SB93 / SB87 / SB86 for M1

M2_TEMP_ID_C — SB110 — R76 220R — M2.TEMP_ID (PD13); C52 2.2nF
M2_TEMP_MORPHO — DNF SB111 — DNF

M2_VBUS_C — SB11 — R92 220R — M2.VBUS (PC2); C33 2.2nF
M2_VBUS_MORPHO — DNF SB10 — DNF

SB89 / SB82 / SB85 / SB111 / SB10 to connect Morpho signals on MC-V2 filters

M2_Resolver_Sin_C — R81 220R — M2.Resolver_Sin; C61 100pF

AC_voltage_C — R106 220R — PFC.AC_voltage; C101 100pF
AC_zero_crossing_C — R63 220R — PFC.AC_zero_crossing; C48 100pF

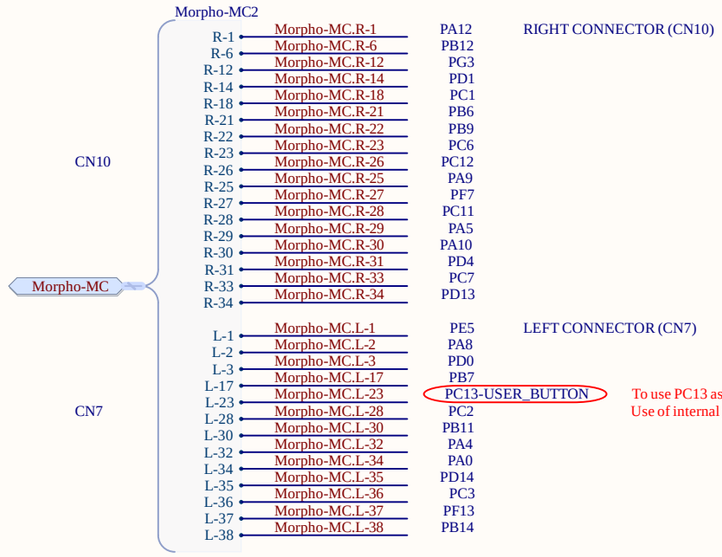
PFC_Current1_C — R67 220R — PFC.Current1; C55 100pF
PFC_Current2_C — R112 220R — PFC.Current2; C110 100pF

Title: **MC Connector V2**		
Project: **STM32G5 MC Discovery control board**		
Variant: G564QE		
Revision: B-02		Reference: MB2070
Size: A3	Date: 05-JUN-26	Sheet: 6 of 13

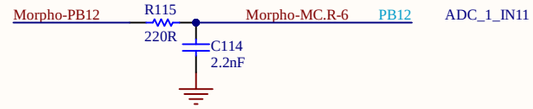
STMorpho MotorControl

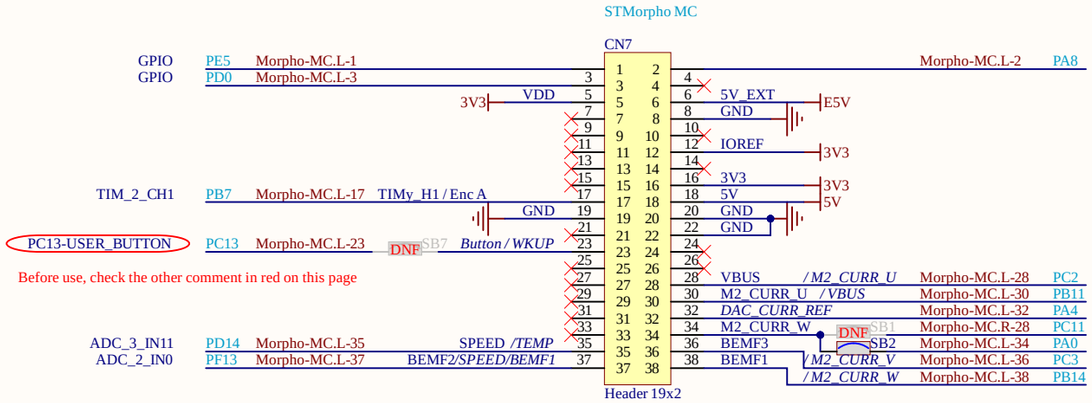
Motor Control 2 is shared between ST MORPHO and MC V2 connectors

All ST Morpho signals to be routed above GND

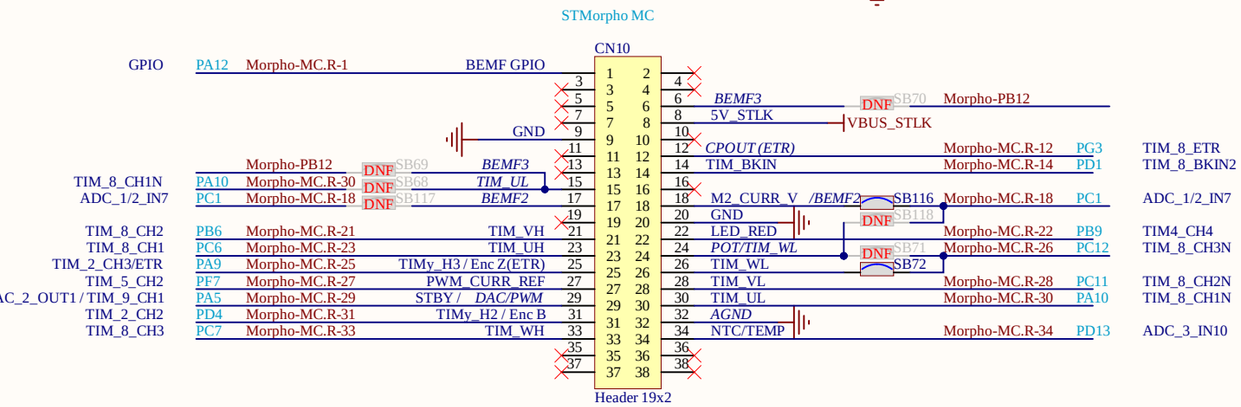


To use PC13 as WKUP and avoid inadvertent short circuit between User button and CN7 function, it is highly recommended to move SB22 on SB7
Use of internal pull-up / pull-down of PC13 is optional





Before use, check the other comment in red on this page



MotorControl shields compatibility and B-G564E-MC1S Solder bridge configuration

IMPORTANT NOTES:

- Motor Control 2 is shared between ST MORPHO and MC V2 connectors : ensure all the relevant solder bridges from MCU_IOs and MC-V2 pages are correctly configured
- To use 34-pin Motor control connector J7 of IHM09, a socket elevator should be used such as ESQ-119-24-x-D on the connectors CN7 / CN10
- Before using any X-Nucleo IHMxx , please refer to relevant user manual to check if some other HW specific configuration are needed

First, populate all the relevant ST Morpho Motor Control 2 Solder Bridge positions on page 3 (by moving the ones fitted on MC-V2 for each shared PIO)
Check SB59 and SB44 are not fitted (POSENC2 SPI)
using PE5 implies to connect SB26
using PB14 also implies to move SB17 on SB16
using PF13 also implies to move SB21 on SB18
using PC3 also implies to move SB6 on SB3
using PB11 also implies to move SB91 on SB89
using PC1 also implies to move SB77 on SB82
using PA0 also implies to move SB83 on SB85
using PD13 also implies to move SB110 on SB111
using PC2 also implies to move SB11 on SB10

Chose any of SB2, SB1 (by moving SB2)
Chose any of SB116, SB117 or SB118 (by moving SB116)
Use SB72 or SB71 or none
Use SB70 or SB69 or none
Use SB71 or SB118 or none
Use SB68 or SB69 or none

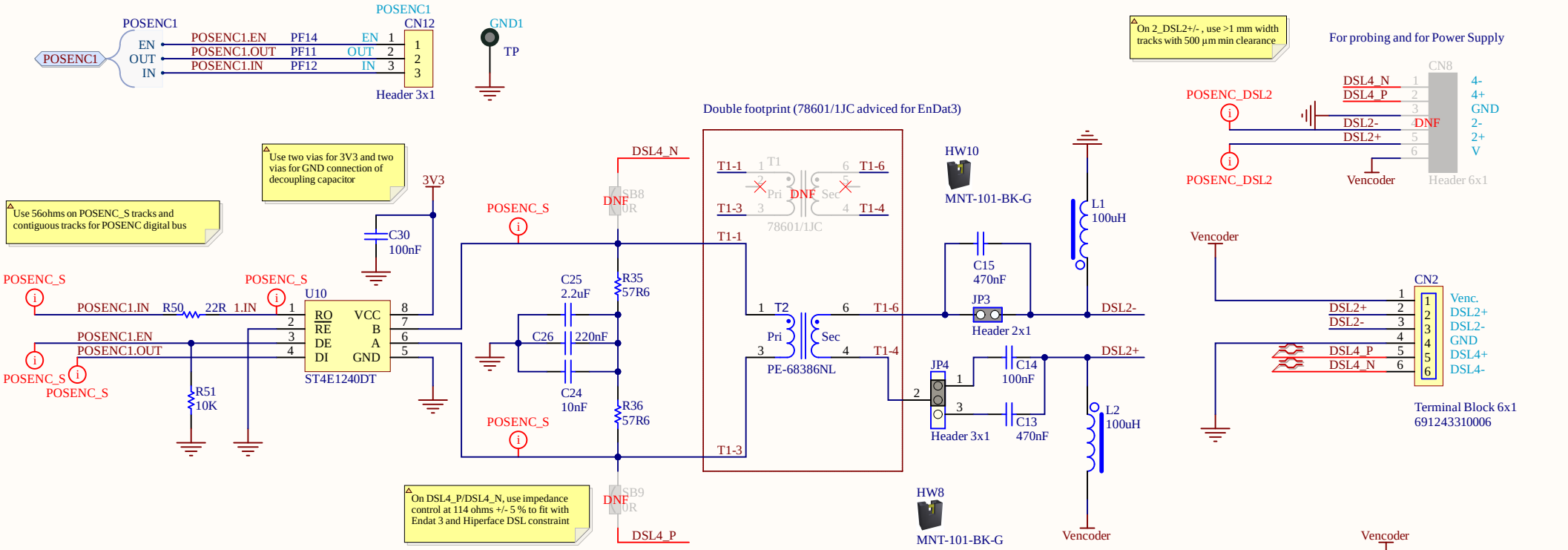
using SB1 also implies to move SB66 on SB65
using SB2 also implies to move SB83 on SB85
using SB68 also implies to move SB57 on SB67
using SB69 also implies to move SB105 on SB106
using SB70 also implies to move SB105 on SB106
using SB71 also implies to move SB109 on SB45
using SB72 also implies to move SB109 on SB45
using SB116 also implies to move SB77 on SB82
using SB117 also implies to move SB77 on SB82
using SB118 also implies to move SB77 on SB82

SBxx	IHM16 (default)	IHM07	IHM08	IHM09	Connector pin
SB1	OPEN	OPEN	CLOSED	CLOSED	CN7-34
SB2	CLOSED	CLOSED	OPEN	OPEN	CN7-34
SB68	OPEN	OPEN	CLOSED	CLOSED	CN10-15
SB69	OPEN	CLOSED	OPEN	OPEN	CN10-15
SB70	OPEN	OPEN	CLOSED	OPEN	CN10-6
SB71	OPEN	OPEN	CLOSED	CLOSED	CN10-24
SB72	CLOSED	OPEN	OPEN	OPEN	CN10-26
SB116	CLOSED	OPEN	CLOSED	OPEN	CN10-18
SB117	OPEN	OPEN	OPEN	OPEN	CN10-17
SB118	OPEN	CLOSED	OPEN	OPEN	CN10-24

Title: **STMorpho MC**			
Project: **STM32G5 MC Discovery control board**			
Variant: G564QE			
Revision: B-02		Reference: MB2070	
Size: A4	Date: 05-JUN-26	Sheet: 7 of 13	

Target to support both EnDat3 and Hiperface DSL (c) modes in 2-wire or 4-wire configuration through jumper changes (BOM changes optional)

Caution : ST4E1240DT RS485 transceiver is internally protected against ESD, but it is not protected against EFT> 4 kV (neither to EFT pulse train nor to surge transients)



2 configuration / 2 modes :
DSL2+/DSL2- 2-wire configuration in EnDat3 mode by default (move JP4 on 470nF and remove JP3 for HIPERFACE DSL mode)
DSL4+/DSL4- 4-wire configuration (connect Solder Bridges and disconnect JP3 / JP4)

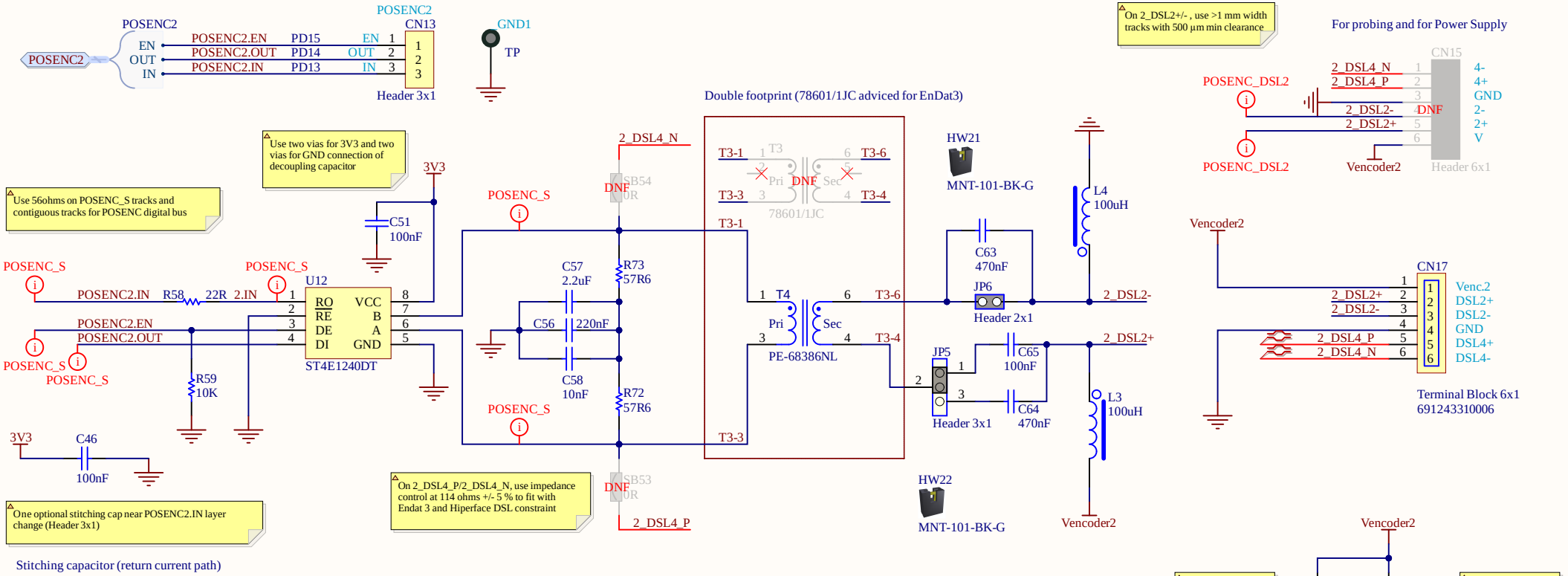
Other Information
Vencoder/GND must come from external Power supply (use CN8 pins to connect), refer to Encoder's specification for power supply voltage/current constraints.
57.6 ohms +/-1 % resistors chosen for EnDAT3 and HIPERFACE DSL (c)
Optional BOM change: can choose any of 2.2 uF or 220 nF (respectively for Hiperface DSL or for EnDat3), can chose any of PE-68386NL or 78601/1JC (for respectively Hiperface DSL or EnDat3)

Title: **POSENC1**		
Project: **STM32G5 MC Discovery control board**		
Variant: G564QE		
Revision: B-02		Reference: MB2070
Size: A4	Date: 05-JUN-26	Sheet: 8 of 13

Target to support both EnDat3 and Hiperface DSL (c) modes in 2-wire or 4-wire configuration through jumper changes (BOM changes optional)

Caution : ST4E1240DT RS485 transceiver is internally protected against ESD, but it is not protected against EFT> 4 kV (neither to EFT pulse train nor to surge transients)

Before using POSENC2, connect/disconnect relevant solder bridges (see POSENC block of MCU_IOs schematics page for shared POs)



2 configuration / 2 modes :
2_DSL2+/2_DSL2- 2-wire configuration in EnDat3 mode by default (move JP5 on 470nF and remove JP6 for HIPERFACE DSL mode)
2_DSL4+/2_DSL4- 4-wire configuration (connect Solder Bridges and disconnect JP5 / JP6)

Other Information
Vencoder2 /GND must come from external Power supply (use CN15 pins to connect), refer to Encoder's specification for power supply voltage/current constraints.
57.6 ohms +/-1 % resistors chosen for EnDAT3 and HIPERFACE DSL (c)
Optional BOM change: can choose any of 2.2 uF or 220 nF (respectively for Hiperface DSL or for EnDat3), can chose any of PE-68386NL or 78601/1JC (for respectively Hiperface DSL or EnDat3)

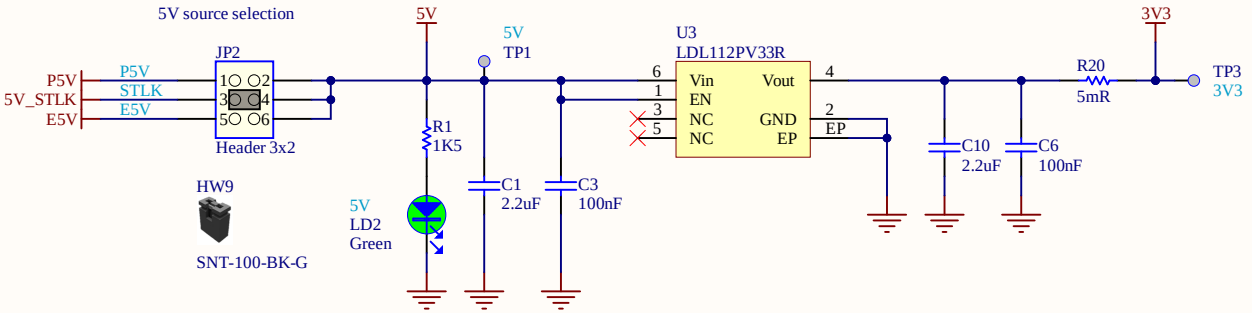
Title: **POSENC2**		
Project: **STM32G5 MC Discovery control board**		
Variant: G564QE		
Revision: B-02		Reference: MB2070
Size: A4	Date: 05-JUN-26	Sheet: 9 of 13

Power

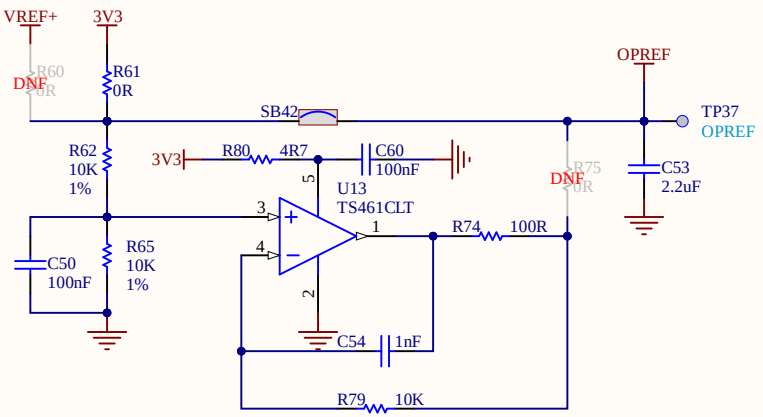
3.3V power

P5V (P5V): MOTOR CONTROL CONNECTOR V2 (1.5A max)
STLK (5V_STLK): 5V from USB-STLINK CONNECTOR (1.5A max)
E5V (5V_EXT): 5V from ST MORPHO CONNECTOR (1.5A max)

Note : 5V_STLK has embedded voltage and current protection (1.5A max)

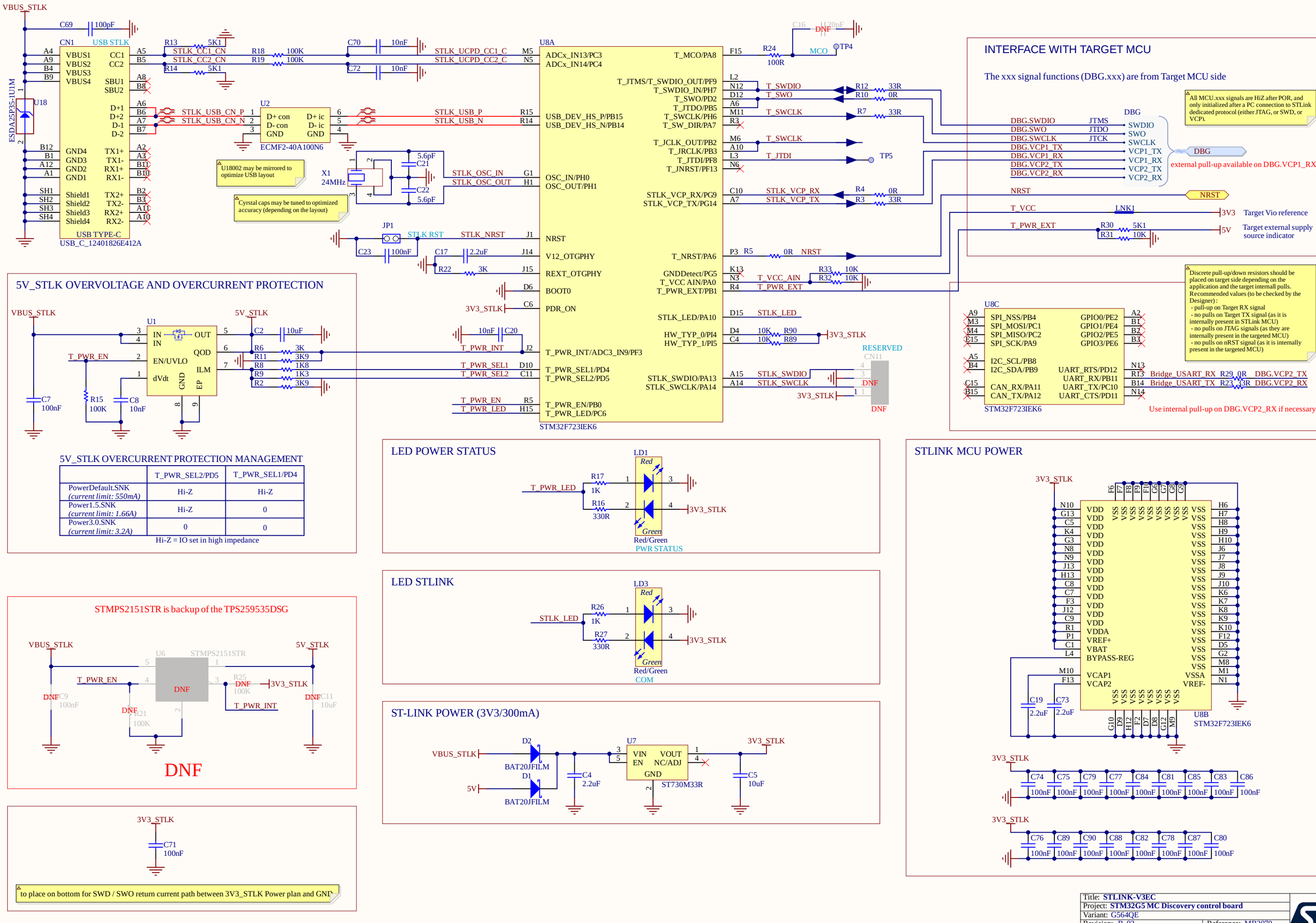


Reference voltage



Title: **Power**		
Project: **STM32G5 MC Discovery control board**		
Variant: G564QE		
Revision: B-02		Reference: MB2070
Size: A4	Date: 05-JUN-26	Sheet: 10 of 13

STLINK-V3EC

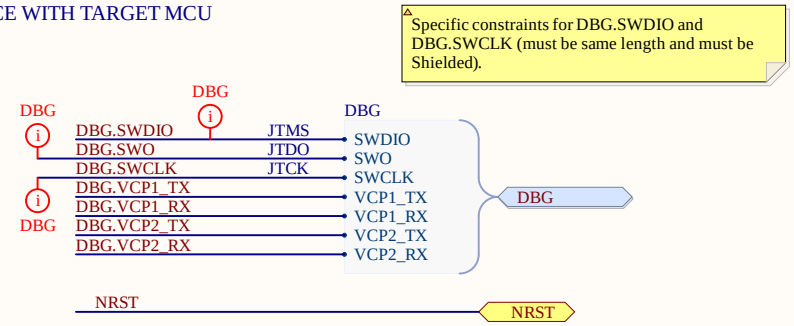


	T_PWR_SEL2/PD5	T_PWR_SEL1/PD4
PowerDefault.SNK *(current limit: 550mA)*	Hi-Z	Hi-Z
Power1.5.SNK *(current limit: 1.66A)*	Hi-Z	0
Power3.0.SNK *(current limit: 3.2A)*	0	0

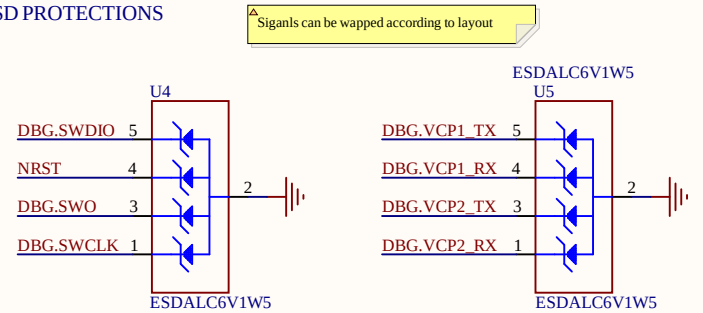
Title: **STLINK-V3EC**		
Project: **STM32G5 MC Discovery control board**		
Variant: G564QE		
Revision: B-02		Reference: MB2070
Size: A3	Date: 05-JUN-26	Sheet: 11 of 13

EXTERNAL DEBUG INTERFACE

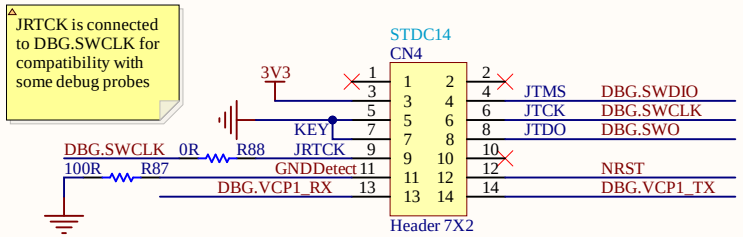
INTERFACE WITH TARGET MCU



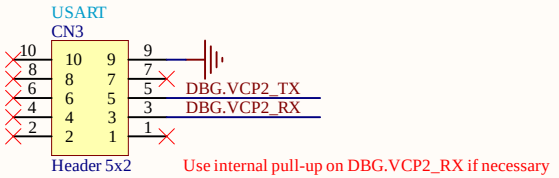
ESD PROTECTIONS



STDC14 RECEIVER



USART connector



The xxx signal functions (DBG.xxx) are from Target MCU side

Title: **External Debug Interface**		
Project: **STM32G5 MC Discovery control board**		
Variant: G564QE		
Revision: B-02		Reference: MB2070
Size: A4	Date: 05-JUN-26	Sheet: 12 of 13

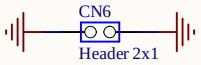
HW11

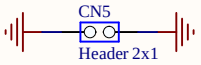
PCB

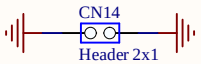
MB2070B

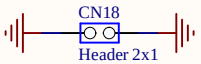
HW3

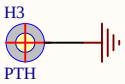
STICKER PRODUCT

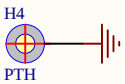


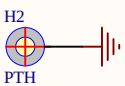


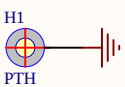
















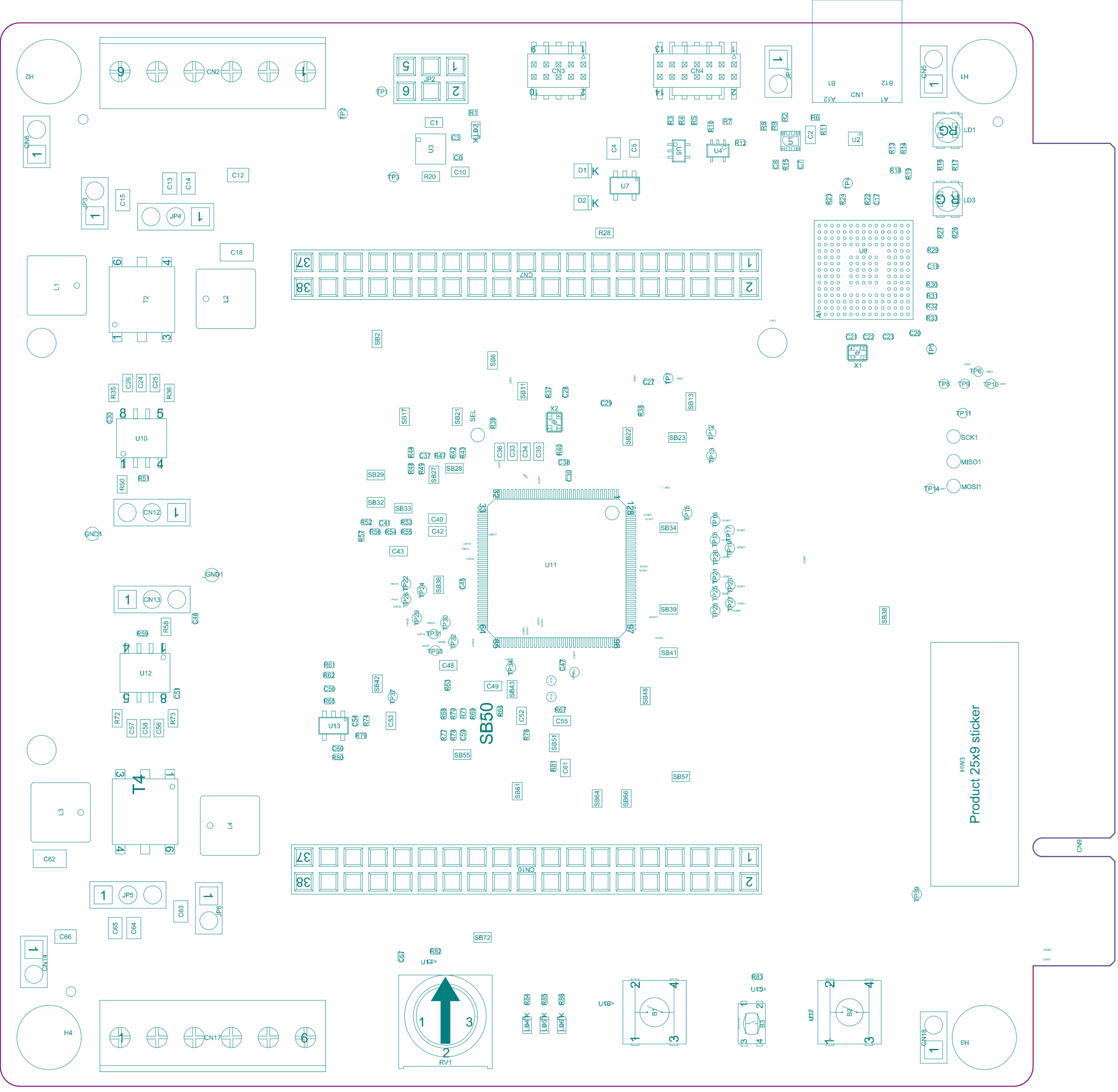




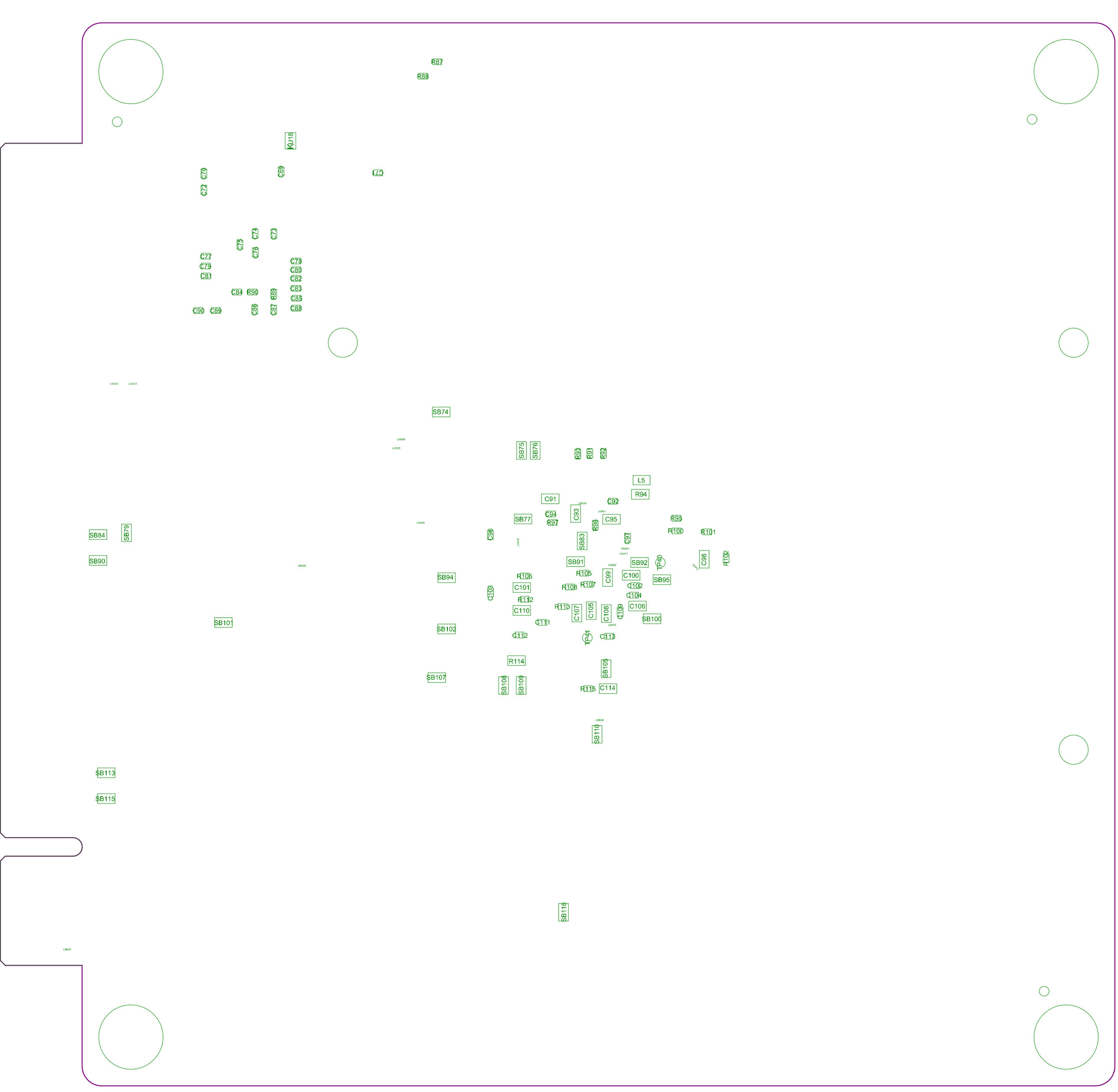




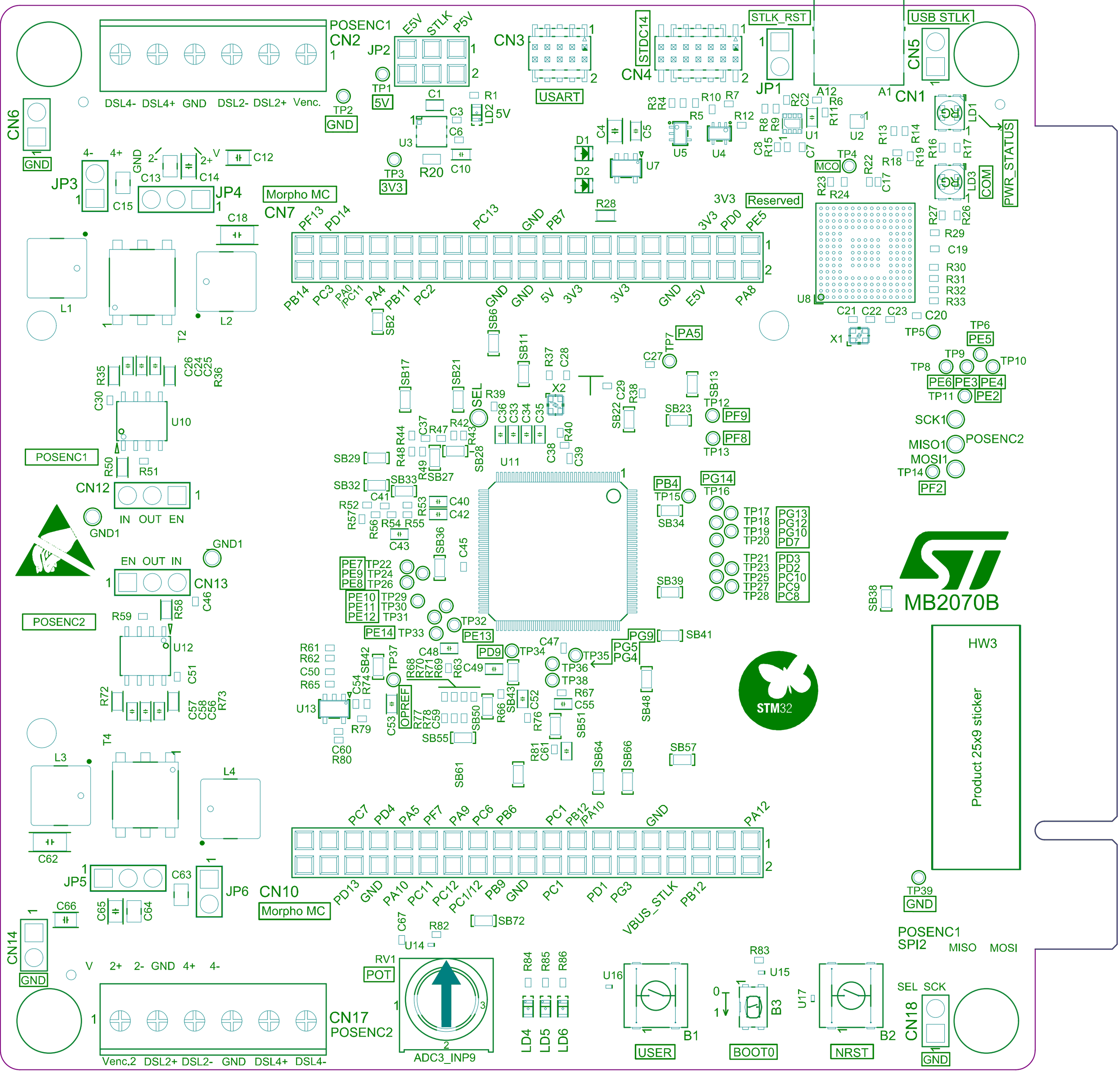
Title: **Mechanical**		
Project: **STM32G5 MC Discovery control board**		
Variant: G564QE		
Revision: B-02		Reference: MB2070
Size: A4	Date: 05-JUN-26	Sheet: 13 of 13



Project: STM32G5 MC Discovery control board	
Layer: M14-Top Assembly	Gerber: .GM14
Variant: G564QE	Ref: MB2070
Date: 05-JUN-26	Rev: B



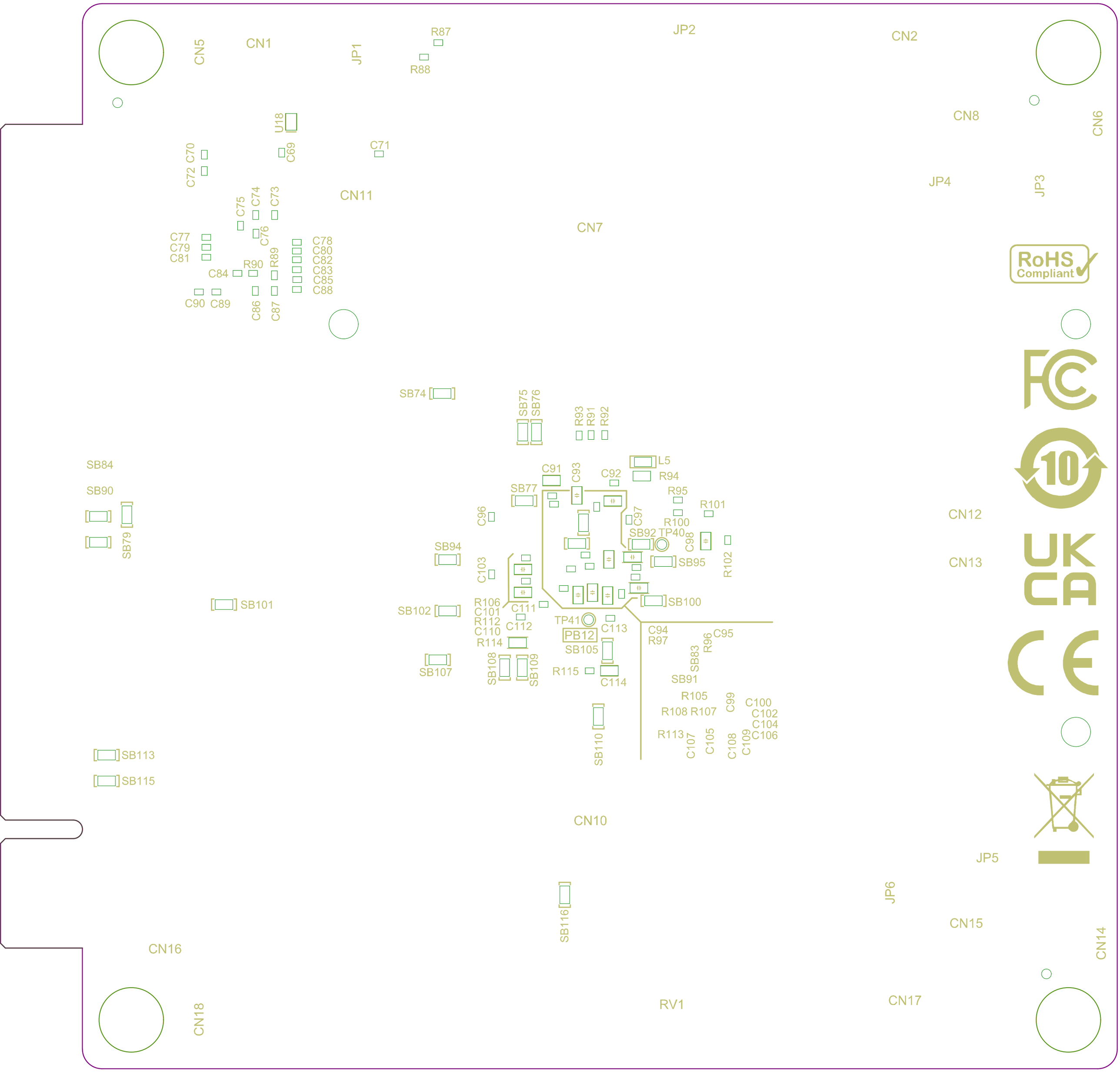
Project: STM32G5 MC Discovery control board	
Layer: M15-Bottom Assembly	Gerber:.GM15
Variant: G564QE	Ref: MB2070
Date: 05-JUN-26	Rev: B



Top Overlay

Mid-1 Overlay

.GTO



M15-Bottom Assembly .GM15

Bottom Overlay