
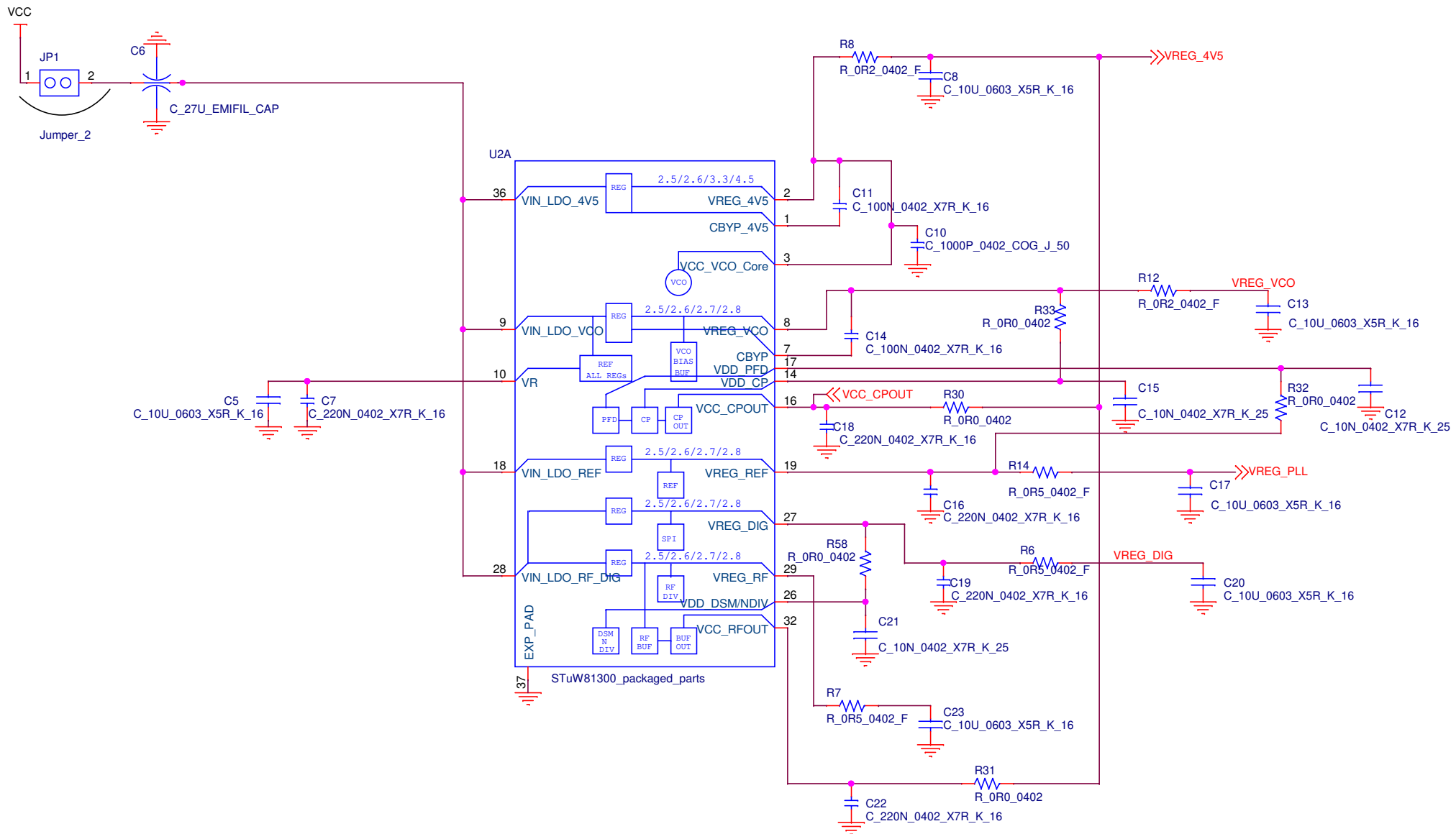

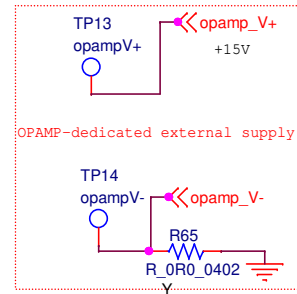
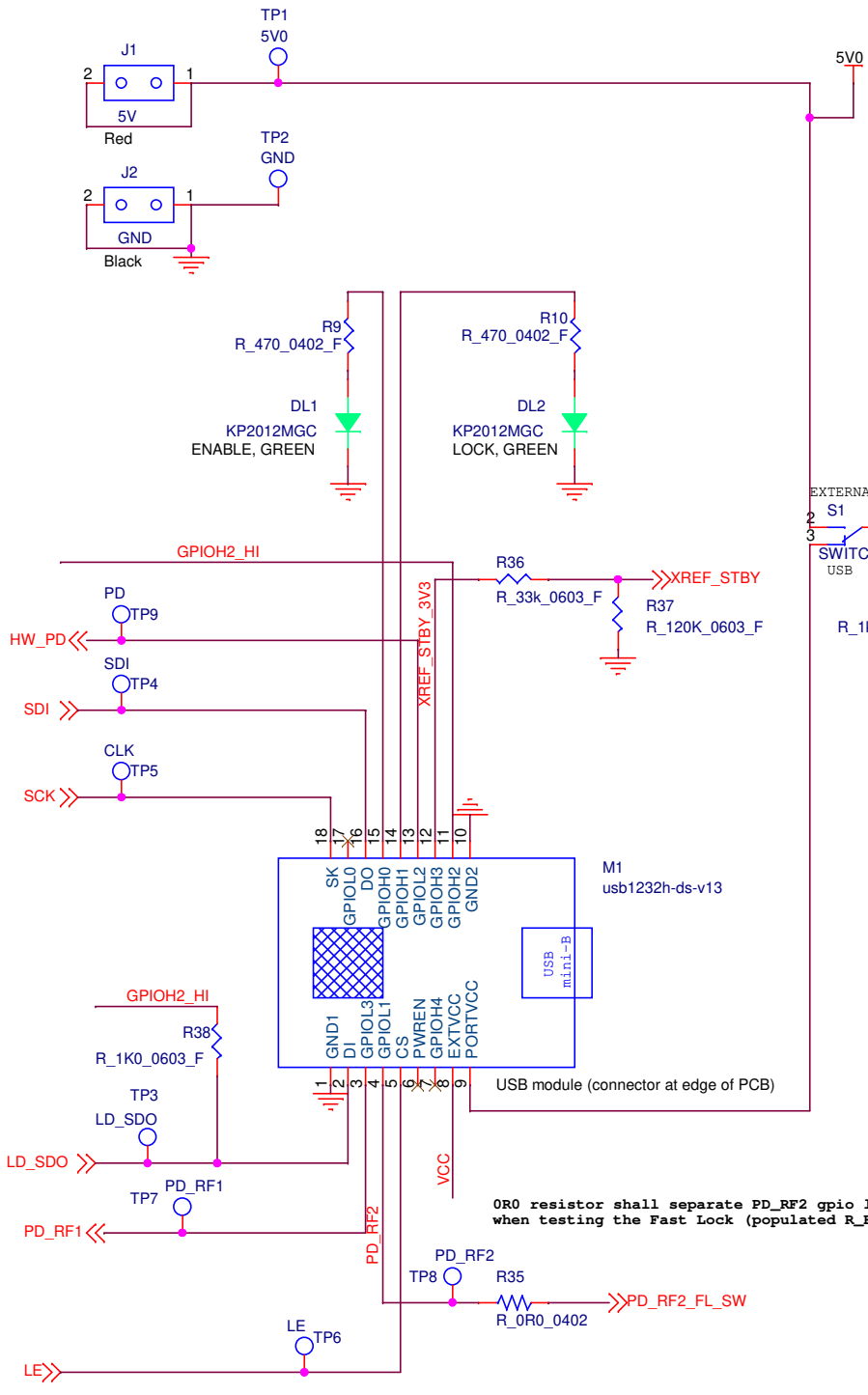


CPFS datasheet ->
 --> "no connection to pad 1 enables oscillator output"

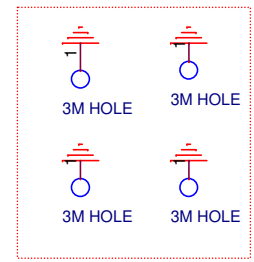
		Board Title		STUW81300_EVB_SCHEMATICS	
		Sheet Title		STUW81300 SIGNALS	
Doc No	Date	September 14, 2015	Rev	C	Sheet 1 / 3



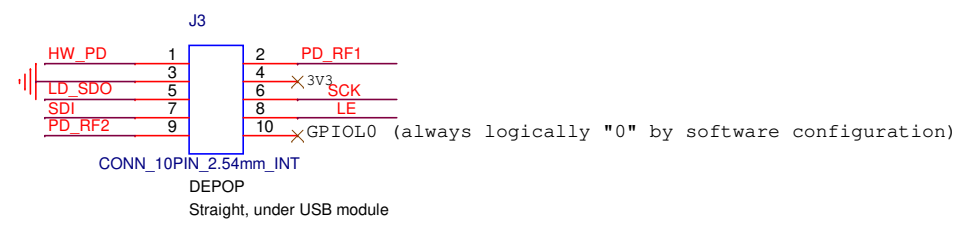
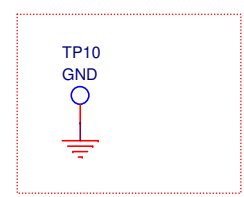
 life.augmented	Board Title STUW81300_EVB_SCHEMATICS				
	Sheet Title STuW81300 POWER				
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					2 / 3




PTH HOLES



GND TEST POINTS



0R0 resistor shall separate PD_RF2 gpio line from FL_SW net when testing the Fast Lock (populated R_FL1)

 life.augmented	Board Title	STUW81300_EVB_SCHEMATICS			
	Sheet Title	STuW81300 INTERFACE			
	Doc No	Date	September 14, 2015	Rev	Sheet
			C	3 / 3	