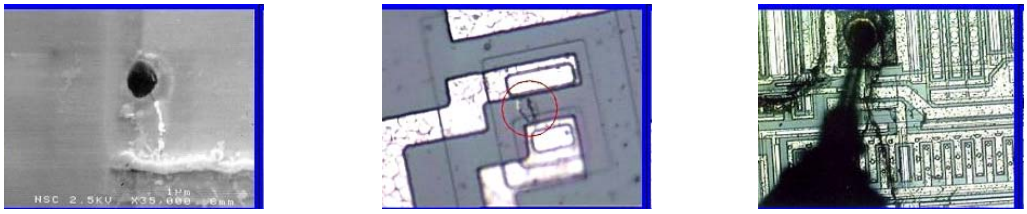
ESD protection improvement in cellular handsets

1 Need for ESD protection

As the wireless market continues to evolve, the next mobile phone generation requires increased functionality with new features like cameras, storage memory cards, FM radio, etc… To integrate such functions, the up-coming chipset generations must use the most advanced and thinnest lithographic technologies. As a result, ESD phenomena is getting more prominent for new circuit generation and is still considered as a major problem in high integration electronic systems.

As shown in *Figure 1*, an ESD event can easily destroy an IC in several ways, resulting in one or more of these attributes: junction leakage, short circuits, or burn-out, dielectric rupture, resistor-metal interface rupture, resistor/metal fusing, etc…

Figure 1. ESD discharge effect on silicon



Oxide fusing point | Metallic junction damage | Metallization damage

These are the reasons why current IC suppliers still recommend designing ESD protection devices to protect main chipsets. However, mainly driven by compact design trend, the implementation of external ESD protection will pose several challenges. Basically designers require a device with the highest level of ESD protection in the smallest possible size. At the same time the protection device must not effect digital and analog signal quality.

STMicroelectronics is introducing a new high performance protection solution of micro packaged ESD diodes, designed for single line or dual line protection of voltage sensitive electronic system.

2 Dual clamping feature

While current single line protection uses one diode to suppress ESD discharge, the dual clamping concept consists of two parallel diodes in the same package.

Figure 2. Dual clamping diode concept versus single ESD protection

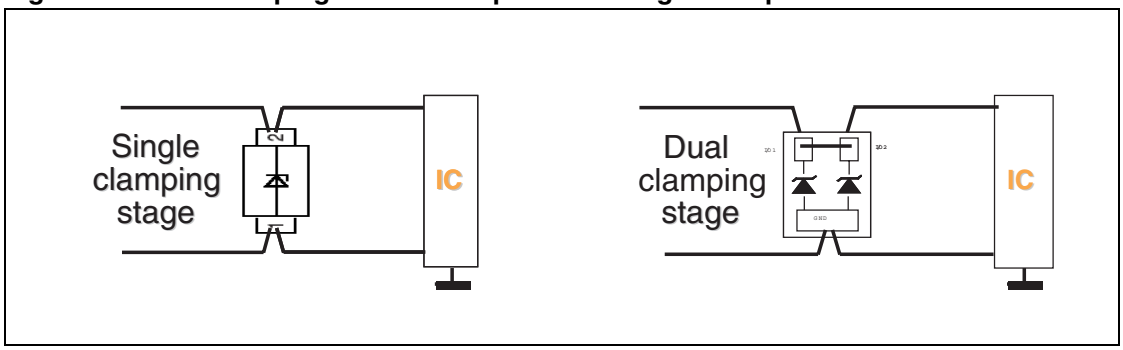


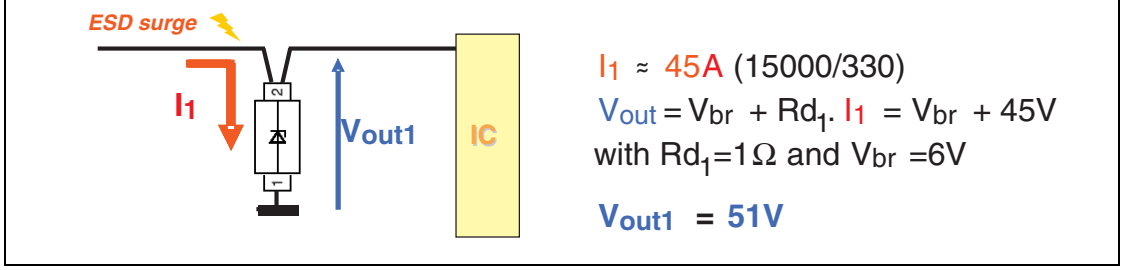
Figure 2 shows the internal structure of the dual clamping concept consists of two unidirectional diodes diffused at the same time in silicon. In comparison with current topology using single ESD diode, the dual clamping voltage solution allows better protection from ESD discharge.

3 Improved ESD protection

This innovative dual clamping feature can bring much better ESD immunity compared to all current single ESD protection diodes. When an ESD discharge is applied at the input of the device, two clamping stages ensure minimal remaining output voltage value across the IC.

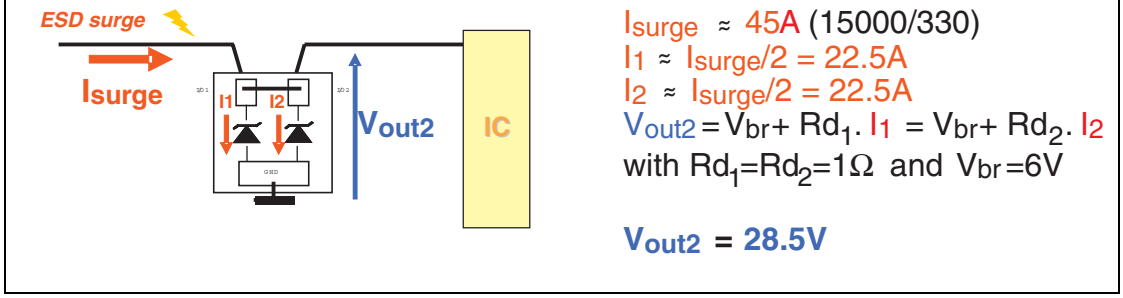
Figure 3 shows an evaluation of the remaining output voltage value when an ESD discharge is applied on single diode topology.

Figure 3. Output voltage when surge applied to single diode topology



Using single diode ESD topology, the IC, which has to be protected against ESD discharge, is exposed to V_{out1} (remaining output voltage) around 50 Volts for a short period. Dual clamping topology will bring much more ESD protection under the same test condition.

Figure 4. Output voltage when surge applied to dual clamping topology



The evaluation in *Figure 4* shows that with two parallel diodes, the remaining output voltage is reduced by **45%** compared to the single diode ESD protection solution. In this case, the value of V_{out} is **28** Volts instead of 51 Volts.

The lowest remaining voltage value reduces ESD damage risks, limits energy levels through the core chipset and also avoids any uncontrolled latch up effect.

This kind of topology can be used instead of multi-layer varistor solutions, while maintaining the small-size advantage. In this case, the maximum clamping voltage is reduced by at least 50% compared to varistor solutions while still providing a superior protection level.

Another advantage offered by a silicon solution is the protection reliability. This solution can withstand multiple ESD strikes without any shift in electrical characteristics.

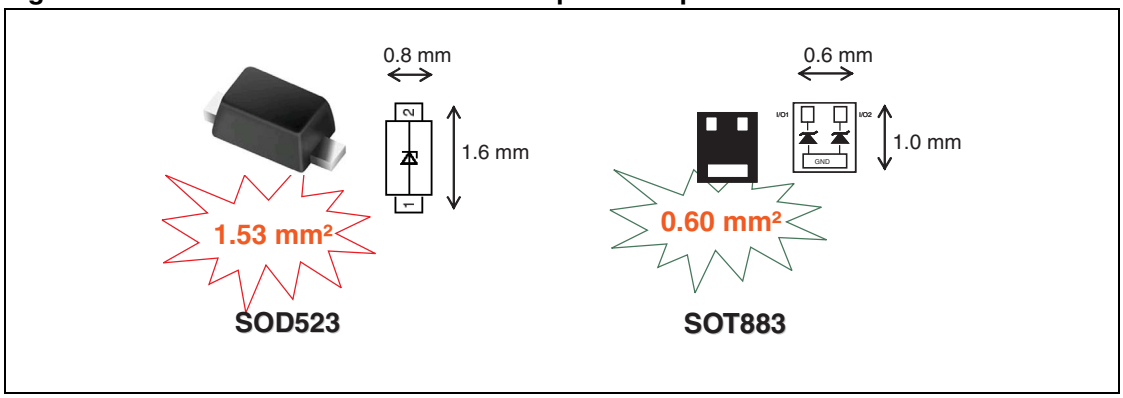
In conclusion, this topology is one of the best ESD protection solutions that complies with the most severe level of IEC61000-4-2 standard (level 4, 15Kv air discharge).

4 PCB space minimization

In comparison with the current single ESD diode protection packed in SOD523, this new highly integrated design in SOT883 provides up to 60% board space savings.

Figure 5 below compares the main package dimensions of SOD523 and SOT883. Besides the more efficient ESD protection using the dual diode concept in SOT883, designers have the added benefit of saving space on the PCB.

Figure 5. The new SOT883 saves 60% of space compared to the current SOD523



The line integration ratio (PCB space/number of lines) of around 0.3 mm^2 per line for the SOT883, is even smaller than 0402 SMD package or the famous SOD523. No other solutions in the current market can provide better integration performance.

5 High speed data compatibility

To avoid disruption of the analog or digital signals, the ESD protection has to be optimized for line capacitance value. In the case of the SOT883 solution, even if the total line capacitance of the device is the sum of the two parallel diode capacitances, the value is still one of the smallest available in the market with 24 pF at 0 Volt. That is, 12 pF per diode.

This results in extremely low impact on the rise and fall times of the signal and no delays.

Figure 6. 40Mhz data transmission test using high and low cap ESD protections

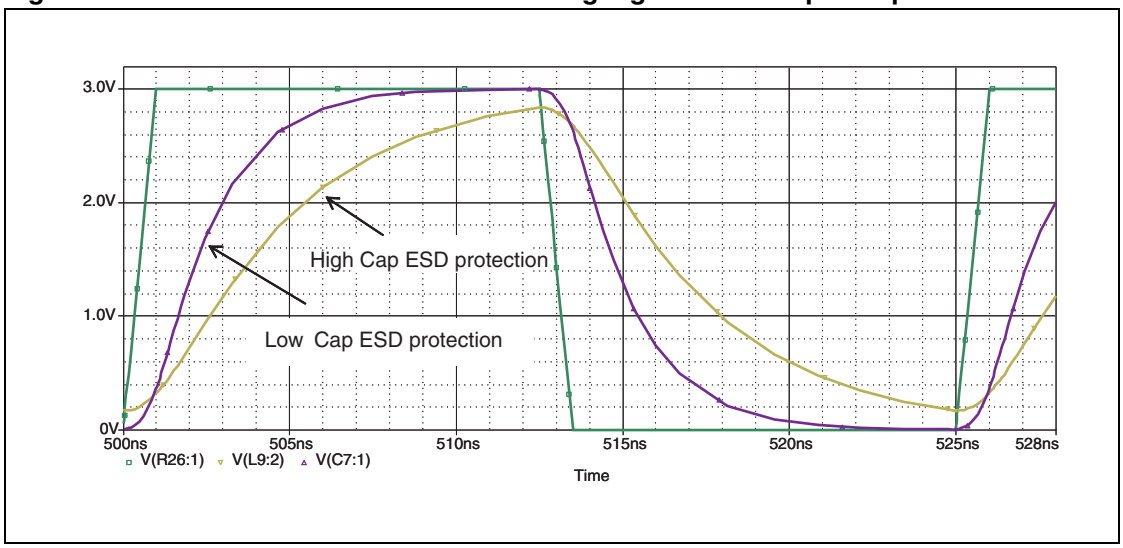
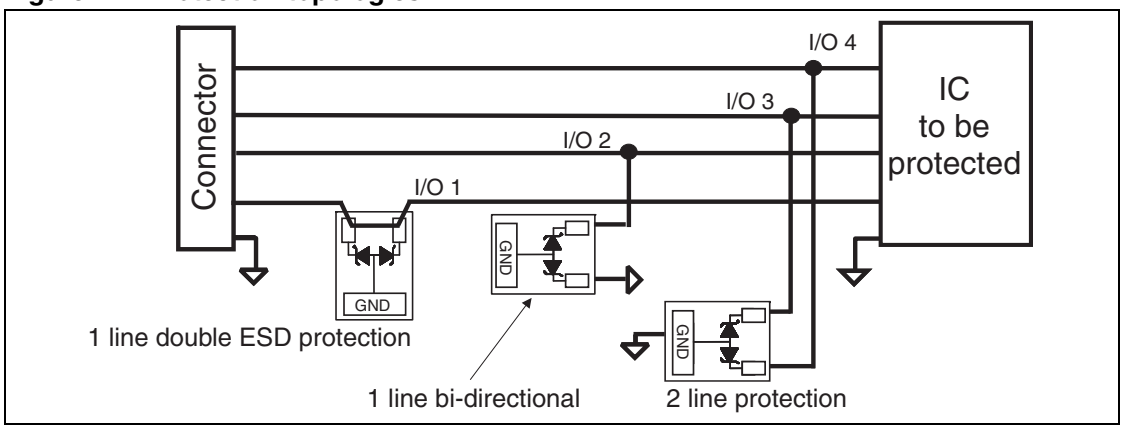


Figure 6 presents a 3,0 Volts signal transmission test at 40 Mhz through a low capacitance ESD protection structure in comparison with a higher capacitance structure. It can be seen that the high capacitance structure has a delay time of 5 to 6 times longer than the low cap structure. In the case of the high capacitance structure, the signal output voltage might not be received correctly.

6 DESIGN FLEXIBILITY

The dual line configuration in the SOT883 package can be used for three different protection topologies: as single, or dual line ESD unidirectional protection, or single line ESD bidirectional protection.

Figure 7. Protection topologies



In addition to the space saving benefit and excellent ESD performance, the use of the SOT883 also optimizes the BOM count.

7 Conclusion

The new STM dual clamping ESD protection concept in SOT883 is the best alternative. It ensures high ESD protection while providing space reduction benefits and design flexibility. In addition, the low capacitance silicon structure can be used for all interfaces, even for high speed signals without any risk of signal perturbation. For more information, please visit www.st.com website.

8 Revision history

Date	Revision	Changes
01-Dec-2005	1	Initial release.