Thermally aware high-power inverter board for battery-powered applications

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Abstract

The growth of battery powered applications is presenting new challenges for designers of electronic motor-driven solutions. Targeting higher performance and efficiency, the power stages of these products must manage high currents while meeting strict power dissipation and size requirements.

The STMicroelectronics STDRIVE101, a 75 V triple half-bridge gate driver with protections provided in a quad flat no-lead (QFN) 4x4 mm package, is a perfect fit for battery powered solutions.

This document illustrates a thermally aware workflow for the design of STDRIVE101 evaluation board, the EVALSTDRIVE101.

Detailed electro-thermal co-simulations using Cadence® Celsius™ Thermal Solver during routing phase of EVALSTDRIVE101 evaluation board enabled the designer to achieve maximum system performance in a short timeframe.

The result is an inverter capable of driving up to 15 A_{rms} current that can be referenced by the final application designers.

Introduction

There has recently been an unprecedented growth in the use of batteries for motor control applications as proven by the massive conversion from AC supply of many appliances like vacuum cleaners or power tools as well as the expanding demand of electric scooters and e-bikes for green mobility.

Battery-powered motor control solutions pose several challenges from a design perspective such as the optimization of printed circuit board (PCB) thermal performance.

The use of batteries for application power supplies requires lower operating voltage, usually in the range of a few tens of volts, due to the limited number of battery cells connected in a series. When applications require high power above hundreds of watts, the management of currents flowing through the motor driving electronics becomes critical to ensure overall system efficiency and reliability. Indeed, motor currents may exceed tens of amperes in such applications, which leads to increased power dissipation inside the inverter module, reducing its efficiency. More power to the electronic components of the inverter also results in higher temperatures, which could consequently degrade their performance over time and/or cause sudden breaks if going above maximum allowed ratings.

Several electronic components widely used in motor control systems are very sensitive to operating ambient temperature. For example, electrolytic capacitors typically used to stabilize the main supply voltage of the inverter are guaranteed by the manufacturer for a minimum number of hours without failures if their temperature remains below specific thresholds, but if operated above the threshold a reduction of their average life should be expected.

For all these reasons, the optimization of thermal performance, in combination with a compact form factor, is a key aspect of the inverter design phase that might hide pitfalls if not properly addressed.

The current density in the PCB is also a critical factor, in particular when the current flows between different planes through via holes. Overstressing a single via connection due to poor placement could result in a sudden failure during operation, making analysis of this issue critical as well.

A transitional approach to this problem would be the production of a first prototype once electrical signoff is completed and a direct check of its thermal performance by on-field validation. The design would then be successively refined, and new prototypes evaluated again in an iterative loop that should converge to the optimal result. The problems of this approach are that electrical and thermal evaluations are totally separated, and electrical-thermal coupling effects are never addressed during PCB design. This results in a long iteration time that directly impacts the time to market.

A more effective alternative method is to optimize the electro-thermal performance of motor control systems by taking advantage of modern simulation technologies. The Cadence® Celsius™ Thermal Solver, industry-leading electrical-thermal co-simulation software for system analysis, is able to provide in just a few minutes a global and accurate assessment of design performance from both an electrical and thermal perspective. This tool dramatically simplifies the inverter optimization process and enables designers to achieve a compact and reliable design in a short timeframe.

STMicroelectronics, leading manufacturer of industrial motor control integrated circuits (ICs), fine-tuned its EVALSTDRIVE101 evaluation board using the Celsius Thermal Solver. The board includes a compact power stage of 50 cm^2, which can deliver over 1 kW power and 15 A_{rms} current to the motor without heatsink or additional cooling.

This work presents a methodology with hints and warnings to help electronic designers of high-power and low voltage inverters reducing the effort usually needed for thermal optimization of designs and reach their market in shorter time. This is done taking the opportunity to describe the workflow that allowed to put in production the EVALSTDRIVE101.

After a brief introduction of the board, an estimation of power losses in the inverter is presented to properly set up the thermal solver. Electro-thermal simulations of final design are detailed that resulted after successive layout refinements. Finally, the EVALSTDRIVE101 experimental validation is presented, proving both the outstanding performance of the board and the effectiveness of the Celsius Thermal Solver in simplifying the development process.

1 EVALSTDRIVE101 description

The EVALSTDRIVE101 is a demonstration board designed to drive three-phase brushless motors, Figure 1. It is based on the STDRIVE101 three-phase gate driver, and six STL110N10F7 power MOSFETs, arranged into three half-bridges. The block diagram of the EVALSTDRIVE101 is represented in Figure 2.

The board can be used in single shunt or three-shunt sensing topology and can support both Field Oriented Control (FOC) and six-step algorithms. Three operational amplifiers present on-board are used to condition the signal of the shunt resistors, for a precise differential current measurement. The on-board Hall sensors connector, and the phase voltage sensing network enable the implementation of both sensor-based and sensor-less algorithms for motion control.

The EVALSTDRIVE101 can be interfaced with different STM32 microcontroller evaluation boards, allowing a full evaluation of the STDRIVE101 features, including the embedded comparator and the drain-source voltage monitoring of each power MOSFET for overcurrent protection.

Figure 1. EVALSTDRIVE101 demonstration board

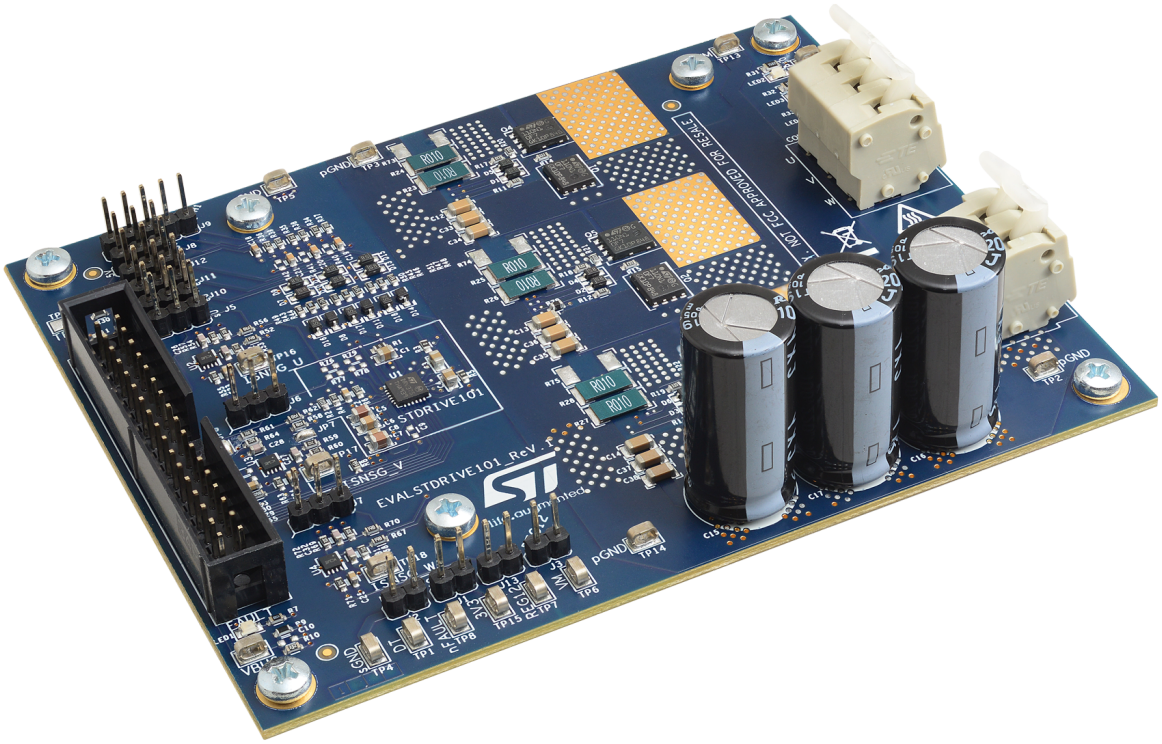
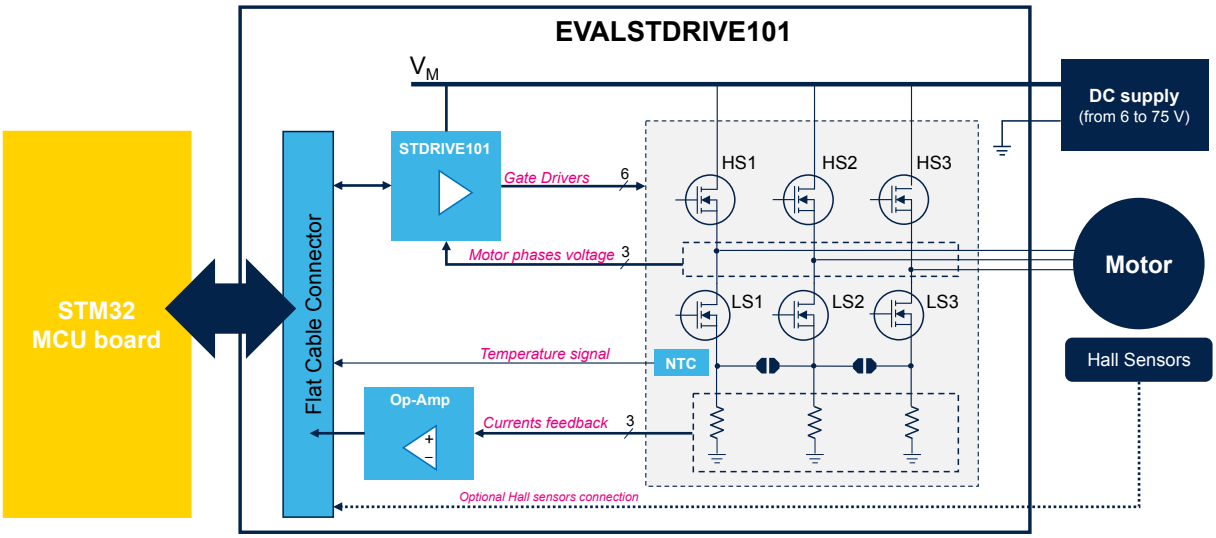


Figure 2. **EVALSTDRIVE101 basic block diagram**



The EVALSTDRIVE101 is a four-layer board with 2 oz copper, width of 11.4 cm and height of 9 cm. Although the board is provided with a custom aluminum heatsink for operations up to 20 A_{rms}, this document addresses operations without heatsink. In this case a maximum power of roughly 1 kW can be delivered to the load with 15 A_{rms} output current and supply voltage of 75 V. In the following the maximum current rating was considered but the supply voltage was scaled down to 36 V fitting better with battery powered scenarios.

From a thermal perspective, the most critical part of the EVALSTDRIVE101, is the power stage area that mainly includes power MOSFETs, shunt resistors, ceramic bypass capacitors, electrolytic bulk capacitors and connectors. The layout of this part of the board can be seen from Figure 3 to Figure 6 and covers roughly half of overall PCB size, i.e. 50 cm^2. Special care was paid in the placement and routing of MOSFETs since these components are responsible for most of power losses during inverter operations. The MOSFET drain terminal corresponds to the exposed pad of the package and provides the main link to silicon substrate for heat dissipation. Consequently, the PCB copper area of all drain terminals was maximized on the top layer as evident from Figure 3 focusing on the VM bus and the three output nets (OUTU, OUTV and OUTW). Copper areas of the VM and outputs as available on the top layer were replicated and enlarged where possible for other layers to improve heat transmission toward the bottom board surface (from Figure 4 to Figure 6). In this way both top and bottom surfaces of the board effectively contribute to heat dissipation by natural convection and radiation. Electrical and thermal connection among different layers is provided by vias of 0.5 mm diameter that facilitate air flow and improve PCB cooling. Grids of vias were located right below the MOSFETs' exposed pads but their diameter was reduced to 0.3 mm to prevent solder paste reflows in the holes.

Aside from thermal perspective, the PCB routing also optimizes electrical performance. With reference to lower panel of Figure 7 showing a placement detail of one half-bridge, the MOSFETs, shunt resistors and ceramic capacitors were placed close each other to minimize current loops and were connected by large top traces to reduce inductive and resistive components positively affecting radiated emission and noise level. The same reduction of parasitic was implemented for connections between STDRIVE101 gate driver and MOSFETs using incremented width of 0.7 mm and two vias for each crossing of layers. This, together with a tuned polarization network of MOSFET gates made by a 33 Ω resistor in parallel with a Schottky diode as shown in the upper panel of Figure 7, also allowed the designer to keep under control induced turn on effects and finally get the best out of motor control.

Figure 3. **EVALSTDRIVE101 top layer PCB**

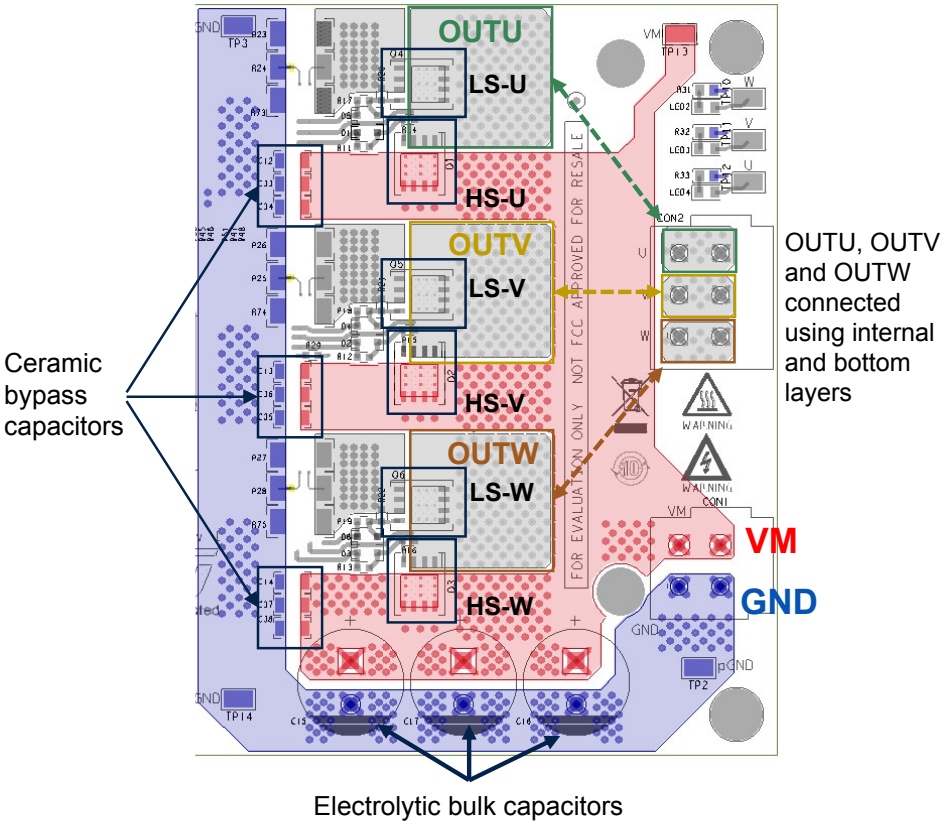


Figure 4. **EVALSTDRIVE101 1st inner layer PCB**

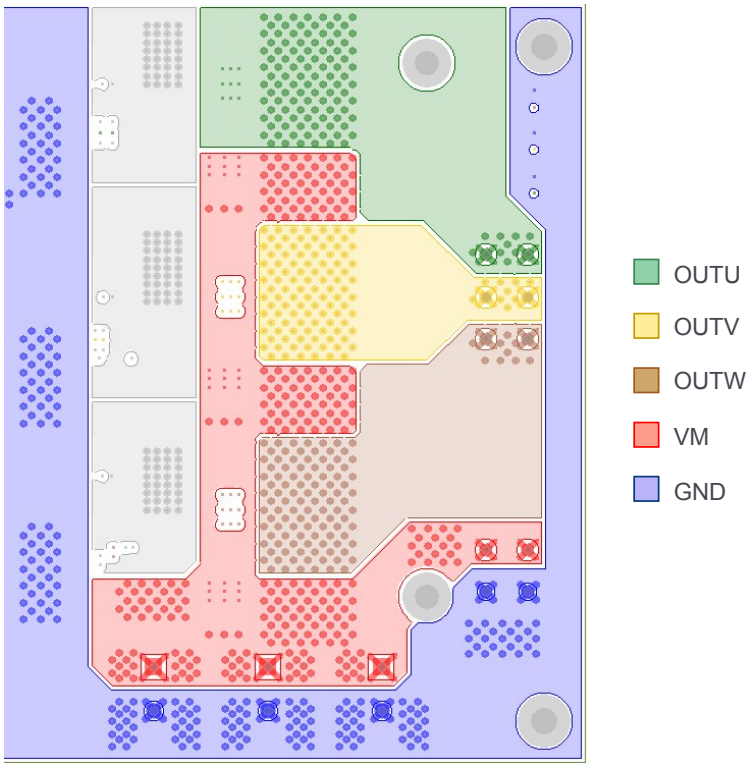


Figure 5. EVALSTDRIVE101 2nd inner layer PCB

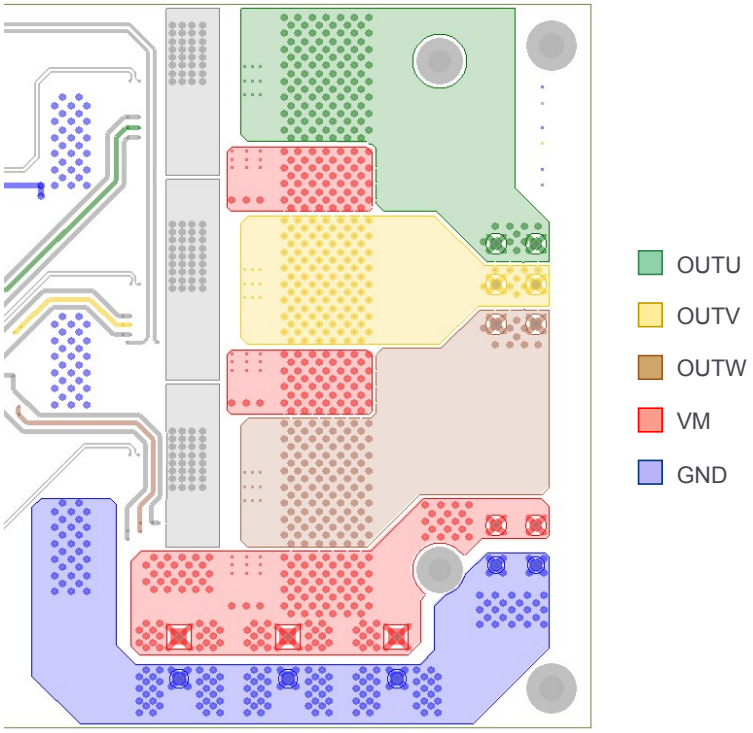


Figure 6. EVALSTDRIVE101 bottom layer PCB

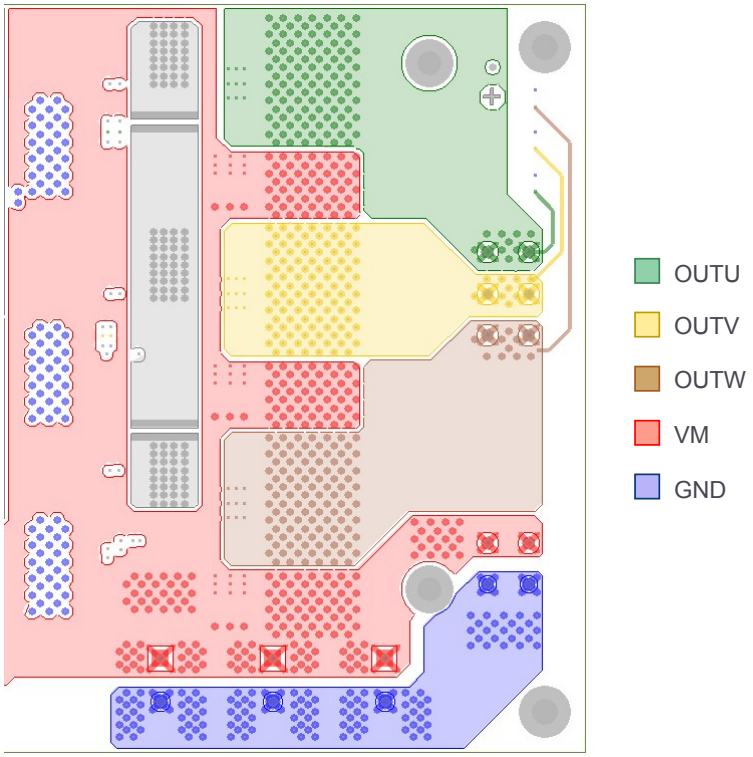
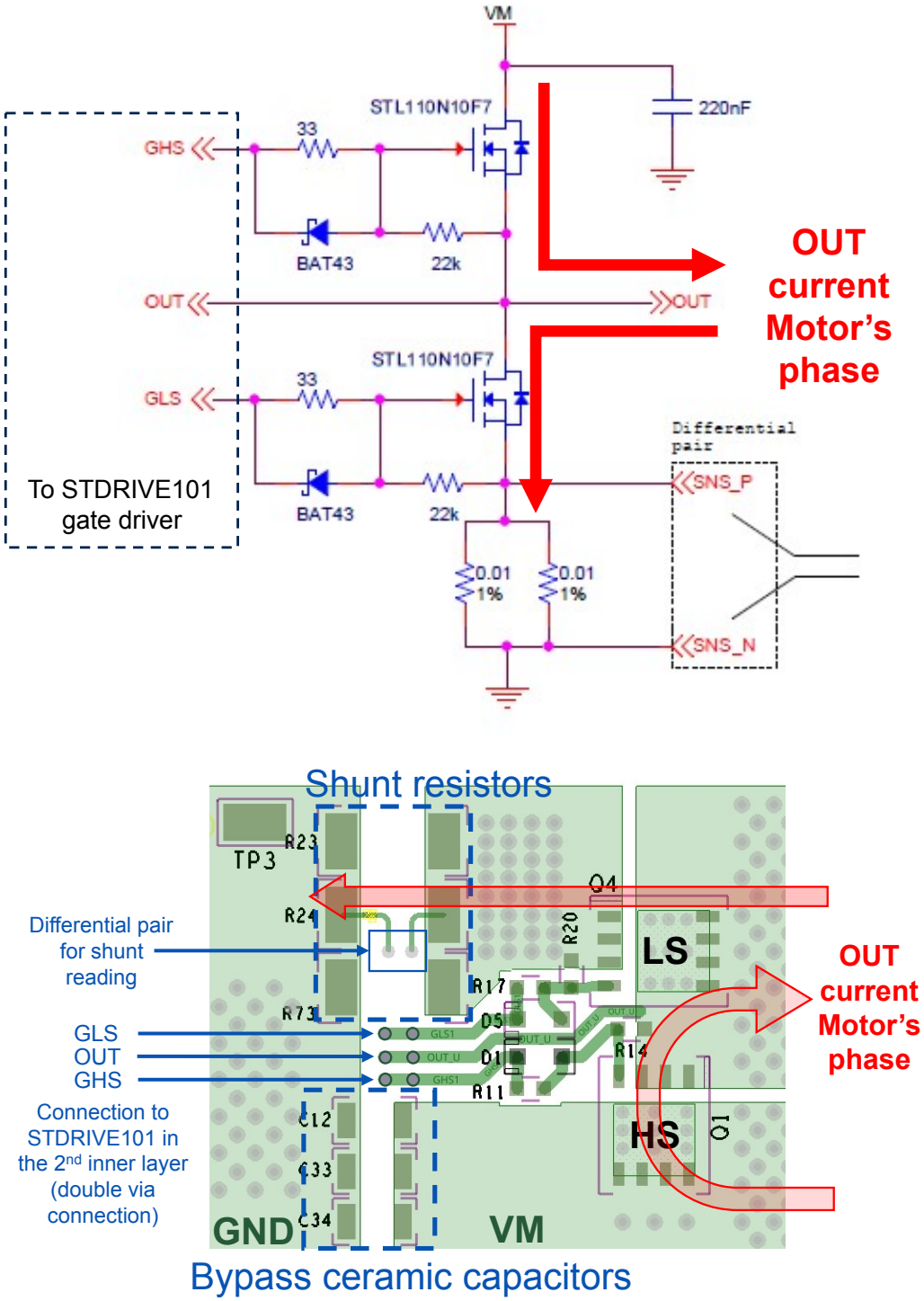


Figure 7. **Schematic of one half-bridge in the EVALSTDRIVE101 and associated layout pattern**



2 Estimate of power losses

It is important to correctly estimate the power dissipated by the inverter during its operation. This estimate is one of the inputs for the thermal simulator and allows the designer to quantify board efficiency in the power transfer to the load. Different methods can be used to quantify power losses of the system during design phase, one of which is the use of a circuit simulator. This tool enables the designer to obtain very accurate results but requires simulation models for the components that are not always available from the manufacturer, especially for newly released products. On the other hand, the implementation of such models by scratch can be difficult and error prone for non-experts in the field, and in some cases not feasible at all due to lack of modeling data for the component. For these reasons board designers may leverage alternative methods that allow them to obtain a reasonable estimate of the power losses, though with approximations.

The inverter losses can be split in two contributions: those due to PCB traces and those due to electronic components.

2.1 PCB trace losses

The losses of PCB traces are due to Joule effect dissipation when high currents pass through the finite resistance of core metal, usually copper, and its plating, for example, gold. The value of these losses can be expressed through the well-known equation:

Equation 1

$$P = R \cdot I^2 = \rho \frac{l}{w \cdot t} \cdot I^2 \quad (1)$$

- R is the resistance of the trace
- I is the current flowing through the trace
- ρ is the resistivity of trace metal
- l is the length of the trace
- $w \cdot t$, trace width by metal thickness, is the cross-section area of the trace

While the formula is simple, quantifying these losses might not be. Shapes of traces are often so complex that they cannot be simply described by the above formula, even when dividing each trace into smaller elementary segments. Currents in these geometries become unequally distributed alongside the path and a spreading occurs with higher current density inside lower resistance regions or in proximity to connectors and components that affect the overall resistance of the trace. This phenomenon is then exacerbated using multiple layers interconnected with vias for current distribution.

The Celsius Thermal Solver overcomes this roadblock by precisely computing the current densities and PCB losses from layout data.

2.2 Component losses

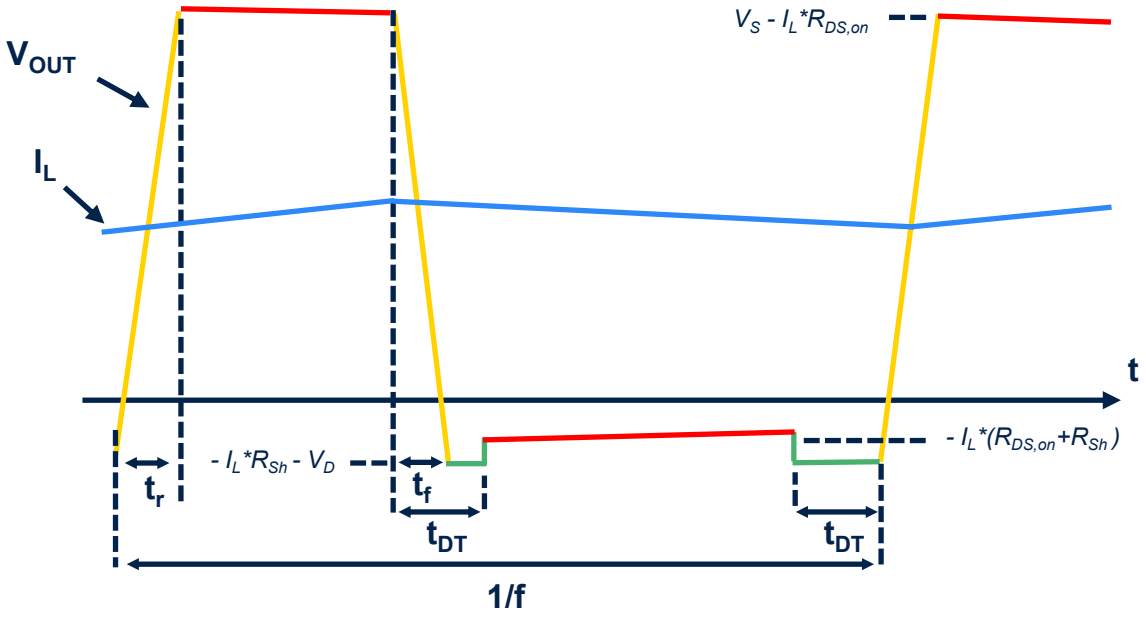
The losses due to electronic components can be evaluated using simplified formulae. Power dissipation of the inverter is dominated by losses inside MOSFETs and shunt resistors, and these are analyzed below, leaving out secondary phenomena such as dissipation for voltage ripple on the equivalent series resistance (ESR) of the capacitors [2] or soldering defects [3].

The two MOSFETs of each half-bridge are turned on in a complementary way, connecting the output node towards the supply bus (high-side MOSFET) or ground (low-side MOSFET), as shown in Figure 8.

The turning on of one MOSFET is delayed with respect to the complementary MOSFET turning off: this delay is called deadtime. The deadtime prevents cross-conduction anomalies, where both MOSFETs are simultaneously turned on at every switching edge, causing additional power dissipation and potentially leading to component damage.

MOSFET losses are by conduction, switching, and the diode drop occurring during the red, yellow and green intervals of Figure 8.

Figure 8. Commutation of the half-bridge



To obtain a proper spinning of the brush-less motor, a control system is typically needed to impose a certain modulation scheme for turning on and off the three half bridges. Several modulations are available for modern high performance motor driving solutions, which may differently affect power losses in the inverter. In the following the sinusoidal pulse width modulation (S-PWM) was considered. In S-PWM three sinusoids are generated on inverter outputs having 120° phase shift and average duty cycle of 50%. Conversely to other modulations such as trapezoidal driving or space vector modulation with discontinuous PWM, the S-PWM provides balanced power loss among the six power MOSFETs.

2.3 MOSFET conduction

Conduction losses occur when a MOSFET is turned on and are due to its channel resistance. The time each MOSFET is turned on or off depends on duty cycle of the generated PWM however their sum is constant. Since the two MOSFETs are nominally equal, the overall conduction loss for the half-bridge can be computed by:

Equation 2

$$P_{cond} \sim R_{DS,on} \cdot I_L^2 \cdot \left(1 - 2 \cdot t_{DT} \cdot f\right) \quad (2)$$

- $R_{DS,on}$ is the drain-source on resistance of the MOSFET
- I_L is the RMS value of the output current
- t_{DT} is the dead time
- f is the switching frequency of the half-bridge

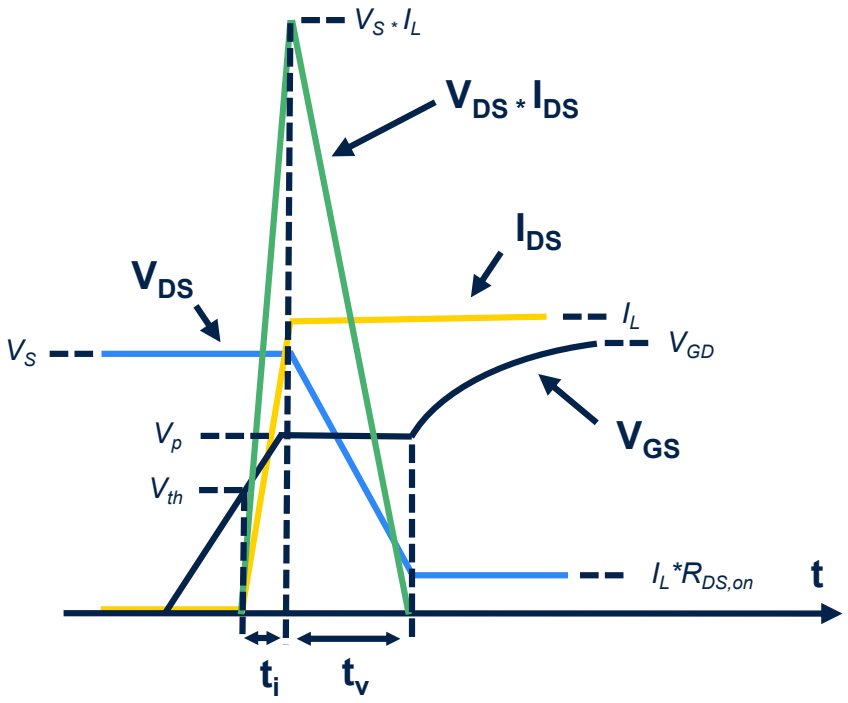
Using Eq. (2) with a value for the channel resistance of 5 mΩ, a switching frequency of 20 kHz, dead time of 500 ns, and current of 15 A_{rms}, the conduction losses for each MOSFET are roughly 551 mW.

2.4 MOSFET switching

Switching losses occur during the time needed to pull the output node high to the supply voltage or low to ground. The MOSFETs of the half-bridge can operate in two different modes: hard switching and soft switching. When the half-bridge sources the current, the high side works in hard switching and the low side in soft switching. Only the turning on/off of the high-side is critical from a power dissipation point of view, as this MOSFET must actively bring the output node up and down conversely to the low side. The two roles are flipped when the half-bridge sinks the current, thus the two MOSFETs operate in hard switching for half of the time because the currents change sign regularly in S-PWM.

Figure 9 shows a simplified version of voltage and current of the MOSFET during hard switching. The MOSFET turns on when the gate voltage exceeds the threshold voltage then its current increases up to the output current value while its drain-source voltage remains constant to the supply voltage. From this point on the gate voltage, namely the Miller plateau region, does not change, while drain-source voltage decreases. In the final part of the sequence, the gate voltage increases, and the channel resistance decreases accordingly up to its final value.

Figure 9. MOSFET commutation of voltage and current during hard switching



Because of the triangular shape for the dissipated energy, the power losses of one commutation edge can be evaluated by:

Equation 3

$$P_{sw} = E_{sw} \cdot f \sim \frac{V_S \cdot I_L \cdot (t_i + t_v)}{2} \cdot f \quad (3)$$

- E_{sw} is the energy dissipated during one commutation
- V_S is the supply voltage of power stage
- I_L is the RMS value of the output current
- t_i is the time needed for the MOSFET current to equal I_L
- t_v is the time needed to toggle the output voltage
- f is the switching frequency of the half-bridge

The t_v time corresponds to the duration of Miller plateau, i.e., the rise/fall time during the hard switching commutation. The EVALSTDRIVE101 is characterized by different times for positive and negative switching edges in the PWM cycle, as the gate of each MOSFET is connected to the gate driver through one resistor in parallel to one diode. The MOSFET is turned on by charging the gate capacitance through the resistor and switched off by discharging the gate through the diode. The following equation can be used to calculate the switching times:

Equation 4

$$t_r \sim \frac{Q_p \cdot R_G}{V_{GD} - V_p};\ t_f \sim \frac{Q_p}{I_p} \tag{4}$$

- Q_p is the charge to perform Miller plateau
- V_{GD} is the gate driver supply voltage
- V_p is the MOSFET gate voltage during plateau region
- R_G is the turning on gate resistance between MOSFET and gate driver
- I_p is the sink gate current during plateau region

The values of Q_p charge and V_p voltage can be found in the MOSFET datasheet for certain values of drain voltage and current, in this case roughly 18 nC and 6 V respectively for the STL110N10F7.

Using Eq. (4), the two switching times are 100 ns and 30 ns with V_{GD} of 12 V, R_G of 33 Ω, and I_p of 600 mA corresponding to the maximum current capability of the STDRIVE101.

The t_i times during turn on t_{ir} and turn off t_{if} of the MOSFET can be estimated using the following equation:

Equation 5

$$t_{ir} \sim R_G \cdot C_{iss} \cdot ln\left(\frac{V_{GD} - V_{th}}{V_{GD} - V_p}\right);\ t_{if} \sim \frac{C_{iss} \cdot \left(V_p - V_{th}\right)}{I_p} \tag{5}$$

- R_G is the turning on gate resistance between MOSFET and gate driver
- C_{iss} is the MOSFET input capacitance
- V_{GD} is the gate driver supply voltage
- V_{th} is the MOSFET turn on voltage threshold
- V_p is the MOSFET gate voltage during plateau region
- I_p is the sink gate current during plateau region

Using Eq. (5) the two times are 68 ns and 26 ns with C_{iss} of 5117 pF and V_{th} of 3 V.

Finally, a dissipation of 602 mW for each MOSFET is obtained using Eq. (3) with V_S of 36 V, I_L of 15 A, f of 20 kHz.

2.5 Diode drop

During dead time the output current flows through the body diode of one MOSFET. When the current is flowing out from the half-bridge it circulates through the low-side diode and shunt resistor toward the ground plain, while it circulates inside the high-side diode toward the supply rail during the opposite case. Half-bridge power losses for dead time can be evaluated by following equation:

Equation 6

$$P_{DT} \sim V_D \cdot I_L \cdot 2 \cdot t_{DT} \cdot f \tag{6}$$

- V_D is the diode forward voltage
- I_L is the RMS value of the output current
- t_{DT} is the dead time
- f is the switching frequency of the half-bridge

The formula provides a slight overestimate since the dead time also includes the output switching time when the diode is not yet turned on.

Using Eq. (6), each MOSFET dissipates 150 mW with V_D of 1 V, t_{DT} of 500 ns, and f of 20 kHz.

2.6 Shunt resistor

The EVALSTDRIVE101 board implements a three-shunt current sensing where the source terminal of each low-side MOSFET is connected to one resistor. In this topology the current flowing through the shunt resistor always corresponds to that of the associated low-side MOSFET, which is on average the output current multiplied by the square root of the PWM duty cycle. Therefore, the power loss of the shunt resistor can be computed as:

Equation 7

$$P_{sh} = \frac{R_{sh} \cdot I_L^2}{2} \quad (7)$$

- R_{sh} is the shunt resistance
- I_L is the RMS value of the output current

Each shunt resistor dissipates 562 mW using Eq. (7), with R_{sh} of 5 mΩ and I_L of 15 A_{rms}.

3 Celsius Thermal Solver simulations

The Celsius Thermal Solver is the first complete electrical-thermal co-simulation solution for the full hierarchy of electronic systems from ICs to physical enclosures. Based on a production-proven, massively parallel architecture that delivers up to 10 times faster performance than legacy solutions without sacrificing accuracy, the Celsius solver integrates with Cadence IC, package, and PCB implementation platforms. This enables new system analysis and design insights and empowers electrical design teams to detect and mitigate thermal issues early in the design process reducing electronic system development time.

By combining finite element analysis (FEA) for solid structures with computational fluid dynamics (CFD) for fluids, the Celsius Thermal Solver enables complete system analysis in a single tool. When using this tool for PCB and IC packaging, engineering teams can combine electrical and thermal analysis and simulate the flow of both electricity and heat for a more accurate system-level thermal simulation than legacy tools. In addition, the tool performs both static (steady-state) and dynamic (transient) electrical-thermal co-simulations based on the actual flow of electrical power in advanced 3D structures, providing visibility into real-world system behavior.

In addition to the heat generated locally around and underneath certain components at the PCB or IC package level due to component power consumption, the Celsius solver can calculate the heat generated by the Joule effect due to the high currents flowing through the copper from the voltage regulator to the sinks. Local increase of the current density at the PCB package level will also introduce a local increase of the temperature (local hotspots). This makes it ideal for applications like DC/DC converter PCB designs, switch mode power supply (SMPS) PCB designs, motor controlling applications, and any automotive and industrial types of applications dealing with high currents.

By empowering electronics design teams to analyze thermal issues early and share ownership of thermal analysis, the Celsius solver reduces design re-spins and enables new analysis and design insights not possible with legacy solutions. In addition, the tool accurately simulates large systems with detailed granularity for any object of interest and is the first solution capable of modeling structures as small as the IC and its power distribution together with structures as large as the chassis.

The Celsius solver allows designers to directly import PCB and IC PKG layout files (.brd, .mcm, .sip, odb++ formats), even in draft version. For example, a board like the EVALSTDRIVE101 which consists of digital, analog and power subdomains can be optimized in the inverter section even if other parts are not yet defined. This feature allows to get immediate feedback when designing PCB therefore it is possible to refine the layout step by step if critical issues are highlighted by simulations. This workflow was adopted to obtain the production-ready version of EVALSTDRIVE101 and involved an iterative work mainly made of changes in component placements, refinement of traces shapes and inclusion/removal of vias. It is not reported below the followed optimization procedure but rather the final outcome highlighting the potential of the tool.

3.1 Manufacturing information

The tool allows the designer to view and modify manufacturing parameters related to the PCB stackup and via characteristics like plating, thickness, and filler. As shown in Figure 10, the EVALSTDRIVE101 has an overall PCB thickness of 1.58 mm and consists of four copper layers that were optimized at 70 µm (2 oz / ft^2). Copper thickness affects not only the electrical resistance of PCB traces, as explained in previous section, but also their thermal resistance. A cross-section area of the traces can be increased with a greater copper thickness to dissipate less power for the Joule effect and to reduce thermal resistance and enable better heat spreading. However, copper thickness requires a tradeoff between performance versus PCB production cost and its minimization is deemed necessary.

Thanks to the stackup settings it is also possible to take into account production tolerances, usually 20% of nominal values, and simulate both in typical and worst-case condition to make the design even more robust. The physical properties of specified materials are automatically provided through the embedded library and their values are adapted according to operating conditions. Copper resistivity, for example, is increased with temperature in order to obtain better simulation results.

Figure 10. **EVALSTDRIVE101 stackup**

Layer #	Color	Layer Icon	Layer Name	Thickness(mm)	Material	Conductivity(S/m)	Fill-in Dielectric
1			Signal$TOP	0.07	copper		FR4
			Medium$41	0.25	FR4	0	
2			Signal$2INN	0.07	copper		FR4
			Medium$43	0.8	FR4	0	
3			Signal$3INN	0.07	copper		FR4
			Medium$45	0.25	FR4	0	
4			Signal$BOTTOM	0.07	copper		FR4

3.2 Electrical analysis

Critical points in the current flow that could produce board overstress can be identified. The Celsius Thermal Solver allows designers to perform simulations that also include an electrical analysis of the system that provides current densities in traces and vias, as well as voltage drops. These kinds of simulations require designers to define the PCB's current loops of interest using a circuit model for the system, made of current sinks, voltage sources, and resistances.

Current paths are not immediately defined for the inverter since these depend on operating condition of the three half-bridges. A full description of system behavior should include current exchange through the high-side or low-side MOSFET within one PWM cycle and account for realistic motor driving by amplitude modulation over time. However, it would be overdetailed and of little use for a simulation that is intended to address longer time-scale phenomena. A more convenient representation is proposed in Figure 11 for each half-bridge. It consists simply of two constant current generators placed between the output and power supply connectors and three short circuits modeling the MOSFETs and shunt resistor. The two current loops provide a good fitting with real case average currents throughout the supply rail and ground plain while the output path current is slightly oversized, a convenient operating condition for evaluating design robustness.

Figure 11. **PCB current loop modeling**

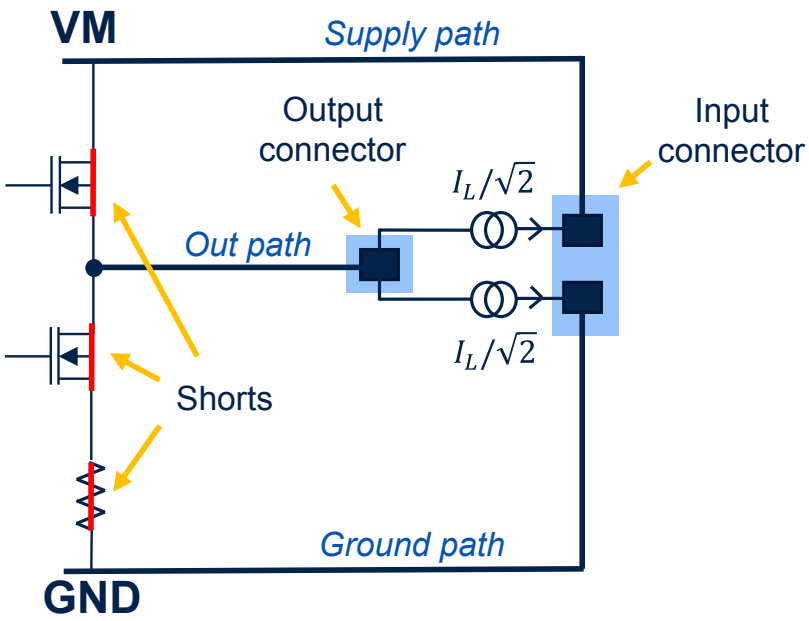
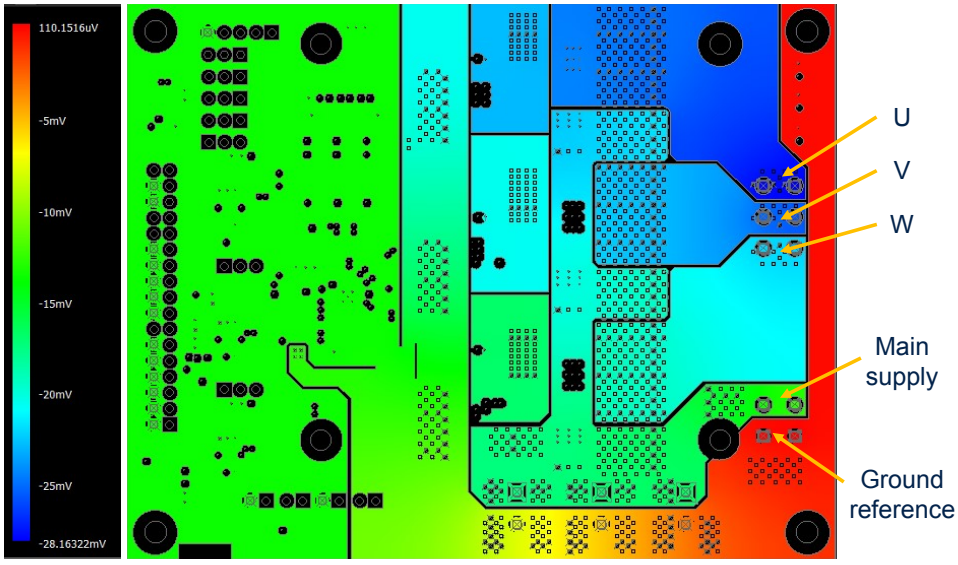


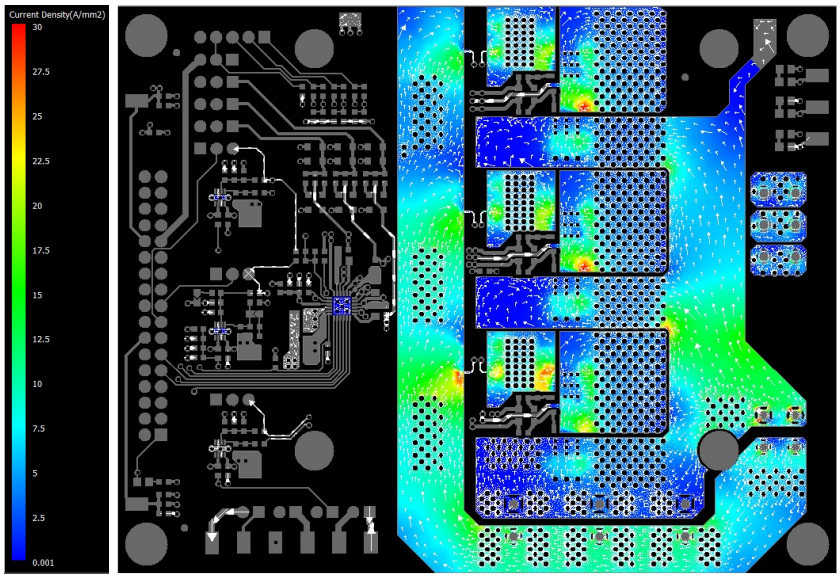
Figure 12 and Figure 13 show the voltage drops and current density of the EVALSTDRIVE101 with I_L of 15 A. Voltage drops simulated with the Celsius Thermal Solver with respect to ground reference highlight a particularly optimized layout with an absence of bottlenecks and well-balanced outputs at 28 mV, 25 mV, and 23 mV for U, V, and W. Output U shows the highest voltage drop while output W, the lowest of the three, that is an expected result considering relative path lengths from power connector.

Figure 12. Voltage drops resulting from DC current loops



The Celsius Thermal Solver analysis of current distributions also confirmed the board's targeted performance (Figure 13). The currents are well distributed in the various paths and have an average density below 15 A/mm^2, which is the recommended value for power traces sizing. Some red areas are highlighted in the proximity of the MOSFETs, the shunt resistors, and the connectors. These represent a higher current density, due to components' terminals smaller than the underlying power traces. However, the maximum current density is far below the limit of 50 A/mm^2, which could realistically lead to reliability issues [1].

Figure 13. Current density resulting from DC current loops



3.3 Thermal analysis

The Celsius Thermal Solver enables designers to set up and run steady-state or transient simulations. The former provides a single 2D temperature map for layers and components, while the latter provides maps for each simulated time instant and warmup curves at a cost of longer simulation time. Settings needed for steady-state simulation can be applied to a transient simulation, but this additionally requires a definition of power dissipation functions for the components. Transient simulations are suitable when defining different operating states for the system with power sources not simultaneously active and also to assess the time needed to reach steady-state temperature. Simulations were done at an ambient temperature of 28 °C with the heat transfer coefficient as boundary conditions and two-resistors thermal model for devices. These models were used instead of detailed thermal models like Delphi since directly available in components datasheets although slightly sacrificing the simulation accuracy [4].

Steady state results for the EVALSTDRIVE101 are provided in Figure 14 and transient simulation results in Figure 15. Step power functions are used in transient simulation to enable all the MOSEFTs and the shunt resistor at time zero.

Figure 14. Celsius Thermal Solver result: steady-state PCB simulated top layer temperature map

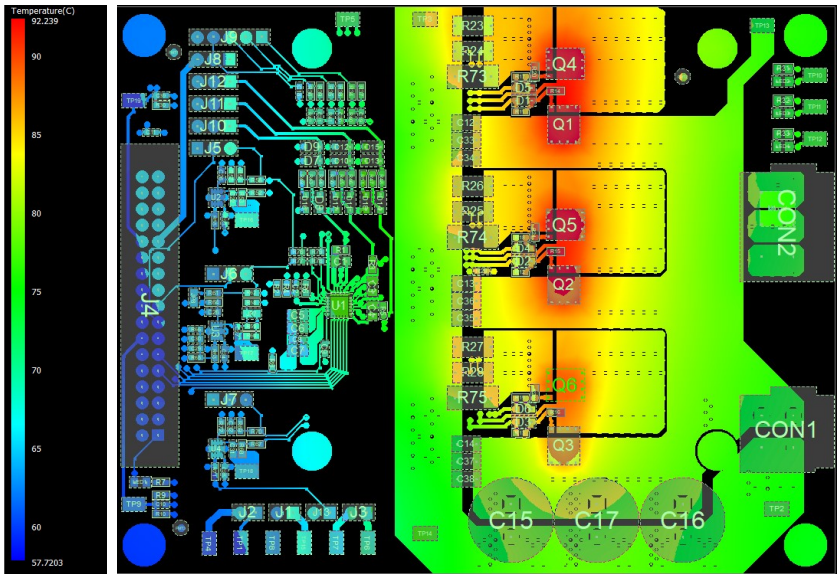
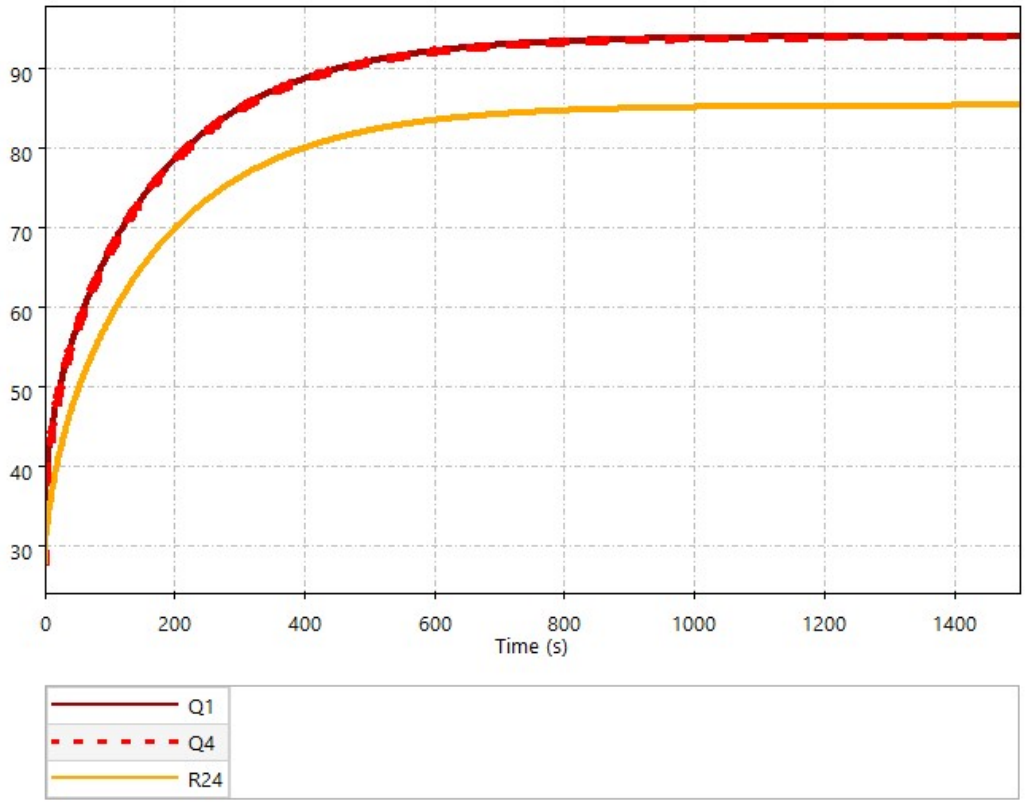


Figure 15. Celsius Thermal Solver result: component warmup of the U half-bridge simulated thermal transient curve



From the Celsius Thermal Solver simulation results, the Q1 MOSFET was the hot spot on the board, at 94.06 °C. Other components such as the Q4 MOSFET, R24 and R23 resistors had a temperature of 93.99 °C, 85.34 °C, and 85.58 °C, respectively.

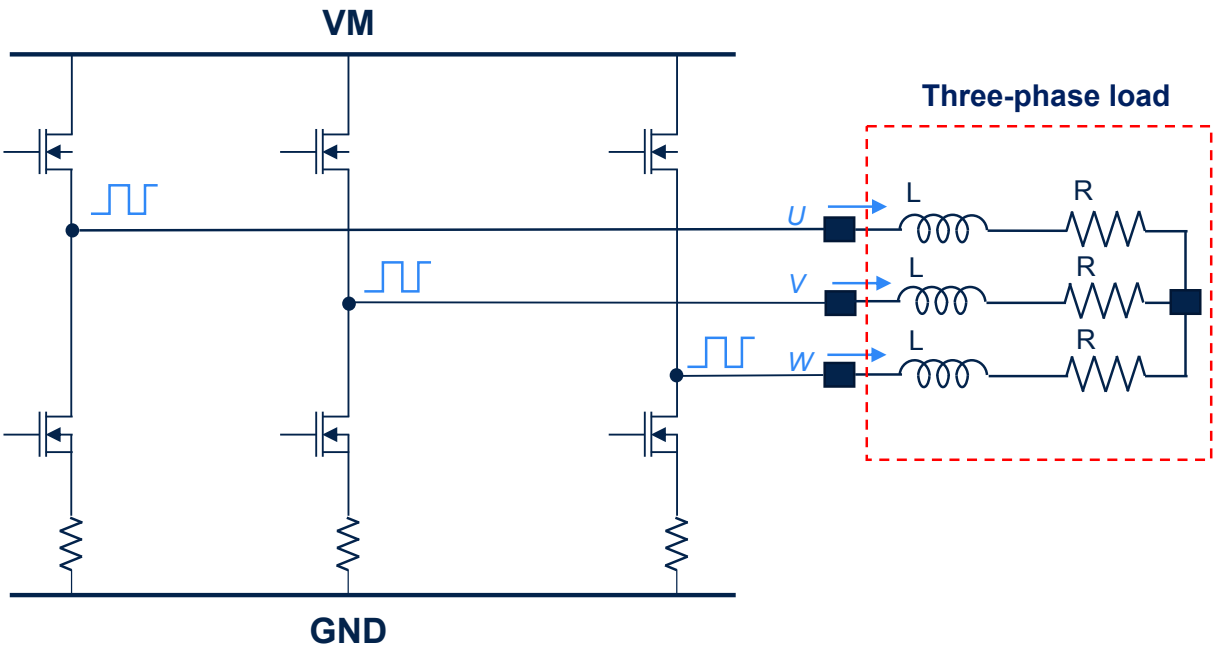
4 Thermal characterization

When evaluating the thermal performance of the EVALSTDRIVE101 board, it is possible to use a motor with proper power rating coupled to a braking bench that should dissipate all mechanical power provided by the motor. This testbench, while challenging to implement, can be greatly simplified by an equivalent setup.

This setup consists of three coils wired in a star configuration, namely a three-phase load that emulates the motor (Figure 16). Each coil must have a saturation current compatible with the board rating, but the inductance or its parasitic resistance value does not need to be equivalent to that of emulated motor.

Indeed, it is more advantageous to have low parasitic resistance value for the coils, to considerably reduce the active power, that would lead to unnecessary Joule effect heating inside the coils, and obtain a lossless reactive power transfer between the board and the load and vice versa.

Figure 16. Three-phase load connected to the inverter



By applying three sinusoidal voltages that are out of phase by 120° to each other to the three terminals of the load, three sinusoidal currents flow in the load. The three sinusoidal outputs are generated by modulating the PWM duty cycle around 50% mean value as in S-PWM.

The peak amplitude of the current is obtained by:

$$I = \frac{V}{\sqrt{(2\pi f L)^2 + R^2}} \quad (8)$$

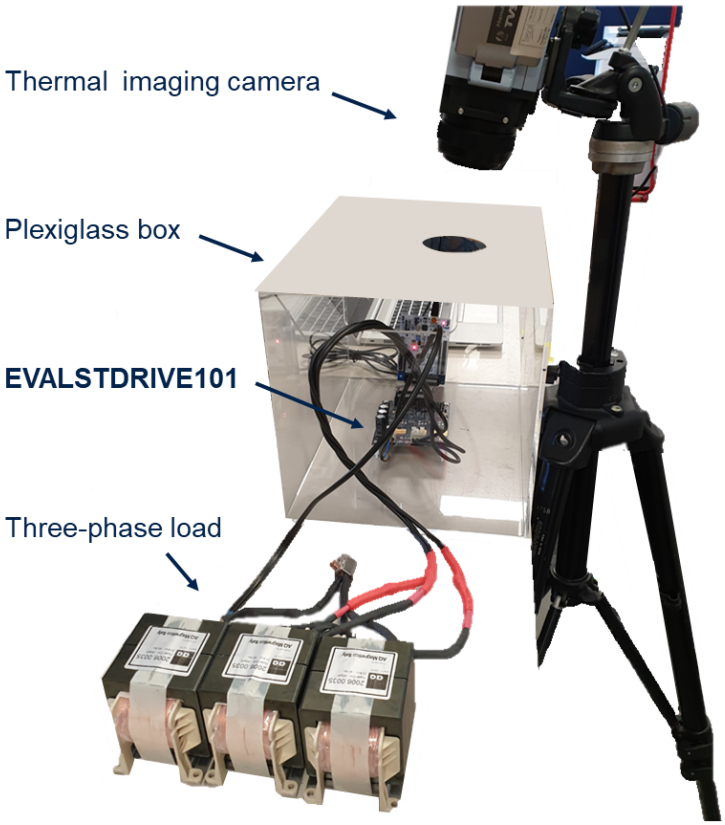
- *V* is the peak amplitude of sinusoidal voltage applied to the load
- *f* is the frequency of sinusoidal voltage
- *L* is the inductance of one coil
- *R* is the resistance of one coil

With this method the power stage works in an operating condition very close to the final motor driving application. Furthermore, the load current is stable and easy to configure by simply varying the frequency and applied voltage amplitude conversely to the motor driving, which needs appropriate closed-loop control algorithms.

4.1 Experimental setup

The setup used for thermal characterization of EVALSTDRIVE101 is shown in Figure 17

Figure 17. Setup for the thermal characterization of the board

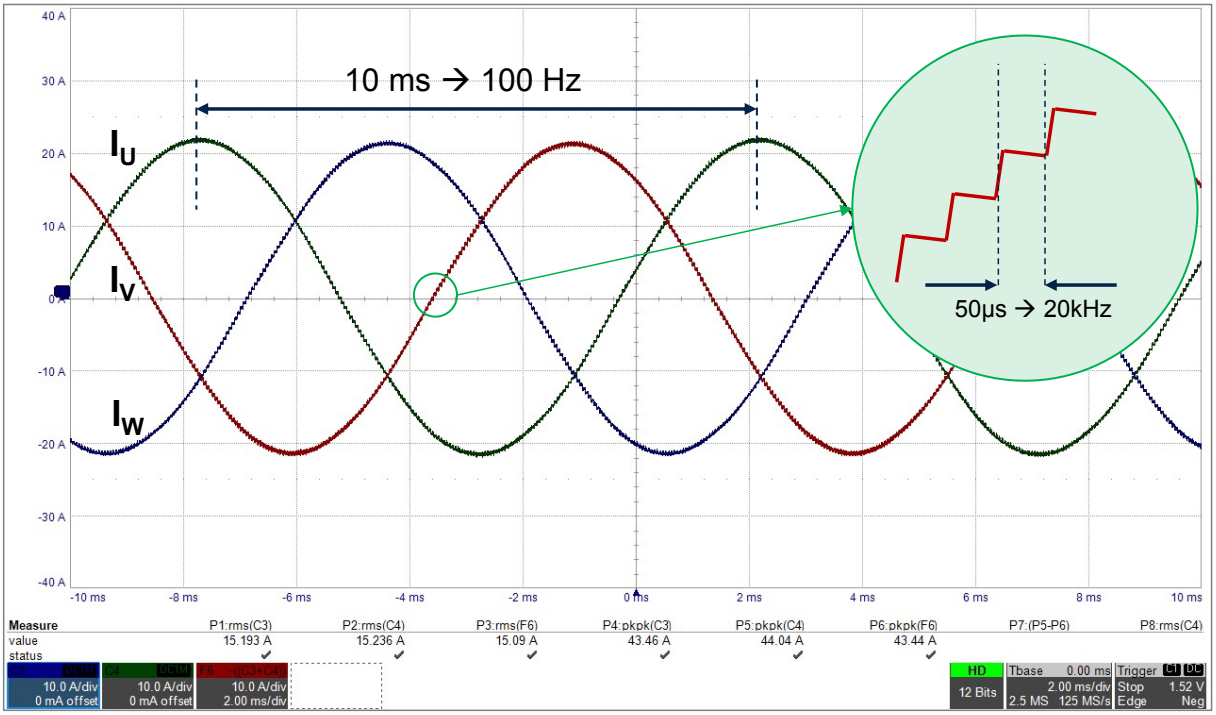


The EVALSTDRIVE101 is connected to a control board to generate the necessary driving signals and is placed inside a plexiglass box to obtain system cooling by convection without accidental air flow.

Above the box there is one thermal imaging camera (model TVS-200 by Nippon Avionics), which frames the board through a hole in the cover of the box.

A three-phase load with inductance of 300 µH and resistance of 25 mΩ for each coil is connected to the board outputs, as previously described, and 36 V is supplied to the system. Figure 18 shows the output current of 15 A_{rms} obtained by applying three out-of-phase sinusoids with a frequency of 100 Hz. The PWM applied by the half-bridges has a frequency of 20 kHz and a dead time of 500 ns.

Figure 18. **Output currents of the three phases using a SV-PWM modulation**



4.2 Power loss measurement

One factor affecting the quality of the simulation results is certainly the data accuracy of the power dissipated by each device on the power stage. This data is obtained in the Section 2 Estimate of power losses using simplified formulae for both the MOSFETs and shunt resistors, thus approximations are introduced.

Measurement was made on the board as described below to evaluate the error in quantifying the dissipated power.

Since the power dissipated by the board is the difference between the input power and the power delivered to the output load, it can be calculated using following equation:

$$P_{loss} = P_{in} - P_{out} = \overline{V_{in} \cdot I_{in}} - \sum_{i=1}^{3} \overline{(V_i - V_c) \cdot I_i} \quad (9)$$

- V_{in} is the input voltage of the board
- I_{in} is the input current
- V_i - V_c is the voltage drop on each coil, i.e. the difference between voltages of i-th output and center tap of the load
- I_i is the current flowing through the i-th coil

The measurement was made using an oscilloscope (model HDO6104-MS by Teledyne LeCroy) and applying the proper math functions to the waveforms: first the point-by-point product of the voltage and current was computed, then the power was averaged over an integer number of sinusoid cycles.

Table 1 shows the measurement results at ambient temperature and at hot when the power stage reached steady state condition. The overall value of power dissipated by the board previously estimated by formulae is also provided.

Table 1. **Measured vs. estimated power losses**

Power	Measure @ T_{amb} [W]	Measure @ T_{hot} [W]	Estimate [W]
P_{in}	27.51	28.39	-
P^{U}_{out}	5.6	5.7	-
P^{V}_{out}	6.5	6.6	-
P^{W}_{out}	6.1	6.2	-
$P_{loss} = P_{in} - (P^{U}_{out} + P^{V}_{out} + P^{W}_{out})$	9.36	9.89	9.5

The results show a very good matching between measurements and estimates which is in line with introduced approximations. An overestimation of the measurement at room temperature of 1.5% is made by the formulae, which provides roughly a 3.9% underestimate compared with hot condition data. This result is in line with the variability associated with the on-resistance of the MOSFETs and shunt resistors since nominal values were used in the computations.

As expected, all power values were higher at hot than at room temperature, due to the increase of the resistances of the coils and MOSFETs with temperature. The data also shows a difference among the measured powers for the three outputs. This effect is due to the unbalancing of the three-phase load, because of slightly different values of L and R from coil to coil. This effect plays a marginal role, since the misalignment is lower than the one between the measurements and the estimate.

4.3 Temperature results

The sinusoids generation and acquisition by the thermal imaging camera were simultaneously activated. The thermal imaging camera was previously configured to collect thermal images every 15 seconds and to include in every capture three temperature markers for components Q1, Q4, and R23, respectively the high-side MOSFET, low-side MOSFET, and shunt resistor of the U half-bridge.

The system remained active until the steady-state condition was reached after about 25 minutes. The ambient temperature detected inside the box at the end of the test was about 28 °C. Figure 19 shows the heating transient of the board that was derived from temperature markers and Figure 20 shows the final temperatures on the board.

Figure 19. **Measured thermal transient curve - EVALSTDRIVE101 warmup at 15 A_{rms}**

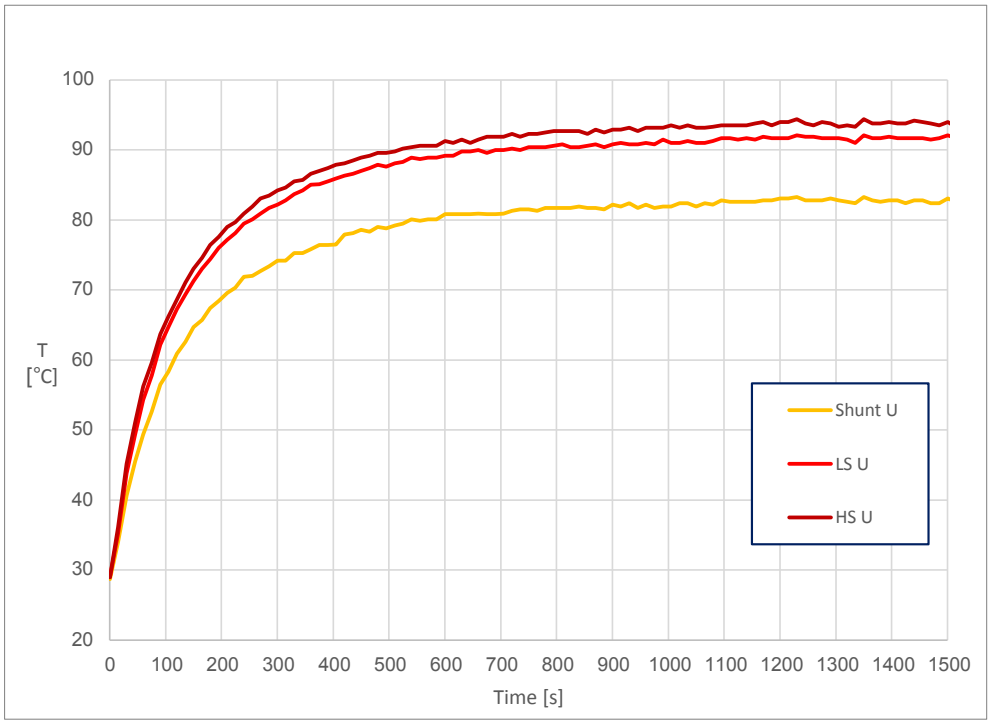
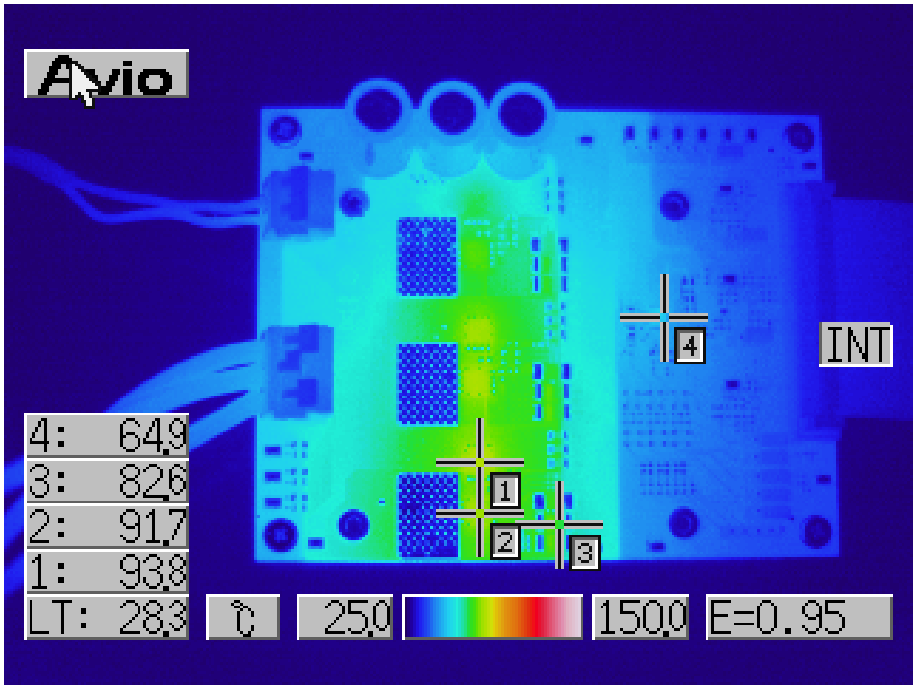


Figure 20. **Thermal measurement - EVALSTDRIVE101 steady-state thermal image**



The measurement showed that Q1 MOSFET was the hottest component of the entire board with a temperature of 93.8 °C, while the Q4 MOSFET and R23 resistor reached 91.7 °C and 82.6 °C, respectively.

As discussed in the previous section, the Celsius Thermal Solver simulated the Q1 MOSFET temperature at 94.06 °C, the Q4 MOSFET temperature at 93.99 °C, and the R23 temperature at 85.58 °C giving a very good matching with measurements. The same agreement can be also found in the time constant of heating transient as can be easily seen from direct comparison of Figure 19 with Figure 15.

5 Conclusion

STMicroelectronics recently released the EVALSTDRIVE101 evaluation board designed taking advantage of Celsius Thermal Solver.

The board targets high power and low voltage three-phase brushless motors as needed by battery powered applications. The board includes a compact power stage of 50 cm^2, which can deliver over 1 kW power and 15 A_{rms} current to the motor without heatsink or additional cooling.

Using different simulation features embedded in Celsius Thermal Solver, it was possible not only to foresee the temperature profile of the board and its hot spots on power stage components but also to have a detailed description of voltage drops and current density along power traces which could be tricky or not feasible at all to obtain by experimental measurements.

Simulation outputs enabled a fast optimization of PCB layout, adjusting placement and correcting layout weakness from early in the design to signoff.

A thermal characterization with infrared camera showed the good agreement between simulated and measured steady state temperatures as well as the transient temperature profile, proving outstanding performance of the board and effectiveness of Celsius Thermal Solver in helping designer to reduce design margin and achieve quick time to market.

6 References

1. L. Coppola, D. Cottet and F. Wildner, "Investigation on current density limits in power printed circuit boards," 2008 Twenty-Third Annual IEEE Applied Power Electronics Conference and Exposition, 2008, pp. 205-210, doi: 10.1109/APEC.2008.4522723.
2. A. Braham, A. Lahyani, P. Venet and N. Rejeb, "Recent Developments in Fault Detection and Power Loss Estimation of Electrolytic Capacitors," in IEEE Transactions on Power Electronics, vol. 25, no. 1, pp. 33-43, Jan. 2010, doi: 10.1109/TPEL.2009.2026749.
3. X. Zhou, Y. Xue, G. Tian and Z. Liu, "Thermal Analysis of Solder Joint Based on Eddy Current Pulsed Thermography," in IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 7, no. 7, pp. 1111-1118, July 2017, doi: 10.1109/TCPMT.2017.2696159.
4. Application Note “Two-Resistor Model for Thermal Simulation” by RHOM Semiconductor.

Revision history

Table 2. **Document revision history**

Date	Version	Changes
01-Feb-2022	1	Initial release.

Contents

List of tables

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