
How to start the User BIST in the PMC

Introduction

This technical note describes how to execute the BISTs implemented in the Power Management Controller Digital Interface (PMC_Dig) of the SPC570Sxx device. The described methodology applies also on other SCP57xx and SPC58xx devices^(a).

User runs the BIST of the PMC – also known as User BIST – to detect failures affecting the voltage monitors embedded in the devices. Since the safety analysis considers the voltage monitors as potential sources of latent faults, User runs these tests at least once after the boot^(b).

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- a. Please check Reference Manual of SCP57xx and SPC58xx to verify if this TN is applicable.
 - b. Other BISTs, such as L/MBIST, are typically performed during the startup phase to detect latent failures and are transparent for the application.

Contents

- 1 Overview 4**
 - 1.1 BIST introduction 4

- 2 How to setup the User BIST 7**
 - 2.1 BIST mode testing scheme 7

- 3 Summary 11**

- Appendix A Further information 12**
 - A.1 Document reference 12
 - A.2 Acronyms 12

- Revision history 13**

List of tables

Table 1.	List of PMC register dedicated for the USER BIST	4
Table 2.	List of monitor checked during BIST	6
Table 3.	BIST timing values	8
Table 4.	BIST time setting	10
Table 5.	Acronyms	12
Table 6.	Document revision history	13

1 Overview

The capability of a circuit to test itself is commonly known as BIST. They are periodic tests used to detect different faults in the device to guarantee its integrity according to the ISO26262 standard.

BISTs described in this document detect latent faults affecting the analog circuitry of the internal voltage monitors.

They are implemented within the PMC and are referenced in the reference manual as User BISTs. User uses the User BIST to check the integrity of all voltage monitors (VD) after power-up.

1.1 BIST introduction

The ISO26262 splits faults in multiple categories:

- Single Point faults: leads directly to the violation of a safety goal.
- Multipoint faults: leads to the violation of the safety goal in combination of other independent faults.

One important difference between these 2 types of faults is the available time to detect them.

System detected a single point fault in a short time that is called *Fault Tolerant Time Interval* (i.e. FTTI). A typical FTTI assumed by the safety analysis is around 10ms.

The time to detect a multipoint fault is more relaxed. Safety analysis assumes to verify the absence of multipoint fault once for trip time that is considered around 12h.

To summarize, typically:

- system executes countermeasures while the safety function runs to detect single point faults;
- system executes countermeasures at least once after the boot in order to detect Multipoint faults.

User BIST detects latent faults affecting the Voltage Monitors. Software starts the User BIST by writing the PMC_dig^(c) registers without the need of configuring any DCF records^(d).

[Table 1](#) reports the list of PMC_dig registers that User configures to execute the User BIST.

Table 1. List of PMC register dedicated for the USER BIST

Register name	Description
BIST_Flags	For monitoring. They are read only bits
BIST_CTRL	It contains control and status bits
BIST_TIME10	To define T0 and T1 time
BIST_TIME32	To define T2 and T3 time

c. Group of Test register inside PMC are dedicated for this scope.

d. User, on the other hands, configures the L/MBIST via DCF records.

Table 1. List of PMC register dedicated for the USER BIST (continued)

Register name	Description
BIST_TIME65	To define T5 and T6 time
BIST_DEBUG	It gives the current VD Under Test of the User

Hereafter a short description of these registers^(e):

- BIST_FLAGS: it contains a monitor of the flag phase 1 and the flags phase 2 for each LVD/HVD monitor. If User BIST pass:
 - BIST_FLAGS_PHASE1 (all bit 'zero') that shows the status monitor is tripped.
 - BIST_FLAGS_PHASE2 (all bit 'one') that shows the status when monitor is lifted.[Table 2](#) lists the 14 monitors checked by the User BIST and the bit position of the two status flags in the *BIST_flags* register.

e. User can find additional details in the Reference Manual

Table 2. List of monitor checked during BIST

Monitoring	BIT_FLAGS bit number	
	FLAGS_P2	FLAGS_P1
UVD_600	2	18
UVD145_C	3	19
UVD145_FL	4	20
HVD400_C	5	21
HVD140_C	6	22
LVD400_AD	7	23
LVD290_C	8	24
LVD290_AD	9	25
LVD290_FL	10	26
LVD108_C	11	28
MVD270_C	12	28
MVD270_FL	13	29
MVD098_C	14	30
MVD098_FL	15	31

- BIST_CTRL: It contains control and status bit. The START flag starts the execution of the BIST. Moreover by configuring this register it's possible to generate:
 - an interrupt and the end of the BIST
 - an FCCU reaction if input fault #2 and 3# are enabled (see "FCCU failure input" table on chapter 6 of Reference Manual [Section A.1: Document reference](#))
- BIST_TIMExy: 3 registers dedicated for configuring the correct timing to execute the BIST sequence (see details on section [Section 2: How to setup the User BIST](#))
- BIST_DEBUG: if the "debug" option is enabled, this register indicates in real time which is the current VD under test (for instance: 0x001100 is for MVD098_FL, 0x001011 is for MVD098_C and so on see Reference Manual for further detail [Section A.1: Document reference](#)).

2 How to setup the User BIST

For SPC570Sxx, default values of PMC_dig TEST registers refers to a configuration of 25 Mhz (AIPS_Clk_0) as work frequency^(f).

User programs the BIST TIME_{xy} registers with proper values, if the BIST is required to run at a different clock. User can find the correct value of the BIST TIME_{xy} register for multiple clock frequencies in the Reference Manual.

If the users want to run the User BIST with the default configuration, they only need to write the START flag.

BIST_CTRL.STATUS (3 bits) gives information about the result of the User BIST:

- 000 = BIST IDLE
- 001 = BIST RUN
- 010 = BIST PASSED
- 011 = BIST FAILED
- 100 = BIST ABORT

User can double check the execution of the User BIST by reading its status in both BIST_CTRL.STATUS register and status register dedicated to each VD (i.e for LVD108_C voltage detector the correspondent register is EPR_LV0 – Event Pending Register^(g)).

PMC_dig implements similar registers for each voltage monitors.

User can enable an interrupt (#477) to alert the end of the BIST execution by configuring the BIST_CTRL register:

- IRQEN flag to enable the interrupt
- IRQST flag to check the interrupt status

In addition User can enable the generation of an NCF in case the User BIST fails:

- NCFEN to enable the NCF on User BIST
- NCFST flag to check the NCF status

2.1 BIST mode testing scheme

As an example this paragraph describes how User tests 3 LVDs via User BIST. These LVDs are:

- LVD_290_F
- LVD_290_A
- LVD_290_C

First point is how to configure the BIST_TIME registers. The execution of the User BIST considers 6 timing for each LVD: from t₀ up to t₆.^(h)

f. The max work frequency for the AIPS_clk is 40Mhz (with PLL running at 80Mhz)

g. In this case, the flag LVD3_C indicates if User BIST has detected any fault in the 1.8 V low voltage monitor: '0' if no currently occurrence and '1' VD occurrence detected on the low voltage 1.08V point supply

h. The timings from t₀ to t₆ are always the same for each VD.

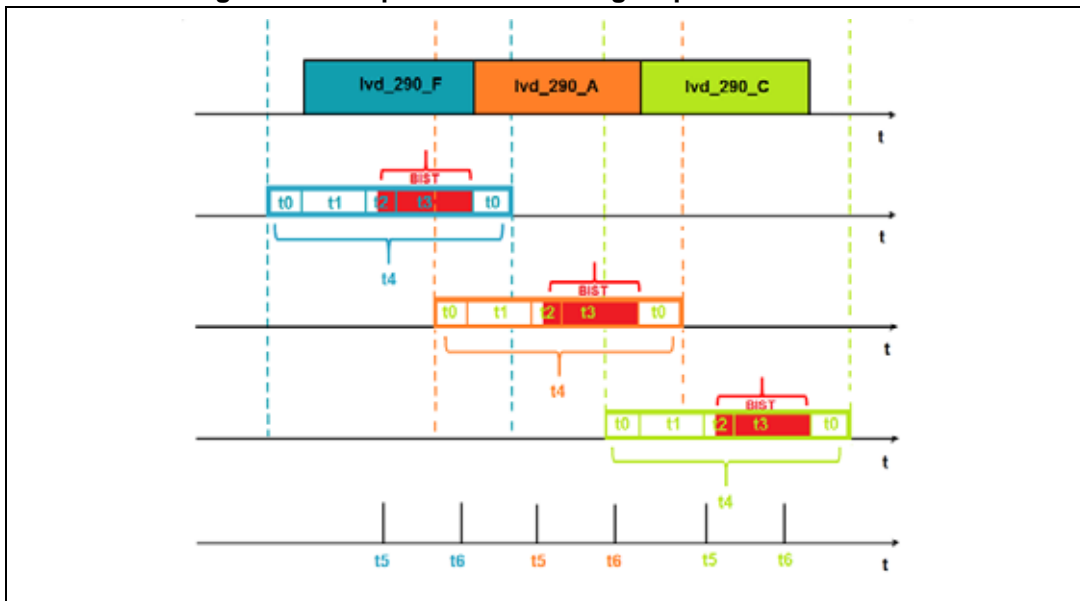
They are:

- t0 and t1 defined in BIST_TIME10 register (converted⁽ⁱ⁾ in TIME_0 and TIME_1 fields)
- t2 and t3 defined in BIST_TIME32 register (converted in TIME_3 and TIME_2 fields)
- t5 and t6 defined in BIST_TIME65 register (converted in TIME_6 and TIME_5 fields)
- $t4 = 2 * t0 + t3 + t2 + t1$

Example of BIST running sequence for 3 LVDs shows a time window of the whole LVD/HVD sequence tested by User BIST.

Within this window 3 LVD are reported: LVD_290_F, LVD_290_A and LVD_290_C.

Figure 1. Example of BIST running sequence for 3 LVDs



Since the execution of User BIST of each LVD overlaps among each other, 't4' timing multiplied by 3 (LVDs) doesn't give the total duration of the User BIST.

User BIST on each LVD is performed between t2 and t3 time (see red parts in the picture). Other timings (t0, t1 and so on) are dedicated for masking and setting the BIST execution.

Table 3. BIST timing values

Label	Description	Value
t0	The time that the monitor output is masked for the SOC before and after the monitor selection	16 μs
t1	The wait time before the BIST testing for a specific LVD takes place. This is required to take care of the transients on the reference	32 μs

i. The formula is provided in the next pages

Table 3. BIST timing values (continued)

Label	Description	Value
t2	The time for which "bm_vthsel_1p2d"(internal signal) is kept logic 0	8 μs
t3	The wait time before starting the testing of the next monitor	32 μs
t4	Time for that the testing monitor output is kept masked from the SoC. $T4 = 2 \cdot T0 + T1 + T2 + T3$	104 μS
t5	The time before "bm_vthsel_1p2d" becomes logic 1 such that the comparator logic 0 output can be checked	350 μs
t6	The time before the end of T3 phase to check logic 1 output of the comparator	350 μs

[Table 3](#) shows the meaning of each timing tx:

ST designers provide the value of these timing slots. User can find them in the reference manual. shows the formula to obtain the value of the related register, e.g. TIME_0, starting from a timing, e.g. t0.

Equation 1

Formula to convert a timing into the value of the related register field

$$TIME_x = tx * AIPS_Clk_freq - 1$$

Equation 2

Example of calculation of TIME_0

$$TIME_0 = t0 * AIPS_Clk_freq - 1 = 16\mu\text{sec} * 25 * \text{Mhz} - 1 = 399$$

In the reference manual, the user can find the values of the register for 2 configurations, i.e. frequency of AIPS_clock equal to 25 MHz or 40 MHz (see [Section A.1: Document reference](#)).

Table 4. BIST time setting

AIPS clock freq.	Base	Time_0	Time_1	Time_2	Time_3	Time_5	Time_6	BIST_TIME register		
								Time_10	Time_32	Time_65
25 MHz	dec	399	799	199	799	8	8	0X031F018F	0X031F00C7	0X00080008
	hex	0x018F	0X031F	0X00C7	0X031F	0X0008	0X0008			
40 MHz	dec	639	1279	319	1279	13	13	0X04FF027F	0X04FF013F	0X000D000D
	hex	0X27F	0X04FF	0X013F	0X04FF	0X000D	0X000D			

User BIST can run up with a max AIPS clock freq of 40Mhz in SPC570S device. This limitation is due to the maximum allowed sys_clock of 80Mhz^(j).

j. AIPS_cloc is defined at sys_clock divided by 2.

3 Summary

This document describes the procedure how to start the User BIST in the SPC570Sxx device that are used to detect latent faults on the VDs of the device.

User BIST can run up to 40Mhz. [Table 3](#) provides the correct timings to execute them. Default execution frequency is 25 MHz. If the user accepts this frequency, he can run the User BIST by simply writing the START flag. No others configurations are needed.

Appendix A Further information

A.1 Document reference

- *SPC570Sx 32-bit Power Architecture® microcontroller for automotive ASILD applications* (RM0349, DocID024507).

A.2 Acronyms

Table 5. Acronyms

Acronym	Name
PMC	Power Management Controller Digital Interface
BIST	Built-In Self-Test
NCF(RF)	Non critical fault/Recoverable fault
CF(UF)	Critical fault/Unrecoverable fault
STCU	Self-Test Control Unit
FCCU	Fault Collection and Control Unit
VD	Voltage Detector
LVD	Low Voltage Detector
HVD	High Voltage Detector

Revision history

Table 6. Document revision history

Date	Revision	Changes
01-Feb-2016	1	Initial release.

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