
FAQ ESD protection**Introduction**

This document contains a list of frequently asked questions (FAQ) on ESD protection components. Our EMC expert replied to these questions during [EMC – system immunity against electrostatic discharges webinar](#).

1 FAQ and answers

1.1 What is ESD protection?

ESD stands for electrostatic discharge. ESD is defined by the ESD association as "the rapid, spontaneous transfer of electrostatic charge induced by a high electrostatic field".

It is the result of static electricity discharge. Static electricity is the collection of electrically charged particles on the surface of a material.

Various materials have a tendency of either:

- Giving up electrons and gaining positive (+) charges
- Attracting electrons and gaining negative (-) charges

Electrostatic discharge will cause potential failure on the integrated circuits of your PCB.

These failures are called electrical over stress (EOS), resulting in silicon melting, oxide punch-through, junction damage, metallization damage or degradation affecting the long-term reliability of your electronic system.

A survey from the EOS industry council (<https://www.esdindustrycouncil.org/ic/docs/Industry%20Council%20White%20Paper%204%20rev1.2.pdf>) shows that 30% of customer claims are due to ESD or EOS (electrical over stress). Furthermore, the miniaturization of the components is increasing the integrated circuits sensitivity to ESD.

1.2 Where can I get more information about eye diagram integrity?

Eye diagram information is defined by standards like USB, HDMI etc.

The ESD protection device compliancy with eye diagram is specified in the related datasheet, for example in [HSP051-4M10](#).

1.3 What about other USB requirements related to ESD? ("TD 4.1.2 " or "TD 4.12.2")

Eye diagrams can be negatively impacted by wrong ESD protection selection. An extremely high capacitance ESD protection may cause the eye diagram test to fail.

On the other hand requirements like attach / detach requirements (more functional) cannot be impacted by the ESD protection because ESD protection is transparent (high impedance and low capacitance in parallel with datalines) in normal operation.

TD 4.1.2 is related to USB Type-C test for R_p that must not be present for source application when source is OFF. ESD protection will be transparent in this test.

TD 4.12.2 is related to USB Type-C test checking if there is only one upstream port in a hub port device.

1.4 How to select the V_{CL} ? (what is the maximum transient voltage accepted by my circuit and if I can assume the maximum absolute voltage of my ICs or is there a better approach to follow?)

The absolute maximum rating (AMR) voltage value is not relevant because it is a DC measured voltage and not measured for a transient voltage, hence an intrinsically pessimistic value (AMR value is too low).

In the presented example the AMR value is too low, $AMR = 5.5\text{ V}$ while the ESD destruction value is 12 V.

The best approach to select the V_{CL} is to apply the SEED methodology described in our [ESD Webinar](#).

If any TLP information is available for the IC to be protected, the lower V_{CL} will ensure the better protection.

1.5 Which ST specific part do you recommend to protect the RF port of a transceiver working at 868 MHz with 14 dBm output power? (it must have very low capacitance and low clamping voltage)

14 dBm corresponds to 1.6 V max on 50 Ω load. As a consequence, [ESDARF02-1BU2CK](#) matches the requirement at 868 MHz (no RF losses, $V_{MAX} < V_{RM}$ and bi-directionnal for RF signaling).

1.6 What about protecting a power line? (V_{BUS} in USB on slide 37 of our expert webinar)

Power lines require high current capability surge protection because lightning and switching transients are present on these lines (cf [IEC61000-4-5](#)) as well as some functional events generating inrush currents (full-load unplugged, adapter failure, etc). STMicroelectronics protection device against IEC61000-4-5 surges are available [here](#).

1.7 Which part do you recommend for protecting 12 V DC outputs?

[ESDA15P60-1U1M](#) fits 12 V DC outputs protection for both ESD ([IEC61000-4-2](#)) and switching transients (cf [IEC61000-4-5](#)).

1.8 Which ESD protection component do you recommend when differential current measurement is used ?

The original question during the webinar was: "My design is analogic measurement current in an isolated high tension (25 kV) system. Sometimes, we have breakdowns, and we have damage (aop 1st stage AD4610 or a voltage regulator (+5 V or -15 V or +15 V). I tried to insert protective components without performance loss. I measured 5 nA current and some TVS diodes have leakage current 1 or 10 or 100 nA. Any useful reference in future can be test", it might be differential measurement.

For that specific case, 2 ESD protections on common mode may be better than a single ESD protection in differential. We recommend [ESDZV5H-1BU2](#) for +/-5 V and [ESDLC20-1BF4](#) for +/-20 V.

1.9 Do we need ESD for the RS-485 transceivers or is it included?

Check the ESD specification for your RS-485 transceiver: if it is only rated per HBM, then system-level ESD is needed ([IEC61000-4-2](#)). To protect RS485 transceiver, [ESDA14V2BP6](#) is recommended.

Please check schematic in figure "ESD14V2BP6 protection device schematic" in [AN5245](#).

ST485 transceiver can be split in 2 families:

- with system ESD protection (ST485E series)
- without system ESD protection (ST485 series)

When ST485E series cannot be placed close to the ESD source, it is required to use external ESD protections in order to avoid any EMI coupling with internal PCB tracks. EMI coupling induced by ESD can generate latch-up failures in your system.

1.10 Do I need additional ESD protection if I use digital isolators for I/Os (like Si86xx)?

Yes, this specific product requires an external ESD protection. For 1 Mbps signal with 5.5 V AMR, we recommend [USBLC6-2SC6](#) or [USBLC6-4SC6](#) according to the number of lines to be protected.

1.11 Can I use the circuits for PSpice simulations and real test setups or is something missing (ST webinar p.11)?

Yes, it is a simplified but functional schematic. Real schematic is more complex with serial inductors.

1.12 Have ST all PSpice models of their portfolio?

You can find ST PSpice ESD protection models under [SPICE models](#).

1.13 Is the track on the PCB from the ESD source to the ESD protection device rated for the ESD maximum discharge current defined by the ESD level required?

The track maximum DC current is not critical due to the ESD event duration (≈ 100 ns).

1.14 How do you connect the shield of the connector to the PCB?

We usually connect it to the GND of the system.

1.15 Should we connect ESD protection ground to 0 V or GND?

ESD protection ground must be connected to the reference GND plane of the protected I/O to limit or avoid any parasitic inductance effect due to multiple ground planes connection.

1.16 Where is the current going on slide 17 of our EMC expert webinar?

The current is flowing to the ground.

1.17 Is it really necessary to provide external ESD protection in case of no ESD protection for GPIO pins of a microcontroller built in?

It is only necessary to protect GPIO exposed to system-level ESD (connector, button) otherwise embedded HBM is enough.

1.18 Can you explain why ESD protection is needed with a USB-C connector housed in a plastic case? Because of the shield ground all around the USB contacts (V_{BUS} and signals) it is impossible to touch contacts directly with a finger.

ESD cannot be assimilated to simple conduction through a metal track, it is a charge equilibrium between 2 systems. As a consequence, air discharge can appear and non-conductive materials can let the charge flow (e.g. side key buttons on smartphone need to be protected).

1.19 Are there other types of ESD protection without using TVS?

Other type of ESD protection can be : MOV, polymer and PCB spark gap. All of them present very high clamping voltage and reliability issues that are not compatible with ESD protection of sensitive ICs.

1.20 When the use of TVS is not enough for protection (for example when voltage or current is exceeded), do you recommend serial resistor or other type of components?

Adding a serial resistor can be recommended because it will decrease the clamping voltage on protected IC I/O. But for some interfaces, adding a serial resistor may exceed the line impedance specified in the standard or decrease the bandwidth.

1.21 Can TVS diode and Zener diode be in parallel (Zener to protect from DC overvoltage and TVS to protect from transients)?

TVS protects against transient over-voltage while Zener is for voltage regulation, because not rated against surges nor over-voltages. To protect against DC over-voltage, an over-voltage protection (OVP) is required. OVP and TVS can be used together with TVS maximum clamping voltage slightly below OVP AMR.

1.22 Regarding on the question about protecting a IO power line (slide 37), the decoupling capacitor also lowers the voltage when a charge is injected, but are there specific requirements for this capacitor?

On power line, capacitor are selected to fit power requirement. The capacitor rated voltage must be higher than the clamping voltage of the TVS to avoid capacitor degradation or destruction when surge event occurs.

1.23 Are there any easier rules to apply to choose the key parameters?

Secure margin between AMR and maximum ESD clamping voltage before destruction can be very scattered. To select the best ESD protection, bandwidth must not be over-sized, V_{RM} must be just slightly higher than line voltage in order to lower the clamping voltage.

1.24 If I choose for the next version the ESDLIN1524BJ close to input current, can I place it at power inputs also to protect voltage regulators?

Power inputs are usually protected using TVS rather than ESD protection components.

Automotive TVS portfolio is available [here](#).

Industrial TVS portfolio is available [here](#).

1.25 Is there any protection related to LEDs?

Standard ESD protection ([ESD051-1BF4](#)) can be used for LED protection. Bidirectional protection is recommended to test LED mounted on reverse.

1.26 What affordable and cheap ESD gun can you recommend?

We use Teseq ESD gun. We do not have any ESD gun benchmark.

1.27 What would you recommend for clothing when handling ESD sensitive devices?

In an ESD-controlled environment, a conductive lab coat with ESD wrist connected to the ground are recommended.

1.28 In terms of ESD certification of an electronic circuit board, can you recommend a provider of this service in France?

EMITECH is a French Lab.

1.29 Can you tell something about protection during soldering (ie: solder connector wires to a board)?

During soldering (connector as example), only HBM is relevant but the environment must be under control (operator with wrist connected to ground, solder iron connected to ground).

1.30 How do you protect multiple MCU pins that do not go outside the PCB and is it necessary? (boards can be completely damaged from accidental touching of a PCB pad)

PINs that do not go outside the PCB do not require specific ESD protection but special care is mandatory for handling (conductive lab coat with ESD wrist connected to the ground).

1.31 Is it possible to expose my problem with an application engineer in next days?

Feel free to reach us via our local support: https://www.st.com/content/st_com/en/support/support-home.html.

1.32 How do you measure ESD signals? Do you use scopes?

We use a high bandwidth, high sample rate oscilloscope on 50Ω with 40dB external input attenuation. See STMicroelectronics [AN3353](#).

1.33 Can I use a Zener diode to clamp an ESD over-voltage?

A Zener diode is used for voltage regulation under DC-current condition but neither their silicon nor their package is rated for transient surge dissipation.

Only ESD or transient voltage suppressor (TVS) specify the transient surge they can dissipate.

1.34 Is a 30 kV ESD diode better for protection?

The best parameter to qualify the efficiency of an ESD protection is the clamping voltage because if your 30 kV ESD diode has a poor clamping voltage it means your application will be more sensitive to transient voltages.

ESD robustness higher than 8 kV has to be taken into account only if your application requires it like in automotive standard ISO10605.

1.35 How can I select the ESD protection based on my IC electrical parameters?

Because TLP data are not specified by ICs suppliers, you can only rely on the V_{RM} of the line to be protected to select your ESD protection. In this case the clamping voltage after an 8 kV ESD contact discharge can help you to compare ESD protection efficiency.

1.36 I need to populate different interfaces with ESD protection, can I use the same ESD protection for all these interfaces?

Yes, but keep in mind that each interface has its own requirement. For example you may choose a low capacitance ESD in a 2-line package to protect D_{plus} and D_{minus} pins of an USB connector in order to keep the best signal integrity on these datalines whereas you may choose a single line ESD protection with high capacitance for a touch button to lower signal bouncing.

1.37 Is external ESD protection needed for CDM (charged device model)?

No, ESD protection according to CDM is granted for all ICs because it is related to component level protection like HBM.

1.38 What is exactly the V_{RM} parameter of an ESD protection and what is it good for?

V_{RM} is the maximal operating voltage of the protection to ensure a good transparency of the application voltage signal in the normal operation. The V_{RM} of the ESD protection must be higher than the normal signal voltage amplitude. If the signal is negative and positive, the protection must be bi-directional to avoid rectifier phenomenon. If the signal to be protected is only positive, an unidirectional protection is preferred. Along with the V_{RM} voltage there is also the protection current leakage parameter called I_{RM} . A too high leakage current can affect the system overall consumption but it can also change a data line voltage. Usually, the leakage current is below 1 μ A at V_{RM} (ESDZV5 has I_{RM} e.g. at 100 nA maximum).

1.39 What does is meant with snap-back ESD protection?

Standard ESD protections activate at breakdown voltage (called V_{BR}) and their voltage increases with the current linearly to clamping voltage. The snap-back protection instead has a snap-back effect which means that it lowers its clamping voltage after the protection is triggered. The holding voltage (V_H) is the lowest voltage when the snap-back protection has turned on. The lower is the holding voltage, the better is the clamping voltage.

The figures below show on the left the I/V characteristics of a standard ESD protection and on the right the I/V characteristics of a snapback ESD protection.

Figure 1. Electrical characteristics (definitions, standard ESD protection)

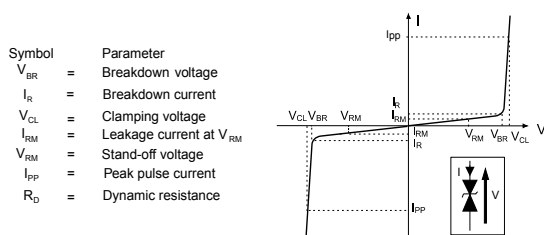
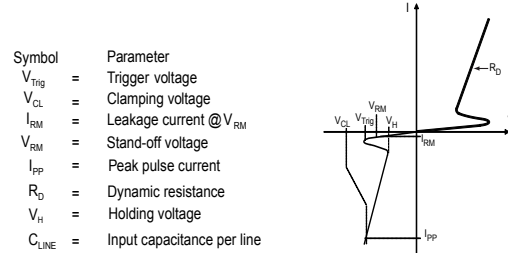


Figure 2. Electrical characteristics (definitions, snapback ESD protection)



Revision history

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Date	Revision	Changes
24-Jan-2020	1	First issue.

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