Technical note

Self-test configuration for SPC58xNx device

Introduction

This document provides the guidelines about how to configure the self-test control unit (STCU2) and start the self-test execution.

The STCU2 on SPC58xNx device manages both memory and logic built-in self-test (MBIST and LBIST) of the device. The MBISTs and LBISTs can detect latent failures which affect the volatile memories and the logic modules.

The reader should have a clear understanding of the usage of self-test. See Section 4.1 Reference documents for additional details.

1 Overview

SPC58xNx supports both the MBIST and LBIST.

SPC58xNx includes:

- 92 memory cuts (from 0 to 91)
- LBIST0 (the safety LBIST)
- 6 LBIST for diagnostic(1) (from 1 to 6)

1. *LBSIT for diagnostic should run when the vehicle is in the garage and not while the safety application is running.*

The reader can consult the complete list on the chapter 7 (Device configuration) of the SPC58xNx Reference Manual.

See Section 4.1 Reference documents for additional details.

2 Self test configuration

Self test can run either in online or offline mode.

2.1 MBIST configuration

To reach the best trade-off in terms of consumption and execution time, we recommend dividing the MBISTs into 11 splits. The MBIST partitions belonging to the same split run in parallel.

The 11 splits run in sequential mode. For examples:

- all MBIST partitions belonging to the split_0 starts in parallel;
- after their execution, all MBIST partitions belonging to the split_1 start in parallel;
- and so forth.

The Section 4.1 Reference documents shows the complete list of the MBISTs and splits.

2.2 LBIST configuration

In offline mode, generally it run the only LBIST0 , that is the safey bist (to guarantee the ASIL D). It's the first BIST in the self test configuration (pointer 0 in LBIST_CTRL register).

In online mode the user can choose to run the other LBISTs (from 1 to 6) for diagnostic use. They include:

- LBIST1: gtm
- LBIST2: hsm, sent, emios0, psi5, dspi
- LBIST3: can1, flexray_0, memu, emios1, psi5_0, fccu, ethernet1, adcsd_ana_x, crc_0, crc_1, fosu, cmu_x, bam, adcsd_ana_x
- LBIST4: psi5_1, ethernet0,adcsar_dig_x, adcsar_dig_x, iic, dspi_x, adcsar_seq_x, adcsar_seq_x, linlfex_x, pit, ima, cmu_x, adgsar_ana_wrap_x
- LBIST5: platform
- LBIST6: can0, dma

2.3 DCF list for offline configuration

MBISTs and LBIST0 can run in offline up 100 Mhz as max frequency. The Appendix reports the list of the DCF to be configured in order to start up the MBIST and LBIST during the boot phase (offline mode). They take around 42 ms.

2.4 Online mode configuration

In online mode the MBIST split list remains the same with some limitations due to life cycle. All MBISTs can run in online mode only in ST production and Failure Analysis (FA). In the other Life Cycles, HSM /MBIST and FLASH MBIST are not accessible. In this case, the maximum frequency for MBIST 200 Mhz, provided by the sys_clock.

The LBIST for diagnostic can run up to 50 Mhz, while LBIST 0 can run up to 100 Mhz. In that case, STCU registers can be configured with the "register value" column of the DCF list file.

3 Summary

In SPC58xNx can run both MBIST and LBIST. During offline can run LBIST0 and all MBISTs according to the split configuration. During online mode can be run also the LBIST for diagnostic.

4 Other information

4.1 Reference documents

Table 1. **Reference documents**

Doc Name	ID	Title
RM0421	028528	SPC58xNx 32-bit Power Architecture® microcontroller for automotive ASILD applications
AN4551	026636	SPC574K72xx self-test procedures

The Split and DCF setting are contained in a Microsoft Excel® workbook files attached to this document. Locate the paperclip symbol on the left side of the PDF window, and click it. Double-click on the Excel file to open it.

4.2 Acronyms

Table 2. **Acronyms**

Acronym	Name
MBIST	Memory built-in-self-test
LBIST	Logic built-in-self-test
STCU2	Self-test control unit
HSM	Hardware system module
LC	Life Cycle
DCF	Device Configuration Format (DCF) Records
UTest	User Test flash block
FA	Failure Analysis

Revision history

Table 3. **Document revision history**

Date	Version	Changes
30-Jun-2020	1	Initial release.

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