
SPC584Cx/SPC58ECx Ethernet address filtering

Introduction

SPC584Cx/SPC58ECx 32-bit MCU automotive micro-controllers feature a quality of service 10/100 Mbit/s Ethernet controller that implements the medium access control (MAC) layer plus several internal modules for standard and advanced network features.

This technical note aims at introducing the internal hardware filtering module and its related registers.

All the information available in this document can be considered and adopted, with minor variances, for the whole SPC58x MCU family where the Ethernet 10/100 controllers are embedded.

1 Ethernet controller overview

The 10/100 Mbit/s Ethernet provides many advanced features that can be summarized into the following categories:

- MAC core
- DMA transaction layer (MLT)
- DMA block
- SMA interface
- Power management block (PMT)

2 RX flexible address filtering modes

The receive block supports different address filtering modes:

- 128 MAC addresses for the 48-bit perfect filtering
- A 64-bit hash filter for multicast and unicast (DA) addresses
- Option to pass all multicast addressed packets
- Promiscuous mode to pass all packets without any filtering for network monitoring
- Additional packet filtering e.g. VLAN

This technical note is focused on the first filter mode in the list above.

3 MAC address filter register groups

The SPC58EC Ethernet supports 128 MAC address filter registers. Not all registers are equal. These registers can be categorized into 4 groups.

- Groups 2 and 3 are identical in all aspects
- Group-1 with 31 registers is the most versatile and flexible group for address filtering
- Group-0 has only one register with limited capabilities for address filtering. Group-0 register is dual purpose, it is used for filtering on the RX side and on the TX side the value of this register is inserted in the SA field of the pause control frame.

The Figure 1 illustrates the grouping of address filter registers and the filtering capabilities of each group.

Figure 1. Address filter register groups

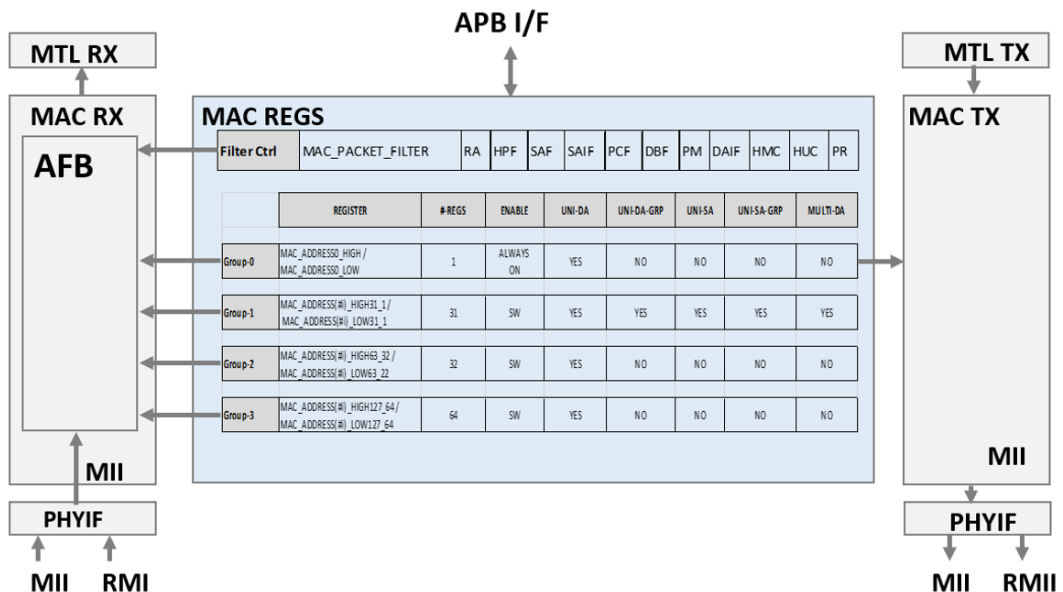
GROUP#	REGISTER NAMES	NUM FILTER REGS	FILTER ENABLE	UNICAST DA	UNICAST DA GROUP	UNICAST SA	UNICAST SA GROUP	MULTICAST DA
Group-0	MAC_ADDRESS0_HIGH / MAC_ADDRESS0_LOW	1	ALWAYS ON	YES	NO	NO	NO	NO
Group-1	MAC_ADDRESS(#)_HIGH31_1 / MAC_ADDRESS(#)_LOW31_1	31	SW	YES	YES	YES	YES	YES
Group-2	MAC_ADDRESS(#)_HIGH63_32 / MAC_ADDRESS(#)_LOW63_22	32	SW	YES	NO	NO	NO	NO
Group-3	MAC_ADDRESS(#)_HIGH127_64 / MAC_ADDRESS(#)_LOW127_64	64	SW	YES	NO	NO	NO	NO

The following Figure 2 shows the interaction of the address filter registers with the address filter block (AFB) in the MAC receive.

The MAC_PACKET_FILTER register is the global filter control register.

Note: Only the bits affecting the MAC address filters are shown for the MAC_PACKET_FILTER register. For field descriptions please refer to the Ethernet register section of the device's reference manual.

Figure 2. Address filter registers and address filter block



3.1 MAC address filter register group-0

The Figure 3 shows the group-0 register. This group has only one register. The MAC uses this register for filtering the received packets and inserting the MAC address in the transmit flow control (pause) packets. This group has very limited filtering abilities. It supports a perfect match on MAC DA field of UNICAST frames only. It is recommended to use registers for filtering.

This filter is always enabled (AE=1) and follows a programming sequence to activate the new value:

- STEP1: Program MAC_ADDRESS0_HIGH
- STEP2: Program MAC_ADDRESS0_LOW

The STEP2 triggers the activation of new values. It is recommended to program the MAC_ADDRESS0_LOW register as a single 32-bit unit.

A smaller programming unit (8 or 16 bits) will result in multiple read-modify write cycles on this register which may result in corruption.

Figure 3. Address filter register group-0

MAC_ADDRESS0_HIGH				MAC_ADDRESS0_LOW
AE=1	RSVD	DCS[1:0]	ADDRHI[15:0] MAC[47:32]	ADDRLO[31:0] MAC[31:0]

3.2 MAC address filter register group-1

The Figure 4. Address filter register group-1 shows the group-1 register organization. This group has a total of 31 registers. This is the most versatile group for MAC address filtering. It is recommended to use registers for filtering.

Like group-0 it supports a perfect match on MAC DA field of UNICAST frames. In addition, it supports the following:

- Filter on either SA or DA
- Filtering of multicast frames
- Group filtering on SA/DA by using byte masks

Unlike group-0 filter, which is always enabled, the filters in this group must be enabled by SW setting AE to 1.

Figure 4. Address filter register group-1

MAC_ADDRESS1_HIGH31_!						MAC_ADDRESS1_LOW31_1
AE	SA	MBC[5:0]	RSVD	DCS[1:0]	ADDRHI[15:0] MAC[47:32]	ADDRLO[31:0] MAC[31:0]

3.3 MAC address filter register group-2 and group-3

The Figure 5 shows the register organization. These groups have identical characteristics with 32 registers each. Unlike group-1 registers these 2 groups have limited filtering abilities. They can be used for perfect filtering on MAC DA of UNICAST frames only.

In regard to the group-0 the only difference is that each filter in these groups must be enabled by SW by setting AE to 1.

Figure 5. Address filter register group-2 and group-3

MAC_ADDRESS32_HIGH63_32				MAC_ADDRESS32_LOW63_32
AE	RSVD	DCS[1:0]	ADDRHI[15:0] MAC[47:32]	ADDRLO[31:0] MAC[31:0]

MAC_ADDRESS64_HIGH127_64				MAC_ADDRESS64_LOW127_64
AE	RSVD	DCS[1:0]	ADDRHI[15:0] MAC[47:32]	ADDRLO[31:0] MAC[31:0]

4 Programming example

The following code shows a basic example of how to program the `MAC_ADDRESS0_HIGH` and `MAC_ADDRESS0_LOW` registers:

```
dataH = (addr[5] << 8) | addr[4];
dataL = (addr[3] << 24) | (addr[2] << 16) | (addr[1] << 8) | addr[0];
reg->MAC_ADDRESS0_HIGH.B.ADDRHI = dataH;
reg->MAC_ADDRESS0_LOW.B.ADDRLO = dataL;
```

Where the `addr` variable is the MAC address passed by the user.

The following code shows how to program one of the `MAC_PF_1_31` registers with an address provided by the user.

```
data = (addr[5] << 8) | addr[4];
reg->MAC_PF_1_31->MAC_ADDRESS_HIGH31_1.B.ADDRHI = data;
reg->MAC_PF_1_31->MAC_ADDRESS_HIGH31_1.B.AE = 1;
data = (addr[3] << 24) | (addr[2] << 16) | (addr[1] << 8) | addr[0];
reg->MAC_PF_1_31->MAC_ADDRESS_LOW31_1.B.ADDRLO = data;
```

The user should program the `MAC_PACKET_FILTER` register according to the configuration desired. This register contains the available filter controls for receiving packets.

5 MAC address filter results

The MAC address filters are the first line of filtering followed by other filters.

The Software application can be programmed to discard the frames failing the filters or forward the frames with fail status. Frames passing the MAC address filtering are then subjected to further filtering.

Appendix A Other information

A.1 Acronyms and abbreviations

Table 1. Acronyms and abbreviation table

Terms	Meaning
SA	Source Address field of MAC frame
DA	Destination address field of MAC frame
UNI	Unicast frames
MULTI	Multicast frames
MAC	Media access control
MTL	Transaction layer
MII	Media independent interface
RMII	Reduce media independent interface
APB	Advanced peripheral bus
AFB	Address filtering block

A.2 Reference documents

- RM0407 reference manual

Revision history

Table 2. Document revision history

Date	Version	Changes
23-Sep-2020	1	Initial release.

Contents

1	Ethernet controller overview	2
2	RX flexible address filtering modes	3
3	MAC address filter register groups	4
3.1	MAC address filter register group-0	5
3.2	MAC address filter register group-1	5
3.3	MAC address filter register group-2 and group-3	6
4	Programming example	7
5	MAC address filter results	8
Appendix A	Other information	9
A.1	Acronyms and abbreviations	9
A.2	Reference documents	9
	Revision history	10

List of tables

Table 1.	Acronyms and abbreviation table	9
Table 2.	Document revision history	10

List of figures

Figure 1.	Address filter register groups	4
Figure 2.	Address filter registers and address filter block	4
Figure 3.	Address filter register group-0	5
Figure 4.	Address filter register group-1	5
Figure 5.	Address filter register group-2 and group-3	6

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