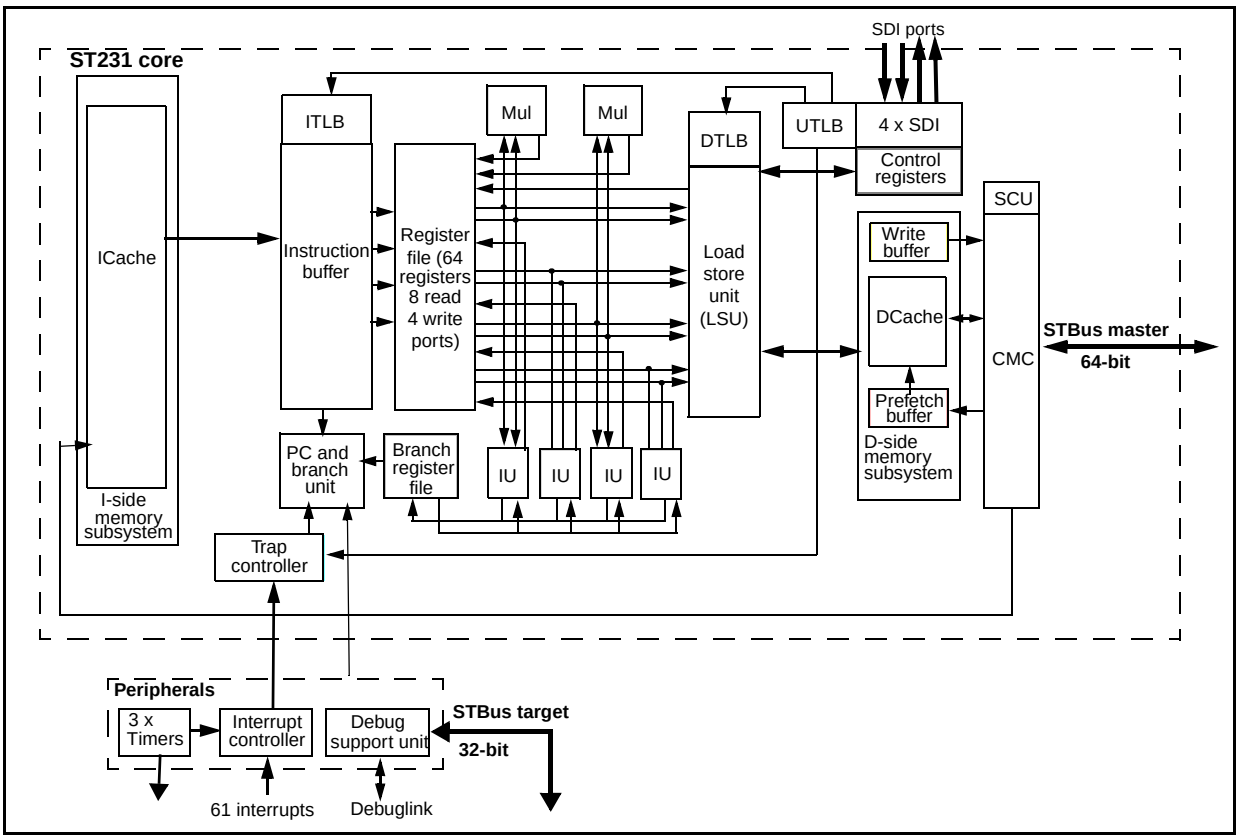
ST231

High performance VLIW processor core

Data Brief



Description

The ST231 very long instruction word (VLIW) core is a high performance low power core designed for use in compute intensive applications as a host and/or audio video processor.

The ST231 core is a four issue VLIW processor and is significantly simpler and smaller than an equivalent four issue superscaler processor. This is because the compiler schedules operations whereas a superscalar processor needs complex hardware to achieve the same.

Applications include embedded systems in the consumer, digital TV, and telecommunications markets where there is a specific need for high performance low cost audio, video and data processing.

The ST200 VLIW family architecture and toolsets allow applications to be developed in C or C++ in conjunction with a real time operating system.

The core provides support for virtual memory by means of a TLB. Full OS21 and Linux tool support are available with this product.

Features

- Performance (when implemented in 65LP):
  - 500 MHz processor clock, 4 issue cycle (peak) providing up to 1.6 billion operations per second
  - 32-bit load and store
  - High speed 64-bit STBus interconnect technology
  - 4 high speed data streaming interfaces
  - Low power consumption combined with small silicon area
- Subsystem:
  - 32-bit instruction set architecture (ISA)
  - 32Kbyte ICache (direct mapped), 32Kbyte DCache (four way set associative)
  - Up to 128-bit wide instruction word
  - Parallel execution units including:
    - four 32 bit integer unit (IU)
    - two 32 x 32 bit multiplier units (MUL)
    - a 32 bit load/store unit (LSU)
  - Interlocks
  - Register file (64 x 32-bit registers)
  - Core memory controller (CMC)
  - 8 entry, software controlled data prefetch buffer (1 cache line per entry)
  - 4 entry write buffer (1 cache line per entry)
  - Virtual memory support using translation lookaside buffers (TLB)
  - Performance monitoring and processor cycle counting hardware
  - Speculative control unit (SCU)
- Peripheral units:
  - 3 x 32-bit programmable timer units (TU)
  - Interrupt controller (INTC) with up to 61 user interrupt sources
  - Debug support unit (DSU)
- Interfaces:
  - 4 streaming data interfaces (SDI) allowing very high bandwidth data to be streamed through the processor to avoid memory bus traffic and cache pollution
  - 64-bit STBus
- Development tools:
  - Optimizing C/C++ compiler
  - Debug access to device through ST Micro Connect and JTAG port
  - STWorkbench, based on the Eclipse® IDE
  - Extensive hardware support:
    - hardware breakpoints
    - performance counters
- Operating system support:
  - OS21 (small real time OS supporting multi-threading)
  - Linux® OS

- Other features:
  - Full scan and BIST testability
  - Power management
    - fully static design
    - idle mode
    - optional fine-grain clock gating
  - Fully synthesizable soft core

ST231 performance

The ST231 VLIW core has been optimized for mobile high performance audio, video and speech applications where low power and energy consumption is critical.

The ST231 core is available as a soft IP.

Additional information

For further information, please refer to the *ST231 Core and Instruction Set Architecture manual (ADCS 7645929)* and the *ST200 Micro Toolset User Manual (ADCS 8063762)* available through your local ST FAE.

Revision history

Table 1. Document revision history

Date	Revision	Changes
27-Jan-2009	D	Reorganised to be consistent with other databriefs.
12-Mar-2008	C	Reorganised for consistency with *ST240 Databrief (ADCS 8110995)*.
05-Feb-2007	B	Updated in new corporate template. Change to the performance features.
25-Mar-2004	A	Initial release

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