Self-test configuration for SPC584Cxx/SPC58ECx devices

Introduction

This document is a guideline about how to configure the STCU run self-test in SPC584Cx/SPC58ECx devices in both offline and online mode. The self-test consists of logic and memory BISTs (L/MBIST). It is used to detect latent failures and is transparent for the application. The reader should have a clear understanding of the usage of self-test. See Reference documents for additional details.

1 Overview

The SPC584Cx/SPC58ECx devices implement only the MBIST. It can detect latent faults in the volatile memory of the device. SPC584Cx/SPC58ECx include 57 memory cuts. The reader can see the complete list in the chapter 7 (Device configuration) of the reference manual.

2 Self-test configuration

Self-test can run either in online or offline mode. To reach the best trade-off in terms of consumption and execution time, we recommend dividing the MBISTs in 12 splits. The MBISTs inside the same split run in parallel mode.

Note: with the exception of the split 11, where the partition runs in sequential mode.
These 12 splits run in sequential mode.

The complete list of the MBISTs and its split are contained in the Microsoft Excel® workbook file attached to this document, see “SPC58ECx_split.xlsx”.

Locate the paperclip symbol on the left side of the PDF window, and click it. Double-click on the Excel® file to open it.

2.1 DFC list for offline configuration

MBISTs can run in offline mode up 180 Mhz as max frequency. The list of the DCF has to be configured in order to start up the MBIST during the boot phase (offline mode), it is contained in the Microsoft Excel® workbook file attached to this document, see “SPC58ECx_DCF_rev2”.

Locate the paperclip symbol on the left side of the PDF window, and click it. Double-click on the Excel® file to open it.

MBISTs run in full run mode in order to reach the maximum diagnostic coverage.

They take around 45 ms.

2.2 Monitors during self-test

Two different phases impact the self-test execution (See reference manual RM0407, see Section A.1 Reference documents).

1. **Initialization (configuration loading)**
   The SSCM (offline mode) or the software (online mode) configures the BISTs by programming the STCU2.
2. **Self-test execution**
   The STCU executes self-test.

Two different watchdogs monitor these phases.

- ***Hard-coded watchdog*** monitors the “initialization” phase.

It is a hardware watchdog configured at 0x3FF. The user cannot modify it.

The clock of the hard-coded watchdog depends on the operating mode:

  - IRC oscillator in offline mode
  - STCU clock in online mode

- ***Watchdog timer (WDG)*** monitors the “self-test execution.”

It is a hardware watchdog configurable by the user (STCU_WDG register). The user can check the status of the STCU WDG after the BIST execution in the STCU_ERR_STAT register (WDTO flag).

The clock of STCU WDG depends on the operating mode:

- It is configurable by the STCU_PLL (IRC or PLL0) in offline mode
- It is configurable by software in online mode

2.2.1 Hard-coded watchdog refresh during initialization

The Hard-coded watchdog timeout is 0x3FF clock cycles.

The SSCM or the software must periodically refresh the hard-coded watchdog by programming the STCU Key2.

To perform this operation, the user must interleave the list of DCF records (offline mode) or the writing accesses to the STCU registers (online mode) with a write to the STCU Key2 register.

In the case of offline BIST, a single write of a DCFrecord takes around 17 clock cycles.

Since the hard-coded watchdog expires after 1024 clock cycles, the user must refresh it every 60 DCF records.

Note: the watchdog expires after 1024 clock cycles. A single DCF write takes 17 clock cycle. The STCU accepts up to 60 DCF records before the hard-watchdog expires (1024/17=60).

In the case of online BIST, the refresh time (STCU key 2 writing) is application dependent.

2.3 Online mode configuration

In online mode, the split list remains the same with some limitations due to life cycle. All MBIST can run in online mode only in ST production and Failure Analysis (FA). In the other life cycle, HSM MBIST and FLASH MBIST are not accessible. Also in this case the maximum frequency is 180 Mhz, provided by the sys_clock. In that case STCU registers can be configured with the "register value" column of the DCF list file.

3 Summary

In SPC584Cxx/SPC58ECx devices, user can only run MBIST, both in offline and online mode with the same setting:

- frequency setting
- MBIST Algo
- MBIST sequence (split list)

Appendix A Other information

A.1 Reference documents

Table 1. **Reference documents**

Doc name	ID	Title
RM0407	028117	SPC58 C Line- 32 bit Power Architecture automotive MCU Dual z4 cores 180 MHz, 4 MBytes Flash, HSM, ASIL-B Reference Manual
AN4551	026636	SPC574K72xx self-test procedures

A.2 Acronyms

Table 2. **Acronyms**

Acronym	Name
MBIST	Memory built-in self-test
LBIST	Logic built-in self-test
STCU2	Self-test control unit
HSM	Hardware system module
LC	Life cycle
DCF	Device configuration format (DCF) records
UTest	User test Flash block
FA	Failure analysis

Revision history

Table 3. **Document revision history**

Date	Version	Changes
23-Aug-2019	1	Initial release.
04-Nov-2021	2	Add the root part number SPC584Cxx. Add a new file SPC58ECx_DCF.
07-Mar-2022	3	Add a new file SPC58ECx_DCF and a new paragraph Section 2.2 Monitors during self-test

Contents

List of tables