Technical note

# SPC58EHx/SPC58NHx OctalSPI IO manager

## Introduction

This technical note aims to provide more details about the IO manager implemented for the OctalSPI peripheral embedded inside the SPC58EHx/SPC58NHx microcontrollers.

More details about the OctalSPI can be found in the RM0452 reference manual of the device and in the AN5524 application note.

# 1 SPC58EHx/SPC58NHx OctalSPI instances

This microcontroller embeds two OctalSPI instances and each instance has its own chip select pin. The Table 1 shows the memory map layout:

**Table 1. OctalSPI memory map**

| Instance | Description | Address space |
|---|---|---|
| OctalSPI 1 | Memory mapped | 0x70000000 - 0x7FFFFFFF |
| | Controller registers | 0x80000000 - 0x800003FF |
| | Delay block | 0x80000400 - 0x80000407 |
| OctalSPI 2 | Memory mapped | 0x60000000 - 0x6FFFFFFF |
| | Controller registers | 0x80001000 - 0x800013FF |
| | Delay block | 0x80001400 - 0x80001407 |

The two OctalSPI instances share the same data lines to reduce the number of signals and a dedicated IO manager is used to multiplex them.

The IO manager is mapped at 0x80002000 - 0x8000200B address space.

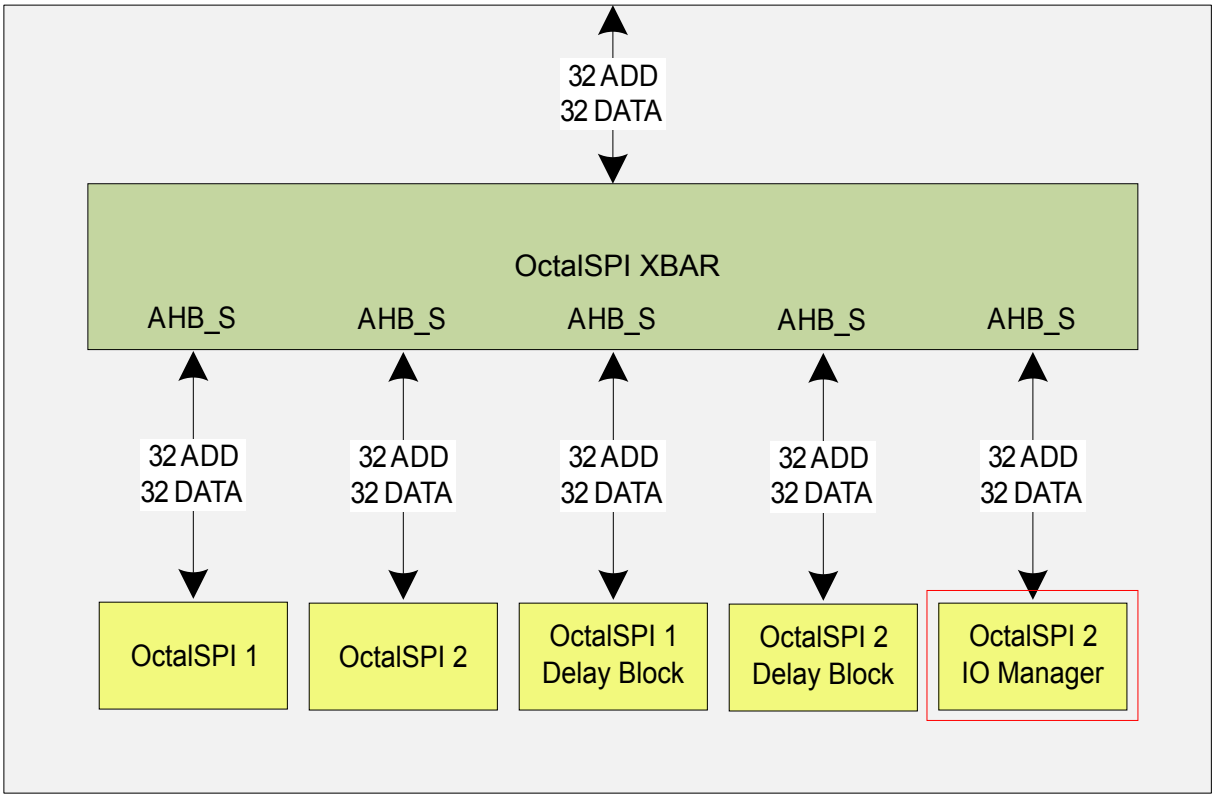
# 2 IO manager

The OCTOSPI I/O manager allows the user to set a fully programmable pre-mapping of the OCTOSPI1 and OCTOSPI2 signals.

Any internal port signal can be mapped independently to the OCTOSPI1 or OCTOSPI2.

The two instances cannot work simultaneously.

**Figure 1. OctalSPI sub-system**



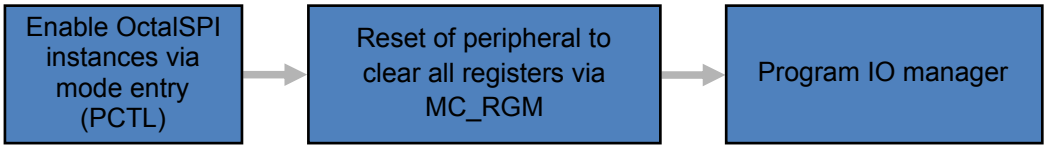

The following setting enables the multiplexing of the two OctoSPI. This can be done before initializing and enabling the devices by programming only one bit in the register below:

*OCTALSPI_IOM.IOM_CR.R = 1U*

No exception/error response is generated on access to the reserved space of OctalSPI.

The Figure 2 shows a basic initialization that can be implemented before enabling the devices.

**Figure 2. Initialization before enabling the OctalSPI instances**



# 3 Hardware example

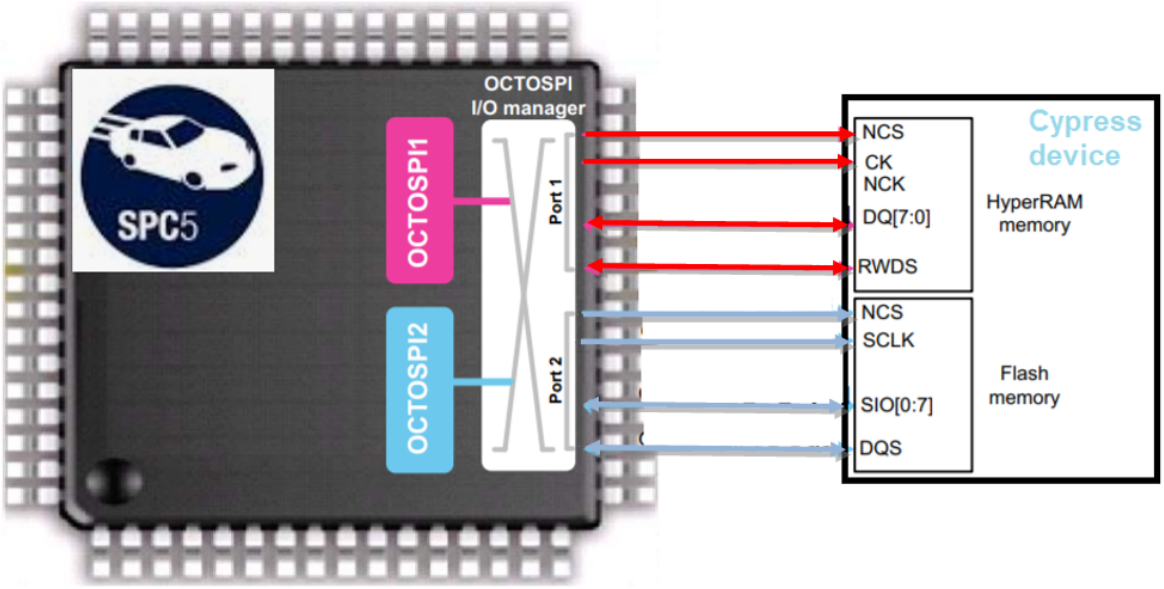
The SPC58NHADPT302S application board used for testing embeds the S71KL256SC0BHB000 by Cypress that is an HyperFlash™ and HyperRAM™ multi-chip package composed of:

- S26K HyperFlash device
- S27K HyperRAM device

In this hardware the following configuration is used by default:

- HyperRAM memory linked to OCTOSPI1 and Flash memory linked to OCTOSPI2
- HyperRAM memory linked to OCTOSPI2 and Flash memory linked to OCTOSPI1

**Figure 3. SPC58NHADPT302S wiring schema**




*Note: The IO manager implementation embedded in this microcontroller does not support any multiplexed mode feature. This can be optionally found in some other platforms to allow both instance signals to be muxed over one port so having a configurable arbitration system for two external memories. Then the arbitration system can be configured with MAXTRAN[7:0] field in OCTOSPI_DCR3 register.*

# Appendix A Reference documents

**Table 2. Reference documents**

| Document name | Document title |
|---|---|
| RM0452 | SPC58 H Line - 32 bit Power Architecture automotive MCU Triple z4 cores 200 MHz, 10 MBytes Flash, HSM, ASIL-D |
| AN5524 | SPC58EHx/SPC58NHx OctalSPI HyperBus |

## Revision history

Table 3. **Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 22-Jun-2021 | 1 | Initial release. |

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