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TN1366

Technical note

How to reduce the effect of the injected current on SAR ADC

Introduction

This document serves as an addendum for the existing errata DAN-005632 (applicable to SPC58 G and E lines) and DAN-005633 (applicable to SPC58N line). These erratas are part of the standard device errata sheets (see Section 5 Reference documents). Nevertheless, the complexity of the topic is beyond what the standard errata sheet allows to show. Therefore, the details are shown in this document. It is shown the scenario and the explanation of the erratum, and a detailed explanation of workarounds #2 and #3.

1 Overview

The internal structure of the overall SAR ADC system, joined channel multiplexer and sampling switches, causes performance accuracy degradation on certain SAR channels while injecting current on a different channel. This happens due to the common net between different SAR units to allow the usage of common test channels.

This degradation can be reduced. The following chapters will show the procedures.

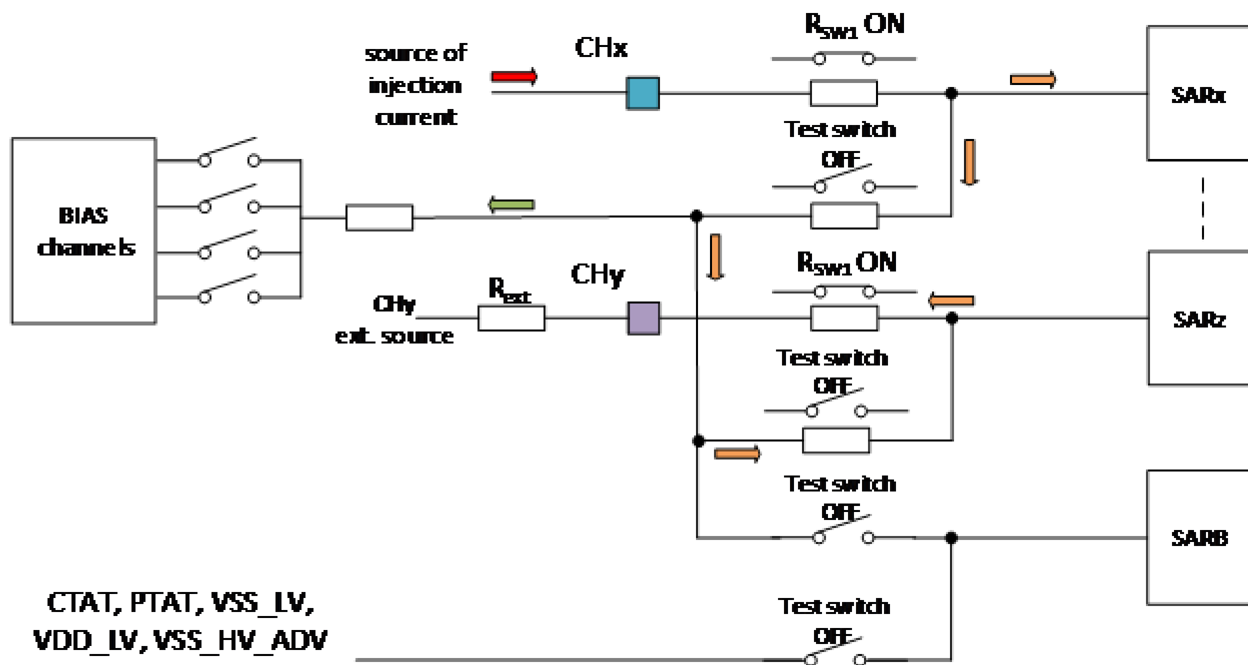
2 Injection scenario

The following figure depicts the block diagram of the complex SAR ADC system with several SAR ADC units and internal analogical structure.

There is a current injection on a channel *CHx* selected on SARx. Simultaneously a channel *CHy* is selected and converted by *SARz*. The external series resistance Rext on channel *CHy* is very high, at the order of kOhms. Some of the injected current from Channel *CHx* will reach channel *CHy* in the form of leaked current through the internal test switch. This current will be sunk by the external source connected to channel *CHy*. As there is the external resistance the leakage current also passes through this resistance, which leads to generation of a voltage drop across it. An additional error on the TUE is generated.

Note: *there can be positive or negative injection. Therefore the direction of the current can turn vs. what is shown below in the picture.*

Figure 1. Injection scenario block diagram



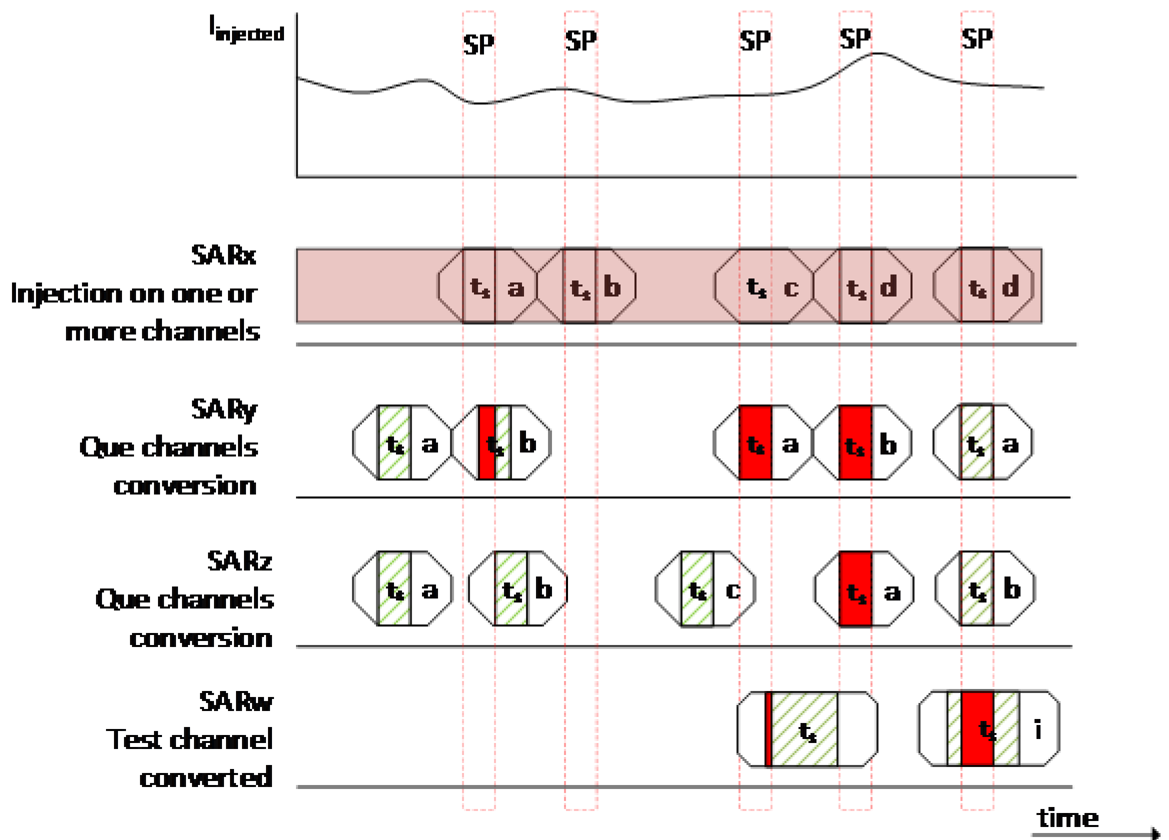
As depicted in Figure 1. Injection scenario block diagram the leakage current can also reach the ADC BIAS channels. This implies the degradation of TUE if the ADC BIAS channels are simultaneously converted while injecting current on *CHx* .

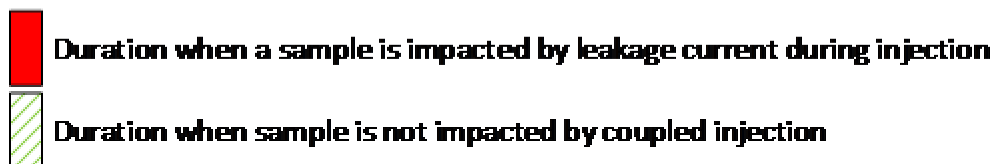
2.1 Condition when a degradation can happen

The injected current can impact another channel only if the sampling phase of the channel experiencing the injection and the sampling phase of another channel or ADC BIAS overlap. The precharge and discharge phases are not relevant.

Note: *in case, more than one channel is under injection condition, the duration of the impact on the other channels is extended accordingly.*

Figure 2. Leakage current application to ADC channels





SP – Sampling phase of a channel on SARx -> where injection current is present
ts – sampling time configured by application
a, b, c, d – example name of converted channels. In reality it can be any.

The errata is applicable only if the selection switch is closed in the injected channel and both the selection and sampling switches are closed in the impacted channel. Only the sampling phase duration is mentioned in the errata, since the selection and sampling switches of a given channel are driven by a single signal, so they open and close simultaneously. As the selection and sampling time are the same, the errata only refers to the latter.

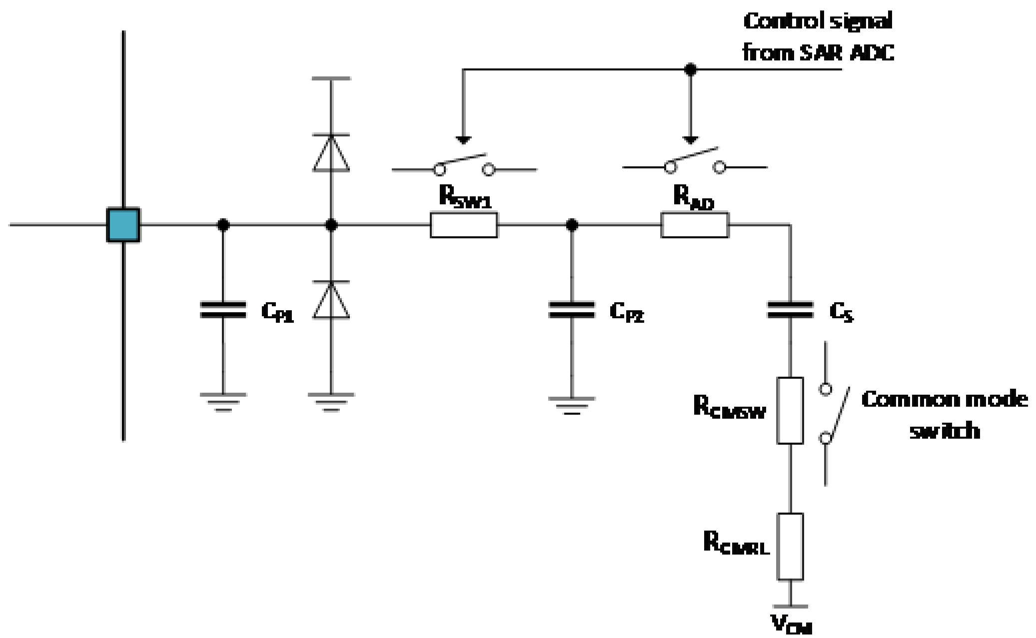


Figure 3. Controlling of selection and sampling switches

3 Workaround implementation and functionality

3.1 Workaround 2 – converting ADCBIAS channel

Since ADCBIAS channels can be impacted by leakage current, this effect can be used by the application to reduce the degradation on the standard channels converted.

The reduction becomes more and more effective as the sampling steps of the BIAS ADC and the impacted channel overlap. Ideally, the ADC BIAS sampling phase lasts as long or longer than that of the affected channel and the conversions are synchronized.

There is no recommendation on which ADC BIAS channel should be selected

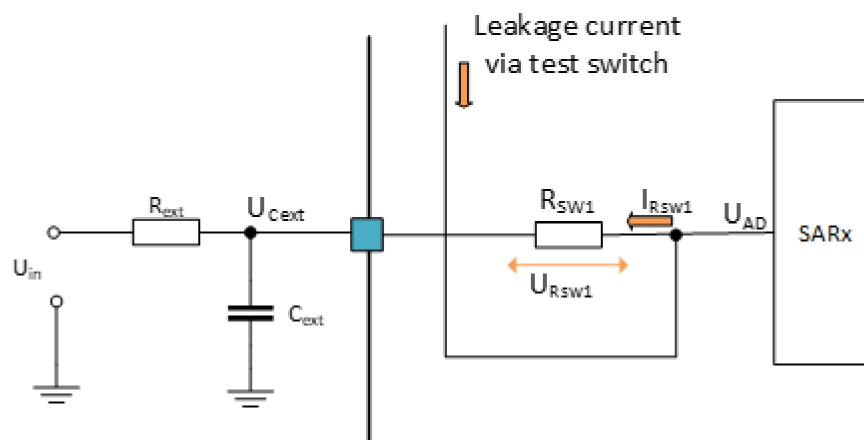
Table 1. **List of applicable ADC BIAS for WA#2**

SAR_ADC_12bit_B0 input channel	Fast SAR	Fast SAR channel	Description
124	SAR_ADC_12bit_0 SAR_ADC_12bit_1 SAR_ADC_12bit_2 SAR_ADC_12bit_3 SAR_ADC_10bit_0 SAR_ADC_10bit_1	124	SAR BIAS 0 - VSS_HV_ADR_S through 20 KΩ source impedance
125		125	SAR BIAS 1 -1/3 (VDD_HV_ADR_S - VSS_HV_ADR_S) through 20 KΩ source impedance
126		126	SAR BIAS 2 -2/3 (VDD_HV_ADR_S - VSS_HV_ADR_S) through 20 KΩ source impedance
127		127	SAR BIAS 3 - (VDD_HV_ADR_S - VSS_HV_ADR_S) through 20 KΩ source impedance

3.2 Workaround 3

An external customer capacity connected to an analog pin may be used for the elimination of the degradation. The principle is shown in the following figure.

Figure 4. **Principle of external capacity**



Where:

U_{Cext} – voltage on C_{ext}

U_{AD} – voltage which is being sampled/converted

U_i – voltage of application signal

U_{Rsw1} – maximum voltage drop of 3 mV specified on channel selection switch

I_{Rsw1} – maximum current of 5 µA specified for the analog channel

The workaround consists in the right design of the external components, especially the capacitor. The aim of this workaround is the elimination of the leakage current to go through R_{ext} which is too big and would cause very high voltage drop. The current needs to be charged into $C_{ext.}$. The following equations can be used for it. The equations are functions of time which introduce sampling time as decisive factor here.

$$Q = U_{Cext} \times C_{ext} = I_{Rsw1} \times t_{sampling} \quad (1)$$

$$U_{Cext}(t) = U_{Cext}(0) + \sum_{t=1}^{t=n} Q/C_{Ext} \quad (2)$$

where t (1;n) = number of conversions done. The final voltage is:

$$\Delta U_{AD}(t) = U_{Cext}(t) + U_{Rsw1} \quad (3)$$

3.2.1 Example of the application voltage drop evaluation

This example shows how the final voltage drop at U_{AD} point can be computed. For simplicity's sake the *t(0)* will be used.

Let’s consider this application configuration:

C_{Ext}- 10 nF

R_{Ext} -higher than the maximum of 0.4 kΩ specified by the erratum

t_{samp}- 800 ns

$$Q = I_{Rsw1} \times t_{sampling} = 5uA*800ns = 4pC \quad (4)$$

$$U_{Cext}(0) = Q/C_{Ext} = 4pC/10nF = 0.4mV \quad (5)$$

$$\Delta U_{AD}(0) = \Delta U_{Cext}(0) + \Delta U_{RSW1} = 0.4mV + 3mV = 3.4mV \quad (6)$$

3.2.2 Conclusion

Considering an input signal that ranges between 0 and 5 V and an internal device capacity (Cp2 + Cs) charged during sampling of 1 *pF* + 5 *pF* maximum, the required charge is 30 *pC*.

This means that the external filter must be designed to make sure that a 30 *pC* charge does not cause accuracy degradation at the pin. This way, the 4 *pC* can be nearly seen as negligible.

4 Summary

There are two effectively applicable workarounds.

Workaround #2 which requires strict timing synchronization which might not be possible for all applications.

Workaround #3 which requires correct and sufficient size of external capacitor and the shortest possible sampling phase configured. This workaround is in most cases already implemented in every customer application where the capacitors in order of tens of *pF* up to tens of *nF* serve as input filter.

5 Reference documents

- SPC58xNx Reference manual, RM0421
- SPC584Nx, SPC58ENx, SPC58NNx Datasheet, DS11734
- SPC58EEx, SPC58NEx Datasheet, DS11646
- SPC58xEx/SPC58xGx Reference manual, RM0391
- SPC584Gx, SPC58EGx, SPC58NGx Datasheet, DS11758
- SPC58xGx devices errata JTAG_ID = 0x1111_0041, ES0399
- SPC58xEx device errata JTAG_ID = 0x1111_0041, ES0397
- SPC584Nx, SPC58ENx, SPC58NNx devices errata JTAG_ID = 0x2011_2041, ES0476

6 Acronyms and abbreviations

Table 2. Acronyms

Abbreviation	Complete name
SARADC	Successive Approximation Register Analog-to-Digital Converter

Revision history

Table 3. Document revision history

Date	Version	Changes
14-Jan-2022	1	Initial release.

Contents

1 **Overview** 2

2 **Injection scenario** 3

2.1 Condition when a degradation can happen 3

3 **Workaround implementation and functionality** 6

3.1 Workaround 2 – converting ADCBIAS channel 6

3.2 Workaround 3 6

3.2.1 Example of the application voltage drop evaluation 7

3.2.2 Conclusion 7

4 **Summary** 8

5 **Reference documents** 9

6 **Acronyms and abbreviations** 10

Revision history 11

Contents 12

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