

Power on reset conditions for EEPROM manufactured in CMOSF9V

Introduction

The purpose of this technical note is to define the power supply conditions that ensure a correct reset of the CMOSF9V EEPROM devices listed in Table 1.

New high density of EEPROM (electrically erasable programmable read-only memory) devices are manufactured with new advanced CMOSF9V technology. They offer low power consumption, high speed, flexibility, footprint optimization, configurable device address, and software write protection.

To ensure the proper operation of an EEPROM, the power supply voltage V_{CC} should be within an acceptable operation range before executing the instructions. Before that, a certain sequence of events must happen, and it begins with the power on reset (POR) signal.

This technical note describes three types of events:

- Controlled power-up.
- · Uncontrolled supply voltage drop.
- Controlled power-down.

Table 1. Applicable products

Series	RPNs
Standard serial EEPROM	M24256E-F
	M24256X-F
	M24512E-F
	M24M01E-F
	M24M02E-F
	M95M04-DR



1 Supply voltage specification

The correct use of the V_{CC} supply voltage for the M24xxxE-F, M24xxxX-F and M95M04-DR EEPROM (hereinafter collectively referred to as M24xxx / M95M04) is defined in the datasheets as in the following chapters.

1.1 Operating supply voltage (V_{CC})

A valid and stable V_{CC} voltage within the specified [V_{CC} (min), V_{CC} (max)] range must be applied before selecting the memory and issuing instructions to it. This voltage must remain stable and valid until the end of the transmission of the instruction and until the end of the internal write cycle (t_W) for a write instruction. To ensure a stable DC supply, it is recommended to decouple the V_{CC} line with a suitable capacitor (from 10 nF to 100 nF) placed close to the V_{CC}/V_{SS} package pins.

1.2 Power-up conditions

When the power supply is switched on, the V_{CC} voltage must rise continuously from 0V to the minimum V_{CC} operating voltage defined in Table 2. A power-on-reset (POR) circuit is incorporated to prevent accidental write operations during power-up. On power-up, the device does not respond to any instruction until V_{CC} reaches the internal reset threshold voltage (this threshold is defined in Table 2 as V_{RES}). When V_{CC} crosses the V_{RES} threshold, the device is reset and is in the following state:

- Standby power mode
- Deselected

1.3 Power-down conditions

During power-down (continuous decrease of the V_{CC} supply voltage below the V_{CC} (min) operating voltage defined in Table 2), the device must be in standby power mode. To avoid accidental operations during power-down, the power-on-reset (POR) circuit is active and as soon as V_{CC} reaches the internal reset threshold voltage. The device is reset and does not respond to any command (this threshold is defined in Table 2 as V_{RES}).

Symbol	Description	Value	Unit
V _{CC} (max)	County well-are record for correct or creation of the NAC trave EV. Endowing	5.5 ⁽¹⁾	
V _{CC} (min)	Supply voltage range for correct operation of the M24xxxE/X-F device		
V _{CC} (max)	Supply valters range for correct exercises of the MOEMOA DD device	5.5	V
V _{CC} (min)	Supply voltage range for correct operation of the M95M04-DR device		
V _{RES}	Reset threshold voltage		

Table 2. Values used in this document

1. 3.6 V for M24256X-F

TN1496 - Rev 1 page 2/13

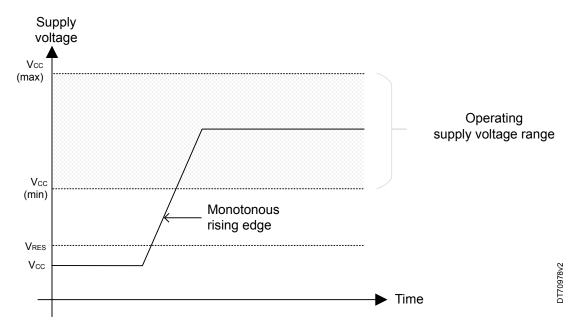


2 Controlled power-up

At power-up, the following parameters must be considered when defining the reset behavior (as shown in Figure 1).

- The lowest supply voltage (below V_{RES})
- The supply voltage rising edge
- V_{CC} operating supply voltage range (between V_{CC}(min) and V_{CC}(max))

Figure 1. Correct M24xxx/M95M04 power-up



Note: The internal reset circuit operates correctly under the following conditions before and during power-up.

- The M24xxx/M95M04 remain not selected⁽¹⁾ and all input signals should remain static, at either V_{IL} or V_{IH} , during the following steps:
 - The supply voltage starts from a voltage lower than V_{RES}
 - The supply voltage rising edge is monotonous (2)
 - The supply voltage rises up above V_{CC}(min), remains stable, and does not exceed V_{CC}(max)
- The ambient temperature is within the specified temperature range (-40 °C to 85 °C)
- M95M04-DR (SPI bus) is selected by driving low the chip select input and deselected by driving high the chip select input. M24xxx (I²C-bus) EEPROM is selected after a start condition and deselected after a stop condition.
- 2. The V_{CC} pin has to be decoupled with a capacitor (usually in the range between 10 nF and 100 nF), this decoupling capacitor is efficiently helping for a continuous edge.

Note:

The internal logic of the M24xxx/M95M04 device is reset when the rising edge passes through V_{RES} , so the device must not be selected while V_{CC} is rising above V_{RES} to avoid decoding any uncontrolled events that may occur on the serial bus.

TN1496 - Rev 1 page 3/13



3 Uncontrolled supply voltage drop

The induced effects on the M24xxx/M95M04 units when the supply voltage drops can be studied under two headings:

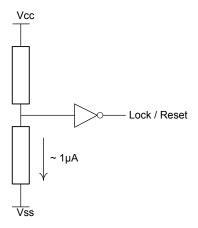
- Uncontrolled drop of the supply voltage below V_{RES} (Section 3.2)
- Uncontrolled drop of the supply voltage above V_{RES} (Section 3.3)

3.1 Overview of the reset function

In the M24xxx/M95M04 devices, the reset circuitry continuously compares the voltage applied to the V_{CC} pin with the internal voltage reference (V_{RES}), the reset threshold voltage.

As long as V_{CC} is lower than V_{RES} , the device logic is locked and in reset mode. When V_{CC} becomes higher than V_{RES} , the internal logic is unlocked. A simplified schematic of the POR circuit is shown in Figure 2.

Figure 2. Simplified schematic of reset circuit



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TN1496 - Rev 1 page 4/13



3.2 Power supply drop below the reset threshold voltage (V_{RES}) inducing the reset

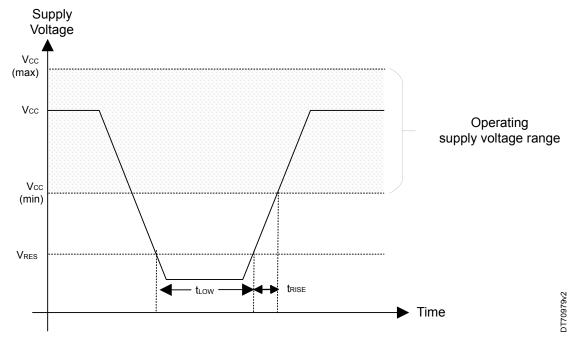


Figure 3. Correct reset after a power supply drop

Note:

- t_{RISE} must be monotonous.
- During V_{CC} rise time, the internal device logic is reset when the rising edge passes through V_{RES} .

The M24xxx/M95M04 are always reset under the following conditions:

- The supply voltage continuously falls below V_{RES} (1)
- The supply voltage remains lower than V_{RES} for at least 50 μ s ($t_{LOW} > 50 \mu$ s)
- The supply voltage rises up above $V_{CC}(min)$, but does not exceed $V_{CC}(max)$
- The supply voltage rising up is monotonous (1)
- The ambient temperature remains inside the specified range⁽²⁾
- 1. The V_{CC} pin has to be decoupled with a capacitor (usually in the range between 10 and 100 nF), this decoupling capacitor is efficiently helping for a continuous edge.
- 2. The temperature range is -40 °C to 85 °C.

During the rising edge of the supply voltage (voltage range V_{RES} to $V_{CC}(min)$) the internal logic of the M24xxx/M95M04 is reset and not locked. Therefore, the M24xxx/M95M04 must not be accessed (that is, the device must not be selected and all input signals must remain static at either V_{IL} or V_{IH}).

Note:

If the device is still performing an internal write cycle when the supply voltage drops below V_{RES} , the data in the addressed locations performing the write cycle are not written correctly.

TN1496 - Rev 1 page 5/13



3.3 Power supply drop above the reset threshold voltage (V_{RES})

3.3.1 Device not selected

A full reset is required to put the device in a proper reset state after a questionable or unknown state. For example:

During a controlled power up

Or

 When the bus controller is not able to exchange information correctly during or after a highly disturbed environment.

When the device is in standby mode (not selected), if the supply voltage falls below $V_{CC}(min)$ but remains above V_{RES} (see Figure 4) and then rises back to a stable V_{CC} value, it is not necessary to reset again if all the internal logic blocks have remained in the previous well-defined state.

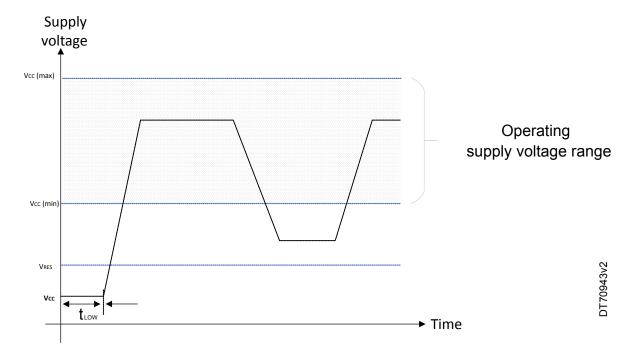


Figure 4. Power supply drop above the reset threshold V_{RES}

The corresponding sequence is (see also Figure 4):

- The M24xxx/M95M04 is properly reset (as described in Section 3.2)
- The M24xxx/M95M04 is not selected (in standby power mode, not during a write cycle)
- The supply voltage decay is monotonous (no ripple during the decay)
- The supply voltage is stable and above V_{RES} (V_{CC}>V_{RES})
- The supply voltage rises up above V_{CC}(min), but does not exceed V_{CC}(max)
- The supply voltage rising edge is monotonous (no ripple during the rise)
- The ambient temperature remains inside the specified range (-40 °C to 85 °C)

After such a sequence, the internal logic of the M24xxx / M95M04 keeps its state and it is set back to its previous state (the one before the supply voltage dropped)..

This new state is:

- in standby Power mode with the Status register keeping its previous value for the M95M04-DR
- in standby Power mode with the address pointer keeping its previous value for the M24xxxE-F, M24xxxX-F

The M24xxx / M95M04 are then ready to decode any new incoming instruction.

TN1496 - Rev 1 page 6/13



3.3.2 Device is selected

If the M24xxx / M95M04 are selected (1) and are transmitting data when the supply voltage drops below V_{CC} (min) but remains above V_{RES} (as shown in Figure 4), the M24xxx / M95M04 are not reset (and selected), the uncontrolled logical levels applied on the M24xxx / M95M04 inputs could be incorrectly decoded (as the supply voltage is below V_{CC} (min)): the M24xxx / M95M04 functionality cannot be guaranteed.

1. The M95M04-DR (SPI bus) EEPROM is selected by driving low the chip select input, the M24xxx (I²C-bus) EEPROM is selected after a START condition.

The corresponding sequence is (see also Figure 4):

- The M24xxx / M95M04 is properly reset (as described in Section 3.2: Power supply drop below the reset threshold voltage (V_{RES}) inducing the reset)
- The M24xxx / M95M04 is selected
- The supply voltage decay is monotonous (no ripple during the decay)
- The supply voltage remains stable and above V_{RES} (V_{CC}>V_{RES})
- The supply voltage rises up above V_{CC}(min), but does not exceed V_{CC}(max)
- The supply voltage-rising edge is monotonous (no ripple during the rise)
- The ambient temperature remains inside the specified range (1)
- 1. The temperature range is 40 °C to 85 °C.

The M24xxx / M95M04 functionality cannot be guaranteed, however when the supply voltage is back to a stable V_{CC} value after the supply voltage drop, the M24xxx / M95M04 can decode a new command.

This is because the new command begins with a select event, which selects the device but it is important to notice the following additional functionality:

Case 1: the voltage supply is back to a stable DC value, within the specified V_{CC} operating values and the M24xxx / M95M04 is not running a write cycle:

- M95M04-DR: before decoding the new command (initiated with a select event), the device was not selected. When not selected, the device is always partially reset (all internal logical blocks are reset, except the status register and the logic monitoring a write cycle): a new command will therefore access a partially reset device.
- M24xxx: before decoding the new command (initiated with a start condition), the device was not selected. When not selected, the part is always partially reset (all internal logical blocks are reset, except the address pointer content and the logic monitoring the write cycle): a new command accesses a partially reset device.

Case 2: the voltage supply is back to a stable DC value, within the specified V_{CC} operating values but the M24xxx / M95M04 is running a write cycle:

- M95M04-DR: before decoding the new command (initiated with a select event), the device was not selected. When not selected, the part is always partially reset (all internal logical blocks are reset, except the status register content and the logic monitoring the write cycle); however, for any write cycle, an internal timer automatically resets the logic monitoring the write cycle after a time-out period of approximately 2 t_W. Therefore, after a time of approximately 2 t_W⁽¹⁾, a new command will be safely decoded as the part is partially reset.
- M24xxx: before decoding the new command (initiated with a start condition), the device was not selected. When not selected, the part is always partially reset (all internal logical blocks are reset except, the address pointer⁽¹⁾ content and the logic monitoring a write cycle); however, for any write cycle, an internal timer automatically resets the write cycle logic after a time-out period of approximately 2 t_W. Therefore, after a time of approximately 2 t_W, a new command (initiated with a start condition that is the select event) has to be preceded with a stop condition (deselect event) to properly access the partially reset device.
- 1. T_W = Internal write cycle time

TN1496 - Rev 1 page 7/13



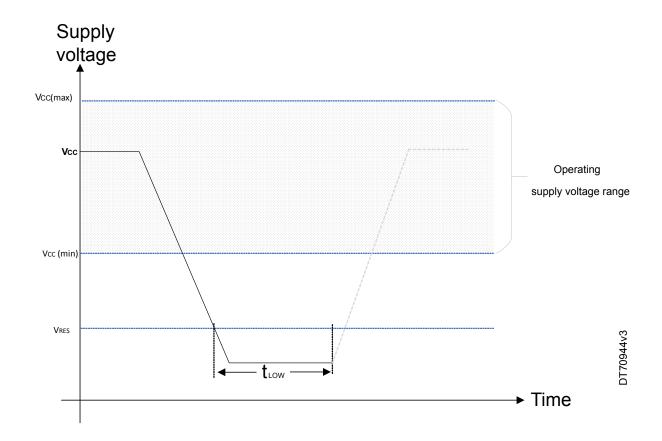
4 Controlled power-down

During a controlled power-down, the application bus controller must deselect the M24xxx/M95M04, to prevent it from attempting to decode any uncontrolled events that might appear on the serial bus.

The reset circuitry runs properly under the following conditions:

- The supply voltage falls lower than V_{RES}(min).
- The supply voltage remains lower than $V_{RES}(min)$ for at least 50 μ s.
- The ambient temperature remains inside the specified range (-40 °C to 85 °C).

Figure 5. Power down conditions



Note: t_{LOW} must be greater than 50 μ s.

TN1496 - Rev 1 page 8/13



Revision history

Table 3. Document revision history

Date	Version	Changes
08-Feb-2024	1	Initial release.

TN1496 - Rev 1 page 9/13



Contents

1	Supply voltage specification			2
	1.1		ting supply voltage (V _{CC})	
	1.2	Power	-up conditions	2
	1.3	Power	-down conditions	2
2	Con	trolled	power-up	3
3	Uncontrolled supply voltage drop			
	3.1		iew of the reset function	
	3.2	Power	supply drop below the reset threshold voltage (V _{RES}) inducing the reset	5
	3.3	Power	supply drop above the reset threshold voltage (V _{RES})	6
		3.3.1	Device not selected	6
		3.3.2	Device is selected	7
4	Con	trolled	power-down	8
Rev	/ision	history		9
Lis	t of ta	bles		11
Lis	t of fig	jures		12





List of tables

Table 1.	Applicable products	1
Гable 2.	Values used in this document	2
Table 3.	Document revision history	ç

TN1496 - Rev 1 page 11/13





List of figures

Figure 1.	Correct M24xxx/M95M04 power-up	3
Figure 2.	Simplified schematic of reset circuit	4
Figure 3.	Correct reset after a power supply drop	5
Figure 4.	Power supply drop above the reset threshold V _{RES}	6
Figure 5.	Power down conditions	8

TN1496 - Rev 1 page 12/13



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TN1496 - Rev 1 page 13/13