# Use of the configurable device address register in CMOSF9V EEPROM product

## Introduction

This technical note is intended to provide guidelines for using the configurable device address (CDA) register for the products listed in Table 1.

New high density of EEPROM (electrically erasable programmable read-only memory) devices are manufactured with new advanced CMOSF9V technology. They offer low power consumption, footprint optimization, configurable device address, and software write protection.

To hook several EEPROM targets on the same I²C bus, CMOSF9V I²C EEPROMs offer a specific software mechanism for the communication with the controller. The user, through the configurable device address register, can set a specific chip enable address value dedicated to the I²C address.

This technical note describes the configurable device address register and how to use and set up this CDA register assuring a correct communication between the controller and the target.

**Table 1. Applicable products**

| Series | Root part number |
|---|---|
| Standard serial EEPROM | M24256E-F |
| | M24256X-F |
| | M24512E-F, M24512X-F |
| | M24M01E-F, M24M01X-F |
| | M24M02E-F, M24M02X-F |

# 1 Introducing the configurable device address (CDA) register

Thanks to the CDA mechanism, software programmable, the CDA register reduces the industry standard 8-pin pinout to a 5-pin pinout. The CDA register controls the three chip enable address bits value. These bits determine which device select code the I²C EEPROM target acknowledges.

STMicroelectronics recommends updating the CDA register exclusively in the manufacturing line. The CDA register must be configured with the values required for the proper use of the application, then must be locked in read-only mode and not to be touched again during the application lifetime.

Even if the default value of the CDA register corresponds to the values desired for the correct operation of the application, STMicroelectronics strongly recommends that the CDA register is locked in read-only mode at the output of the production line.

## 1.1 Correspondence between chip enable address and configurable device address bits

Communication with the I²C CMOSF9V EEPROM begins with an 8-bit device address byte. As multiple target devices can reside on the serial bus, each target device must have its own unique device address programmed in the configurable device address register, so that the controller can access each target independently.

The first four bits contain the device type identifier, followed by three bits containing the chip enable address bits (or the MSB address bit for density higher than 512Kbit). The I²C CMOSF9V EEPROM responds only to the specific device type identifiers, as shown in Table 2. Device select code.

The three chip enable bits correspond to the three configurable device address bits,C2 C1 and C0, inside the CDA register. See Table 3. These bits must correlate with the values programmed in the CDA register. The device responds to all valid device address byte combinations that it receives. .

**Table 2. Device select code**

| Features | Device type identifier bits | | | | Chip enable address (1) or address bit | | | R/W |
|---|---|---|---|---|---|---|---|---|
| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Memory | 1 | 0 | 1 | 0 | C2 | C1(2) | C0(3) | R/W |
| Registers and identification page | 1 | 0 | 1 | 1 | C2 | C1(4) | C0(5) | R/W |

1. *C2,C1 and C0 are compared with the value read on bits b3,b2 and b1 of the CDA register.*
2. *Booked for address bit A17 for 2 Mbit EEPROM density*
3. *Booked for address bit A16 for EEPROM in 1 Mbit and 2 Mbit density*
4. *Don't care bit for 2 Mbit density*
5. *Don't care bit for 1 Mbit and 2 Mbit density*

## 1.2 CDA register description

The configurable device address (CDA) register is a nonvolatile 8-bit register allowing the user to define a configurable device address (with C2, C1, C0 bits) and a specific bit, named device address lock (DAL), to freeze it definitively. Once the desired configurable device address register is set, the register can and must be permanently locked, preventing further changes to device operation.

The CDA offers four nonvolatile bits to configure by the user:

- Three bits for setting the desired configurable address identified as Cn (1) bits
- One bit to definitively freeze in read-only mode the CDA register and identified as DAL bit.

1. *n = 0 to 2 according to the EEPROM density.*

Table 3 describes the configurable device address register:

**Table 3. Configurable device address register**

| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|
| x (1) | x | x | x | C2 | C1(2) | C0(3) | DAL |

1. *X = Don't care. Read as 0*
2. *Don't care for EEPROM in 2 Mbit density*
3. *Don't care for EEPROM in 1 Mbit and 2 Mbit density*

## 1.3 CDA register management

On power-up, the device loads the last configuration from the CDA register. The values of C2, C1 and C0 contained in this register will be the 3 bits of the chip enable address to be set in the 8-bit of the device select code. The EEPROM will only respond ACK after the device select code if the values C2, C1 and C0 match.

### 1.3.1 In case of chip enable address change

If the standard values C2, C1 and C0 do not correspond to the values required for the application to work correctly, the user must change the values C2, C1 and C0.

The user updates the CDA register as long as the DAL bit remains to 0, it means:

- With the DAL bit set-up to 0, the user can update the C2, C1, and C0 and DAL bits as often he wants.
- After writing the C2,C1, and C0 bits with the final value, STMicroelectronics strongly recommends locking the CDA register in read-only mode. This step is carried out by programming the DAL bit to 1.

Once the DAL bit is set to 1, the CDA register update is no longer possible. It becomes permanently frozen and protected.

### 1.3.2 If the chip enable address is maintained

Even if the standard values C2, C1, and C0 correspond to the desired values for the proper operating of the application, STMicroelectronics strongly recommends locking the CDA register in read-only mode. This step is carried out by programming the DAL bit to 1.

Once the DAL bit is set to 1, the CDA register update is no longer possible. It becomes permanently frozen and protected.

### 1.3.3 Information about power supply failure

Power supply loss is critical for an EEPROM device when a write instruction is issued or executed. In this case, the current write request or internal write process in the EEPROM may not have been completed, resulting in data corruption and inconsistency.

The user must therefore ensure that the CDA register is correctly written with the desired values for C2, C1 and C0 without interrupting the power supply while this register is being updated in the manufacturing line.

In the event of power supply loss when writing the CDA register, there is a probability of losing the value of the 7 bits (4 system bits and 3 user bits) of the device select code reserved for register addressing. In this case, the user must plan and deploy a software routine, which makes it possible to find the correct value of the first 7 bits of the device select code (exhaustive search).

# 2 CDA programming

If several targets are on the same bus, each device must have a unique device select code (that is device type identifier and chip enable address) to be accessed individually. See Figure 1.

The CDA register allows the user to modify, in manufacturing line, the chip enable address to give a specific I²C address to the CMOSF9V EEPROM.

Once the correct values of bits C2, C1 and C0 have been programmed, the CDA register must absolutely be permanently locked in read-only mode, by setting the DAL bit to 1.

In the example given in Figure 1, the CMOSF9V EEPROM is a M24512E-F and is identified as target 3.

The 8-bit device address is equal to 1010 001x.

The chip enable address is equal to 001. The corresponding bits C2,C1 and C0 inside the CDA register must be equal to (0;0;1).

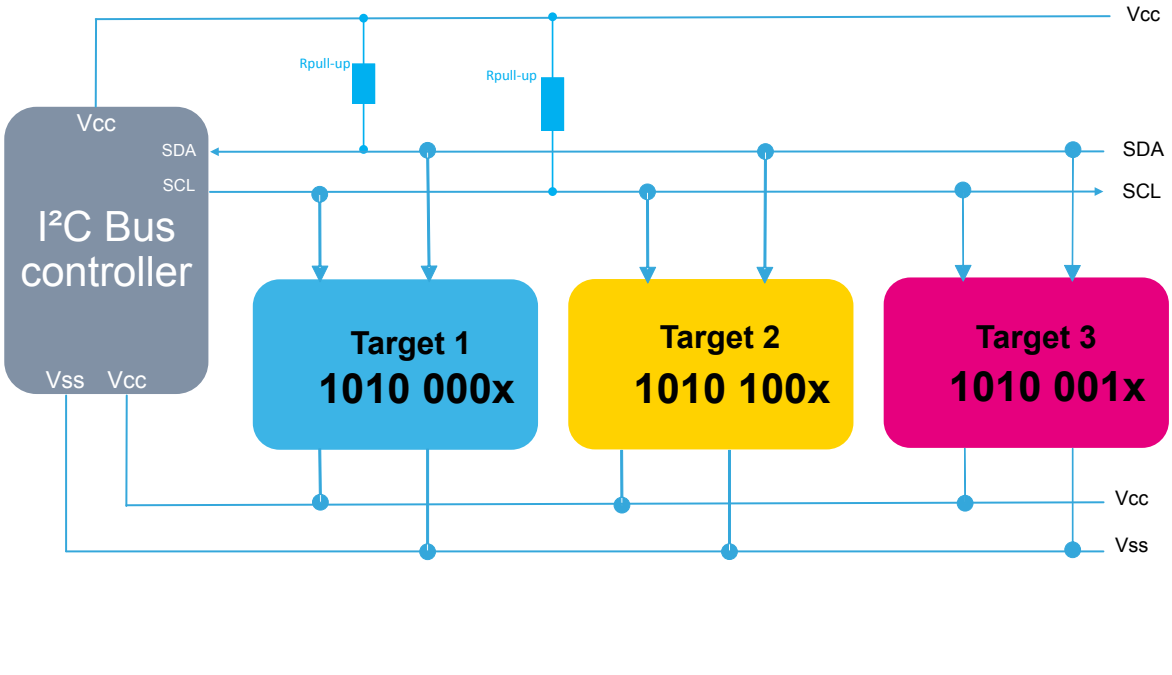
The CDA register must be definitively frozen setting the DAL bit to 1 .

The final value of the CDA register corresponds to 00000011 (0x03):

**Table 4. Example of CDA register value for a M24512E-F**

| bit 7 | bit 6 | bit 5 | bit 4 | bit 3(C2) | bit 2(C1) | bit 1(C0) | bit 0(DAL) |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |

**Figure 1. Configuration of several targets on the same I²C bus**



# 3 Conclusion

At manufacturing step and with a software solution, the user can program the CDA register to configure a specific chip enable address on the EEPROM device.

This software solution allows the user to:

- easily choose the desired I²C address of the EEPROM
- authorize several devices on the same I²C bus
- to avoid conflicts with other targets

## Revision history

Table 5. **Document revision history**

| Date | Version | Changes |
|---|---|---|
| 15-Mar-2024 | 1 | Initial release. |

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