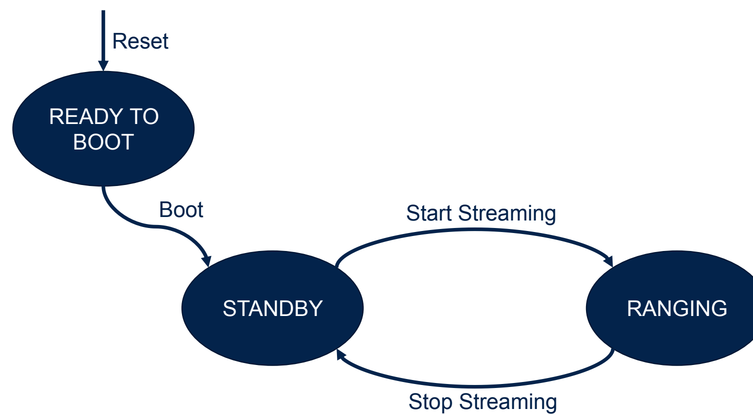
Thermal guidelines when using the VL53L9CX

Introduction

The VL53L9CX module offers many modes of operation that affect power consumption. These modes allow the device to enter different power states. Placing the device in a low-power idle state (STANDBY) consumes significantly less power than continuously ranging (RANGING).

Figure 1. State machine



This document highlights different profile scenarios and the associated power consumed, as well as the power that must be dissipated from the design through heat.

1 Thermal design theory

Thermal resistance (θ) quantifies a material or system's ability to resist heat flow. It represents the expected temperature rise at the hot end of a system (like the silicon die junction) compared to the cool end (like the thermal pad or heat sink) for a given amount of power dissipation. The unit of thermal resistance is degrees Celsius per Watt (°C/W).

The fundamental relationship governing thermal resistance is:

$$\theta = \frac{\Delta T}{P} \tag{1}$$

Where:

- ΔT is the temperature rise (°C).
- P is the power dissipated (W).
- θ is the thermal resistance (°C/W).

When a module is soldered to a PCB (printed circuit board) or flex (flexible circuit), the total thermal resistance of the system is made up of the internal thermal resistance of the module itself and the integration thermal resistance. This relationship is the PCB/flex to ambient condition. It is expressed as follows:

$$\theta_{Total} = \theta_{Module} + \theta_{INT} \tag{2}$$

Where:

- θ_{Module} is the internal thermal resistance of the module.
- θ_{INT} is the integration thermal resistance of the PCB or flex to the ambient condition.

Note: *The thermal resistance through the module's cap is significantly higher than that through the substrate due to the presence of air gaps above the primary heat sources. As a result, heat dissipation through the cap is minimal and is therefore ignored in these calculations. The dominant path for heat dissipation is through the substrate and into the connected system. This assumption simplifies the thermal model while maintaining sufficient accuracy for practical design considerations.*

By combining Eq. (1) and Eq. (2), the expected junction temperature of a module with a single die under steady-state operating conditions can be determined as follows:

$$T_J = T_A + P \times (\theta_{Module} + \theta_{INT}) \tag{3a}$$

Where:

- $T_A$is the ambient temperature (°C).
- P is the power dissipation (W).

Since the module has a defined maximum permissible die junction temperature, Eq. (3a) can be used to determine the required θ_{INT} value to ensure that the system operates within safe thermal limits. θ_{INT} is calculated as follows:

$$\theta_{INT} = \frac{\left(T_{j_{\max}} - T_A\right)}{P} - \theta_{Module} \tag{3b}$$

In modules with multiple heat sources, such as the VL53L9CX, self-heating between die components can significantly impact thermal performance. When one die generates heat, it can transfer thermal energy to adjacent dies, increasing their junction temperatures beyond the expected steady-state values as defined by Eq. (3a). This interdie heating effect must be considered in thermal modeling to check for localized overheating.

The principle of linear superposition accounts for self-heating by modeling the mutual thermal resistances between different heat-generating elements. Each die's temperature is influenced not only by its own power dissipation but also by heat dissipation from neighboring dies (see Eq. (4)).

$$T_{ji} = T_A + \sum_{k=1}^{n} (\theta_{ik} \times P_k + \theta_{INT} \times P_k), i = 1 \ldots n,\ k = 1 \ldots n \tag{4}$$

Where:

- T_{ji} is the junction temperature of the ith die (°C).
- θ_{ik} replaces θ_{Module} and is the thermal resistance of heat escaping from the ith die due to power dissipated on the kth die source (°C/W).
- θ_{INT} is the integration thermal resistance of the PCB or flex to the ambient condition.
- P_k is the power dissipation on the kth die source (W).

Expanding this into a matrix form (Eq. (5)) enables the assessment of each component's thermal behavior to ensure that all junction temperatures remain within permissible limits.

$$\begin{pmatrix} T_{J1} \\ T_{J2} \\ \vdots \\ TJn \end{pmatrix} = T_A + \begin{pmatrix} \theta_{11} & \theta_{12} & \dots & \theta_{1n} \\ \theta_{21} & \theta_{22} & \dots & \theta_{2n} \\ \vdots & \vdots & \ddots & \vdots \\ \theta_{n1} & \theta_{n2} & \cdots & \theta_{nn} \end{pmatrix} \cdot \begin{pmatrix} P_1 \\ P_2 \\ \vdots \\ P_n \end{pmatrix} + \theta_{INT} \begin{pmatrix} P_1 \\ P_2 \\ \vdots \\ P_n \end{pmatrix} \tag{5}$$

Solving for θ_{INT} in a similar manner to Eq. (3b) gives the maximum integration thermal resistance for each die junction temperature to remain below its maximum permissible temperature. Solving for a multiple die module yields a row matrix of permissible θ_{INT} values, one for each die junction. The minimum is selected so that the total system thermal resistance is compatible for all die. The result of this analysis is given in Table 2. Maximum system RTh for a range of use cases and ambient conditions. The end user can select their highest power and highest ambient condition and use the integration thermal resistance target in designing their hardware.

2 Typical power

Current consumption is at its highest during ranging with typical figures for current consumption during ranging recorded as:

- AVDD (2.8 V) = 25 mA
- DVDD (1.2 V) = 65 mA
- IOVDD (1.8 V) = 4 mA
- VBAT (3.3 V) = 100 mA

The frame rate, integration time, ranging mode, and ambient light conditions can be altered depending on the application. They affect the amount of power to dissipate. The table below gives some examples of power consumption in different operating modes. The higher the frequency or the longer the integration time, the higher the power consumption. Integration time must be no higher than the frame period. Any PCB design must consider the worst-case scenario in which the device is to be used. A separate power calculator spreadsheet is available to assist in measuring the power consumption.

Table 1. Typical power consumption for different profiles and conditions

Profile	Frame rate	Exposure	Sunlight equivalent (klx)	Symbol	Power (mW)
Precision mode 54x42	30	10	5	P	350
Ambient mode 54x42	50	16	40		800
Precision mode 24x20	30	5	5		260
Ambient mode 24x20	30	10	40		400
Robotic mode 54x42	20	20	40		500

3 Thermal resistance of system integration

The maximum permitted junction temperature of the VL53L9CX is between 105°C. For a power dissipation of 0.500 W, operating at the maximum specified ambient temperature of 70°C (worst-case scenario), the maximum permitted system thermal resistance is calculated as follows:

Table 2. Maximum system RTh

Parameter	Symbol	Ambient temperature (°C)						Unit
		20	30	40	50	60	70	
Precision mode 54x42	Θ_{INT}	190	170	150	120	100	70	°C/W
Ambient mode 54x42		60	50	40	30	30	20	
Precision mode 24x20		280	240	210	170	140	110	
Ambient mode 24x20		140	120	100	80	70	50	
Robotic mode 54x42		110	90	80	70	50	40	

Note: To ensure that the maximum junction temperature is not exceeded, and to ensure optimum module performance, ST recommends that the above target thermal resistance is not exceeded.

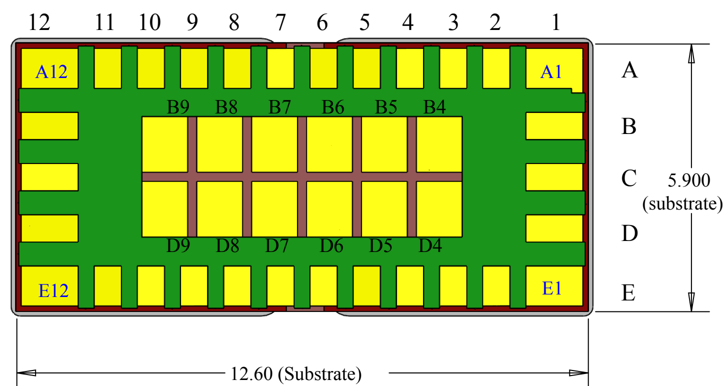
Note: These values are defined at steady state (worst case). If used for a short period of time, less heatsinking is required.

4 Layout and thermal guidelines

Use the following guidelines when designing the module PCB or flex:

- Maximize the copper cover on the PCB to increase the thermal conductivity of the board
- Utilize the module thermal pads B4–B9/D4–D9 shown in the figure below (see the VL53L9CX datasheet for more details) adding as many thermal vias as possible to maximize thermal conductivity into adjacent power planes
- Identify heating components in the application based on their maximum power consumption as they may impact the ToF sensor performance.
- Place the ToF module as far as possible from heat-generating components. However, ignore this step if the heat-generating component does not impact the ToF sensor usage.
- Consider using a good PCB layout design to increase ToF heat dissipation. Refer to the PCB guidelines section of the product datasheet.
- The thermal power dissipation can be assumed to be evenly distributed amongst the thermal pads when calculating the Θ_{INT}.
- Place the device in a low-power state when not in use.

Figure 2. VL53L9CX pinout (bottom view)



Revision history

Table 3. **Document revision history**

Date	Version	Changes
28-Feb-2025	1	Initial release
08-Aug-2025	2	Section 3: Thermal resistance of system integration: Modified maximum temperature to 70°C.
18-May-2026	3	Section 3: Thermal resistance of system integration: Clarified maximum junction temperature is 105°C. Updated values in Table 2. Maximum system RTh. Section 4: Layout and thermal guidelines: Changed Θ_{PCB} to Θ_{INT} in bullet point regarding thermal power dissipation.

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