UM1700

User manual

# SPC56A-Discovery+ Evaluation board

## Introduction

The SPC56A-Discovery+ Evaluation board, here after named SPC56A-DISP, helps you evaluate the SPC56 A line Power Architecture® Microcontrollers.

The discovery board is based on SPC564A70L7, a 32-bit Power Architecture Book E compliant e200z335 CPU core with 1.5 Mbyte on-chip in an LQFP176 package.

The numerous interfaces including CAN/SCI/K-LINE/DSPI/GPIO make the SPC564A-DISP an excellent starter kit for customer quick evaluation and project development.

The SPC56 A line is designed to address cost sensitive powertrain and transmission applications.

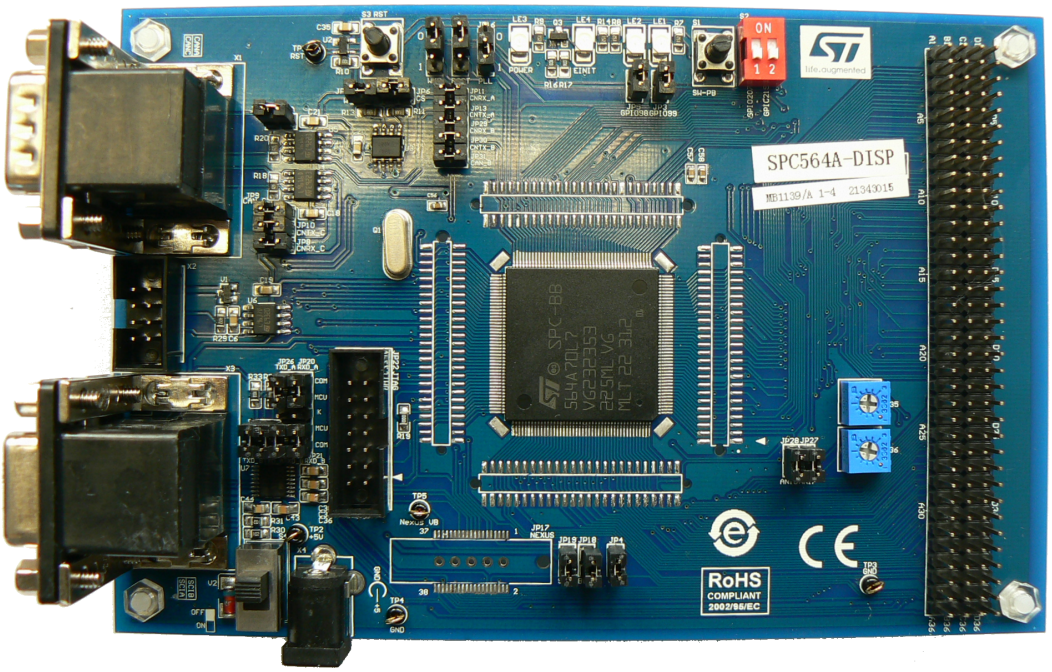
The SPC56 A line key functionality is a Time Processing Unit (eTPU) with a coprocessor to create events in sync with internal or external signals without flooding the CPU with interrupt to serve.

Free ready-to-run application firmware examples are available inside SPC5Studio at www.st.com to support quick evaluation and development.

# 1 SPC564A-DISP with SPC564A70L7

## 1.1 SPC564A-DISP Discovery board

Figure 1. SPC564A-DISP Discovery board



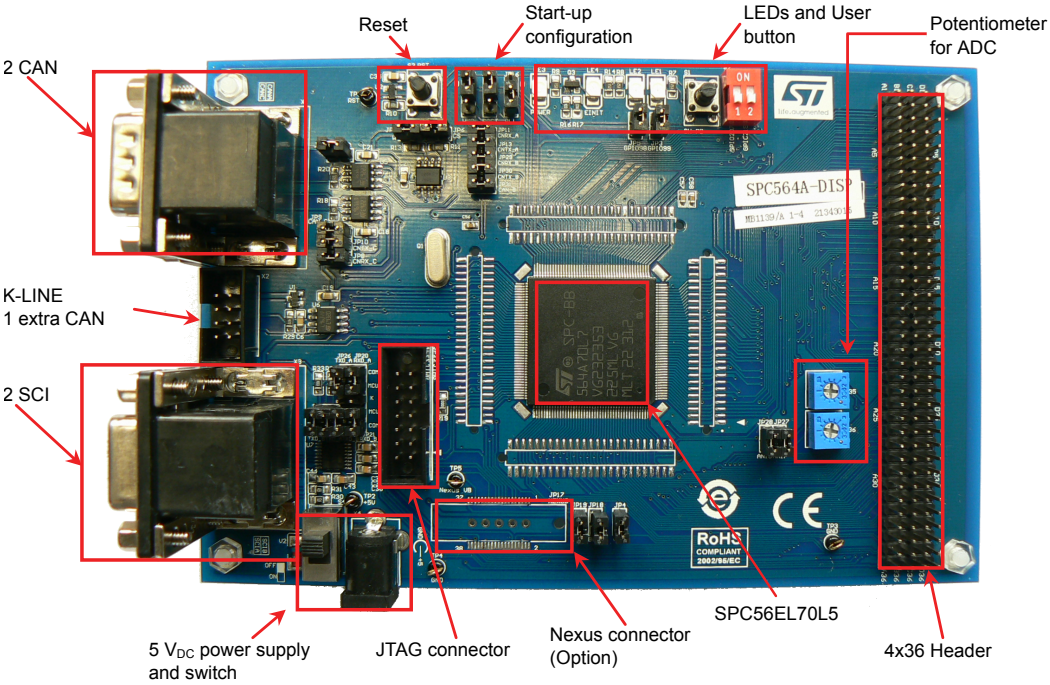

The content of hardware of SPC564A-DISP withSPC564A70L7 consists of:

- SPC564A-DISP Discovery board (see Figure 1);
- Power Supply (Mains: 90-240 $V_{AC}$ - Output: 5 $V_{DC}$).

The PCB, the components and all HW parts assembled in the board meet requirements of the applicable RoHS directives.

# 2 Hardware overview

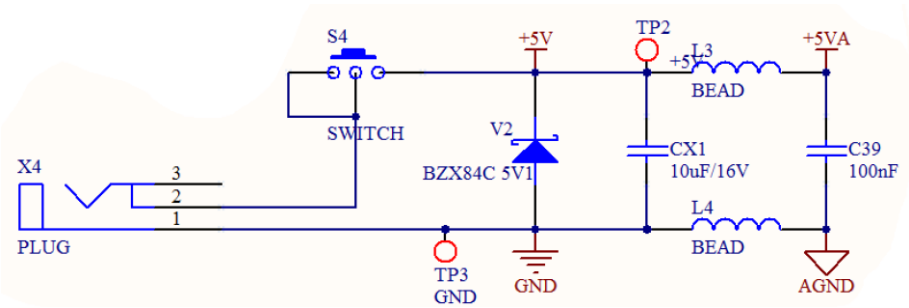
Figure 2. **HW overview**




## 2.1 5 $V_{DC}$ power supply

The 5 $V_{DC}$ voltage is used to supply the whole board including SPC564A70L7 and communication interface transceiver chips. A zener diode, rating 5.1 V, closed to the power supply connector is used to protect the chips for high voltage (wrong connection) in a short time. On the board a slide switch for quickly switching on/off is present.

Figure 3. **PSU Section (+5.0 $V_{DC}$)**




The test point TP2 is available to measure the DC input voltage levels (+5 V) while TP3 is connected to GND.

## 2.2 Device start-up configuration

When the MCU is power-on, it will latch the status of pin WKPCFG, BOOTCFG1 and PLLREF.

- “WKPCFG” determines the weak pull up/down configuration of eMIOS and eTPUpins;
- “BOOTCFG1” is for boot selection;
- “PLLREF” set the source of clock reference input and external circuit related to clock source.

The detailed logic table is the following:

**Table 1. SPC564A-DISP – Device startup configuration**

| | WKPCFG | BOOTCFG1 | PLLREF |
|---|---|---|---|
| 0 - Low | Weak pull down | Boot from internal flash | Clock from external reference |
| 1 - High | Weak pull up | Serial boot from FlexCAN/eSC | Clock from external oscillator |

The evaluation board provides three jumpers, JP14, JP15 and JP16, which can be used by the user to configure the device in different working conditions. The figure below shows a typical configuration of the evaluation board which has only an external crystal oscillator.

**Figure 4. Device start-up configuration**

## 2.3 User LEDs

The board provides four LEDs for device status and monitors GPIO98 and GPIO99 outputs. The detailed information is given in User LEDs here below:

**Table 2. User LEDs**

| Item | Mark | Color | Function |
|---|---|---|---|
| LE1 | - | Green | GPIO99 switching high/low test<br>ON: LOW, OFF: HIGH |
| LE2 | - | Red | GPIO98 switching high/low test<br>ON: LOW, OFF: HIGH |
| LE3 | Power | Green | Turn on when 5 V supply is ON and it is plugged into the socket (X4) |
| LE4 | EINIT | Green | Indication for internal / external RESET<br>OFF: RESET, ON: normal |

**Figure 5. User LEDs**

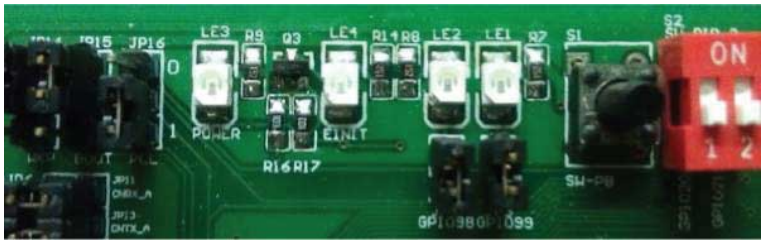


Figure 6. User LEDs - LE1/LE2 (schematic diagram)

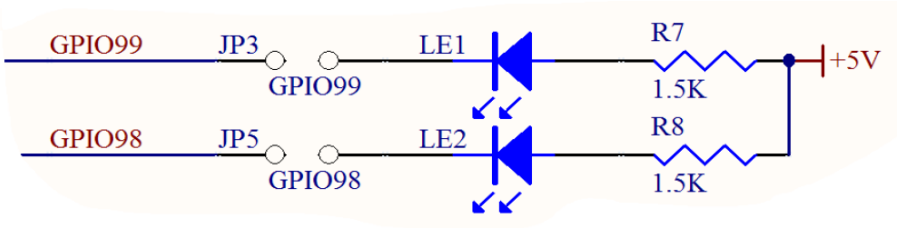
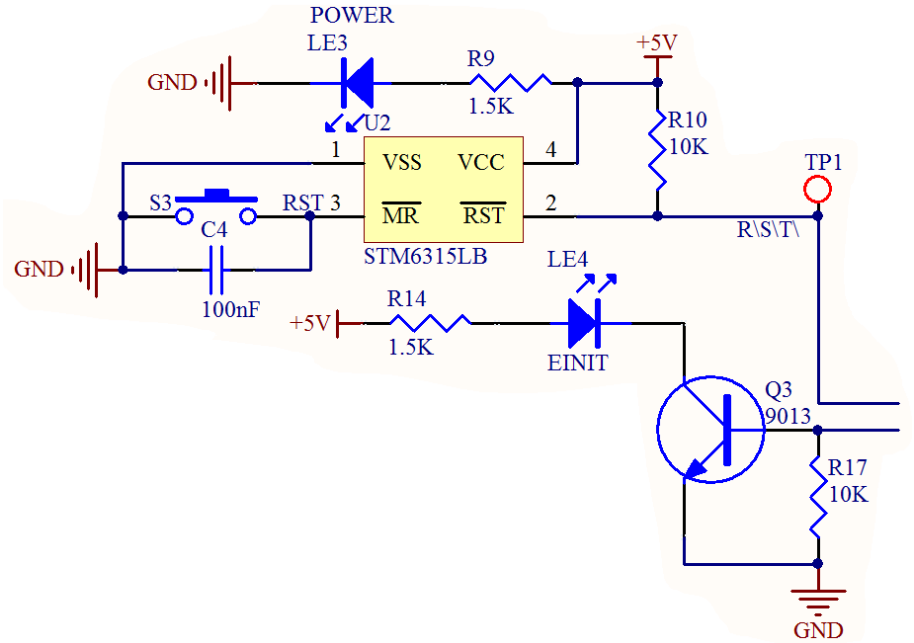



Figure 7. User LEDs - LE3/LE4 (schematic diagram)



## 2.4 JTAG/Nexus debug connection

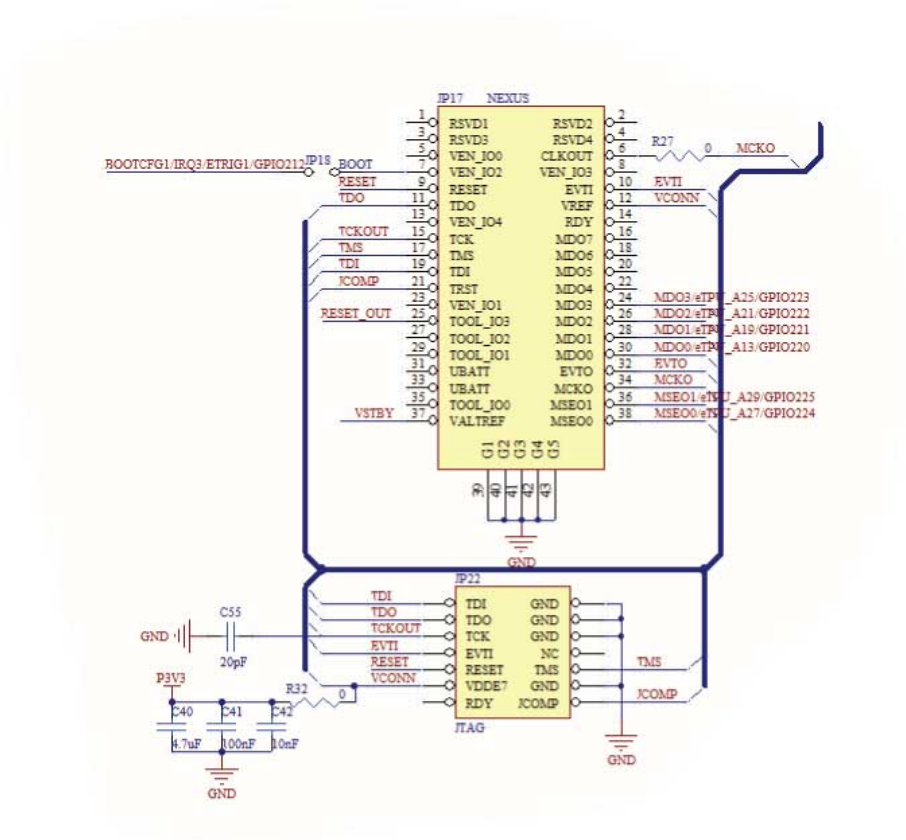
Two kinds of debug interfaces are used in the evaluation board:

- the standard 14-pin JTAG connector of PPC for low-cost/end tools;
- 3MTM Mictor 38-pin connector for Nexus interface in high-end development tools.

Prior to connect any development tool to the debug interface, it is highly recommended to switch off the power supply of the board and make sure the pin 1 of the tools' ribbon cable lines up with the pin 1 of onboard connector.

**Figure 8. JTAG/Nexus debug connection**

**Figure 9. JTAG/Nexus debug connection (schematic diagram)**



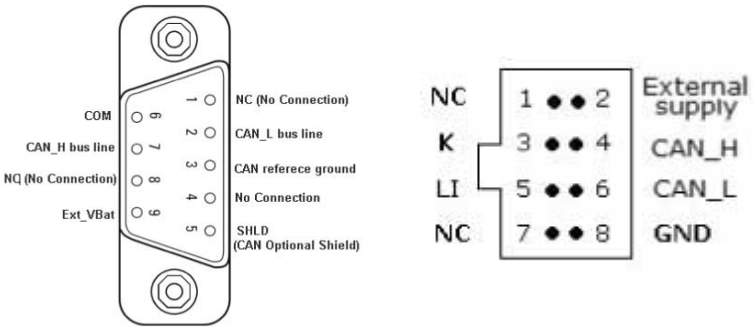
## 2.5 High speed CAN interface

The whole CAN interface circuit usually includes the CAN module in microcontroller, CAN transceiver and CAN connector.

In the evaluation board, CAN module is integrated with L9616 transceiver which supports high-speed CAN.

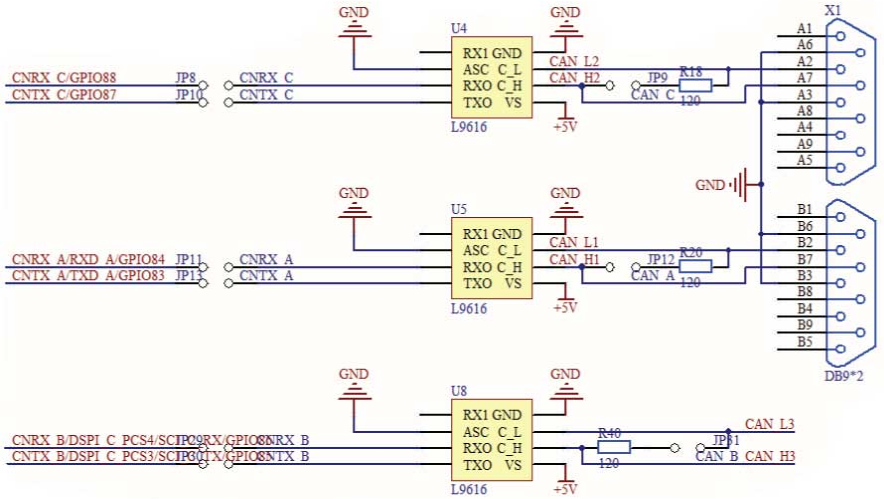
Regarding the CAN connectors, the two basic CAN channels of SPC564A70L7, CANA and CANC, are located in two DB9 male connectors.

**Figure 10. High speed CAN interface**




As the CAN TX/RX IO of microcontroller is multiplexed with other functions, several jumpers are placed between L9616 and the MCU. It avoids unwanted connections to L9616 if the CAN TX/RX has been configured to GPIO; detailed information is reported in the following figure.

**Figure 11. High speed CAN interface (schematic diagram)**




*Note: jumpers JP9, JP12 and JP31 are used to set proper 120 Ω termination resistor for CAN bus. Please disconnect the jumper if unnecessary.*

## 2.6 eSCI/K-LINE

eSCI stands for enhanced serial communication interface, as it enhances the conventional asynchronous RX/TX with DMA and LIN support. High speed CAN interface, HW configurations show the hardware connection on the evaluation board:

ST232 is the bridge between RS232 DB9 female interface and TX/RX signal of microcontroller.

L9637 is the ISO9141 interface chip. In the microcontroller side, user can set the jumper 20, 21, 23, 26 to choose two SCI interfaces, 1x SCI + 1x K-Line or 1x SCI/K-Line.

**Figure 12. High speed CAN interface (schematic diagram)**

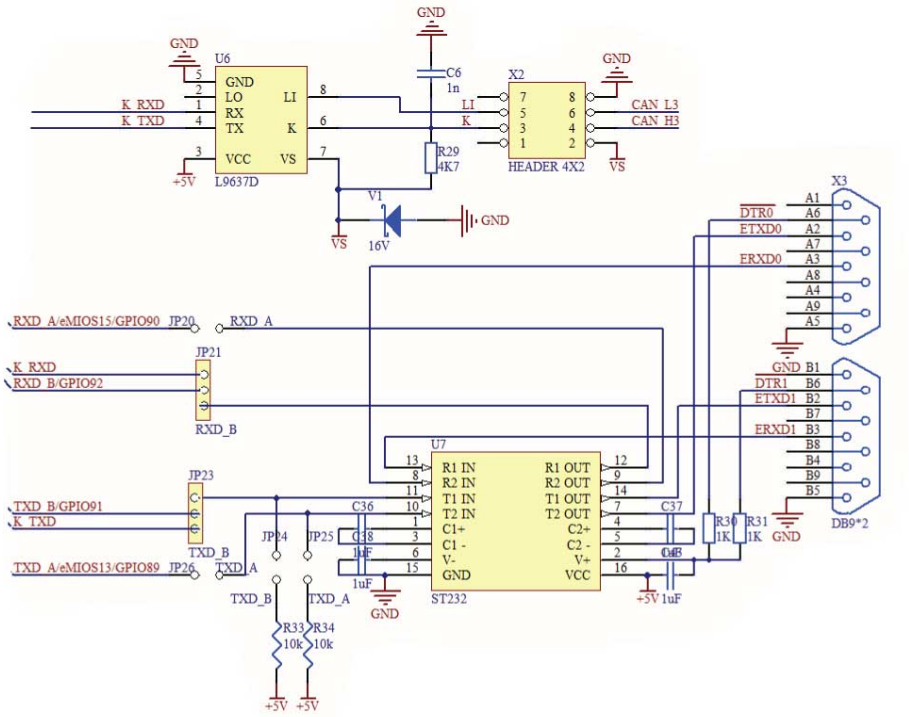



**Figure 13. High speed CAN interface, HW configurations**

| 2x SCI, SCIA, SCIB | SCIA + K-Line on T/RXD_B | SCIB + K-Line on T/RXD_A | SCIA | SCIB | K-Line on T/RXD_A | K-Line on T/RXD_B |
|---|---|---|---|---|---|---|
| | | | | | | |

## 2.7 I/O header

All GPIOs/DSPI/eMIOS/eTPU of the MCU can be accessed through the 4x36 I/O headers.

**Table 3. I/O header: pin out table**

| Pin number | A | B | C | D |
|---|---|---|---|---|
| 1 | GND | GND | GND | 5 V |
| 2 | AN10/ AN39/ANY | AN9/ANX | AN37 | AN36 |
| 3 | AN11/ANZ | AN16 | AN22 | AN24 |
| 4 | AN18 | PCS_B1/GPIO106 | AN27 | AN30 |
| 5 | PCS_B5/PCS_C0<br>GPIO110 | eTPU_A12/PCS_B1<br>GPIO126 | AN32 | AN34 |
| 6 | PCS_B0<br>GPIO105 | eTPU_A17<br>GPIO131 | AN17 | eTPU_A29<br>AN15/ FCK |
| 7 | eTPU_A10/eTPU_A22<br>GPIO124 | eTPU_A9/eTPU_A21<br>GPIO123 | MCKO<br>GPIO219 | MDO0/eTPU_A13<br>GPIO220 |
| 8 | eTPU_A11/eTPU_A23<br>GPIO125 | TDI18/eMIOS5<br>GPIO232 | MDO1/eTPU_A19<br>GPIO221 | MDO2/eTPU_A21<br>GPIO222 |
| 9 | eTPU_A16<br>GPIO130 | eTPU_A27_O | MDO3/eTPU_A25<br>GPIO223 | GPIO219 |
| 10 | eTPU_A18<br>GPIO132 | eTPU_A21<br>IRQ9<br>GPIO135 | GPIO206 | eTPU_A24/IRQ12<br>SCK_C_LVDS-<br>GPIO138 |
| 11 | eTPU_A19<br>GPIO133 | eTPU_A23/IRQ11<br>eTPU_A21<br>GPIO137 | TXD_A<br>eMIOS13<br>GPIO89 | RXD_A<br>eMIOS15<br>GPIO90 |
| 12 | RESET | eTPU_A13_O | RESET_OUT | PLLREF/IRQ4/ETRIG0<br>GPIO208 |
| 13 | GPIO207 | EVTI<br>eTPU_A2<br>GPIO231 | BOOTCFG1/IRQ3<br>ETRIG11<br>GPIO212 | VSTBY |
| 14 | GPIO99 | MSEO0/eTPU_A27<br>GPIO224 | WKPCFG/NMI<br>GPIO213 | eTPU_A29_O |
| 15 | eMIOS1/eTPU_A1<br>GPIO180 | PCS_B4/SCK_C<br>GPIO109 | CNRX_A/RXD_A<br>GPIO84 | eTPU_A2_O |
| 16 | PCS_B2/SOUT_C<br>GPIO107 | PCS_B3/SIN_C<br>GPIO108 | CNRX_C<br>GPIO88 | eTPU_A4_O |
| 17 | CNTX_A<br>TXD_A<br>GPIO83 | CNTX_C<br>GPIO87 | eMIOS8/eTPU_A8<br>TXDB<br>GPIO187 | MSEO1<br>eTPU_A29<br>GPIO225 |
| 18 | eMIOS14/IRQ0<br>eTPU_A29<br>GPIO193 | eTPU_A27<br>AN14<br>MA2/SDI | eMIOS9/eTPU_A9<br>RXDB<br>GPIO188 | eTPU_A28<br>PCS_C1<br>GPIO142 |

| Pin number | A | B | C | D |
|---|---|---|---|---|
| 19 | eTPU_A19<br>AN12<br>MA0/SDS | eMIOS13<br>GPIO192 | eTPU_A27/IRQ15<br>SOUT_C_LVDS+<br>SOUTB/ GPIO141 | eTPU_A26/IRQ14<br>SOUT_C_LVDS-<br>GPIO140 |
| 20 | eTPU_A29<br>PCS_C2<br>GPIO143 | eTPU_A21<br>AN13<br>MA1/SDO | GPIO98 | eTPU_A14/PCS_B4<br>eTPU_A9<br>GPIO128 |
| 21 | RXD_B<br>GPIO92 | TXD_B<br>GPIO91 | eMIOS11<br>GPIO190 | eTPU_A15/PCS_B5<br>GPIO129 |
| 22 | eMIOS4<br>eTPU_A4<br>GPIO183 | eMIOS12/DSPI_C_SOUT<br>eTPU_A27<br>GPIO191 | eMIOS15<br>IRQ1<br>GPIO194 | eTPU_A8/eTPU_A20<br>SOUT_B_LVDS+<br>GPIO122 |
| 23 | eMIOS2<br>eTPU_A2<br>GPIO181 | eMIOS23<br>GPIO202 | eTPU_A7/eTPU_A19<br>SOUT_B_LVDS-<br>eTPU_A6/GPIO121 | eTPU_A6/eTPU_A18<br>SCK_B_LVDS+<br>GPIO120 |
| 24 | eTPU_A20<br>IRQ8<br>GPIO134 | eTPU_A22/IRQ10<br>eTPU_A17<br>GPIO136 | eTPU_A5/eTPU_A17<br>SCK_B_LVDSGPIO119 | eTPU_A4<br>eTPU_A16<br>GPIO118 |
| 25 | eTPU_A30/PCS_C3<br>eTPU_A11<br>GPIO144 | eTPU_A25/IRQ13<br>SCK_C_LVDS+<br>GPIO139 | eTPU_A3<br>eTPU_A15<br>GPIO117 | SCK_B<br>PCS_C1<br>GPIO102 |
| 26 | AN21 | AN1/ DAN0- | SOUT_B/PSC_C5<br>GPIO104 | SIN_B/PCS_C2<br>GPIO103 |
| 27 | AN0/DAN0+ | AN3/DAN1- | eTPU_A0/eTPU_A12<br>eTPU_A19<br>GPIO114 | eMIOS0/eTPU_A0<br>eTPU_A25<br>GPIO179 |
| 28 | AN2/DAN1+ | AN5/DAN2- | eMIOS10<br>GPIO189 | eTPU_A1/eTPU_A13<br>GPIO115 |
| 29 | AN4/DAN2+ | AN7/DAN3- | eTPU_A31/PCS_C4<br>eTPU_A13<br>GPIO145 | eTPU_A2<br>eTPU_A14<br>GPIO116 |
| 30 | AN6/DAN3+ | AN25 | TDO/eMIOS6<br>GPIO228 | eTPU_A13/PCS_B3<br>GPIO127 |
| 31 | AN23 | AN31 | VRH | EVTO/eTPU_A4G<br>GPIO227 |
| 32 | AN28 | AN35 | GND | GND |
| 33 | AN33 | AN8/AN38/ANW | 5 V | 5 V |
| 34 | GND | GND | GND | 5 V |
| 35 | GND | eTPU_A19_O | eTPU_A21_O | eTPU_A25_O |
| 36 | GND | eMIOS3/eTPUA3_O<br>GPIO182 | eMIOS6/eTPUA6_O<br>GPIO185 | eMIOS7/eTPUA7_O<br>GPIO186 |

## 2.8 Jumper setting

Figure 14. Jumper setting

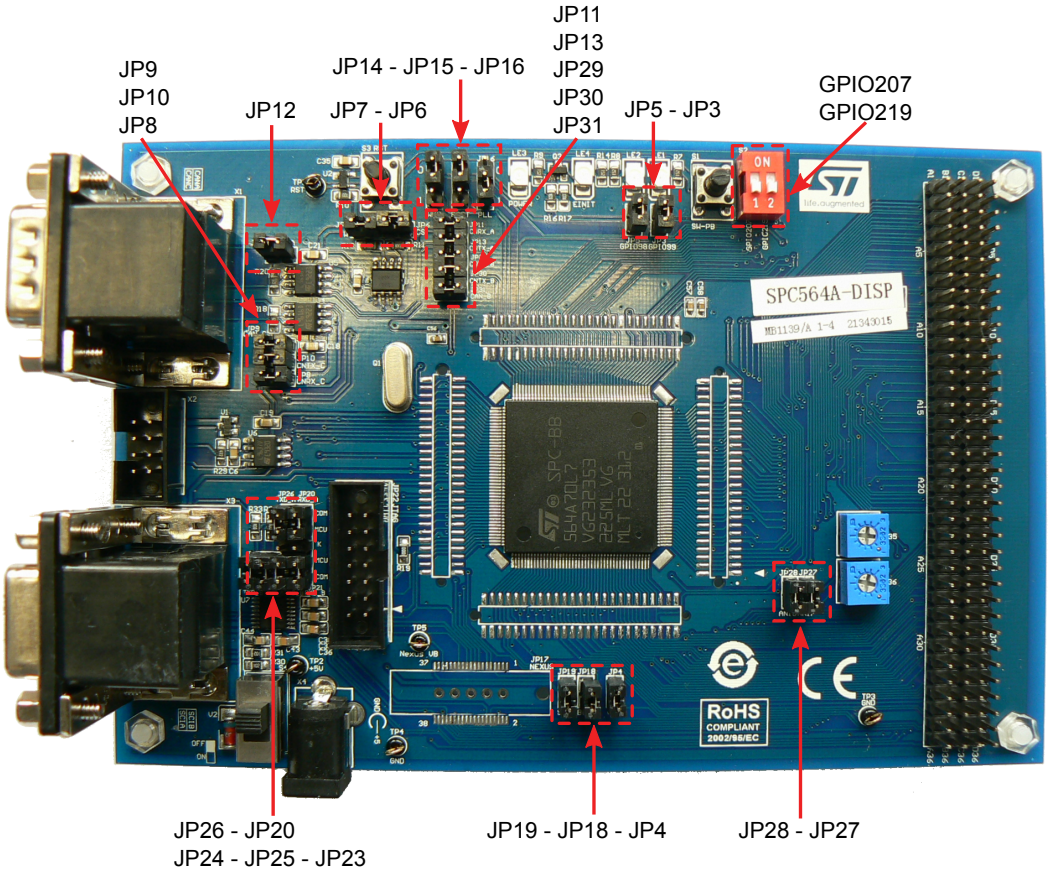



Table 4. Jumper setting: JP12, JP9, JP10, JP8

| JP12 | JP9 | JP10 | JP8 |
|---|---|---|---|
| R20, 120 Ω | R18, 120 Ω | TXO (U4 L9616) | RXO (U4 L9616) |
| CAN_H1 | CAN_H2 | CNTX_C | CNRX_C |

Table 5. Jumper setting: JP26, JP20, JP24, JP25, JP23, JP21

| JP26 | JP20 | JP24 | JP25 | JP23 | JP21 |
|---|---|---|---|---|---|
| T2IN (U7 ST232) | R2OUT (U7 ST232) | 5 V (10 kΩ to Vcc) | 5 V (10 kΩ to Vcc) | TXD_B GPIO91 | RXD_B GPIO92 |
| TXD_A GPIO89 | RXD_A GPIO90 | T1IN (U7 ST232) | T2IN (U7 ST232) | T1IN (U7 ST232) | R1OUT (U7 ST232) |

Table 6. Jumper setting: JP7, JP6

| JP7 | | JP6 | |
|---|---|---|---|
| 5 V | W (M95128) | CS (M95128) | GPIO128 |

**Table 7. Jumper setting: JP14, JP15, JP16**

| JP14 | JP15 | JP16 |
|---|---|---|
| GND<br>(10 kΩ to GND) | GND<br>(10 kΩ to GND) | GND<br>(10 kΩ to GND) |
| WKPCFG | BOOTCFG1 | PLLREF |
| 5 V<br>(10 kΩ to Vcc) | 5 V<br>(10 kΩ to Vcc) | 5 V<br>(10 kΩ to Vcc) |

**Table 8. Jumper setting: JP11, JP13, JP29, JP30, JP31**

| JP11 | JP13 | JP29 | JP30 | JP31 |
|---|---|---|---|---|
| RXO<br>(U5 L9616) | TXO<br>(U5 L9616) | RXO<br>(U8, L9616) | TXO<br>(U8, L9616) | R40, 120 Ω |
| CNRX_A | CNTX_A | CNRX_B | CNTX_B | CAN_L3 |
| RXD_A | TXD_A | RXD_B | RXD_B | - |

**Table 9. Jumper setting: JP5, JP3**

| JP5 | JP3 |
|---|---|
| LED2 | LED1 |
| GPIO98 | GPIO99 |

**Table 10. Jumper setting: GPIO207, GPIO219**

| GPIO207 | GPIO219 |
|---|---|
| ON (LOW) | ON (LOW) |
| OFF (HIGH) | OFF (HIGH) |

**Table 11. Jumper setting: JP28, JP27**

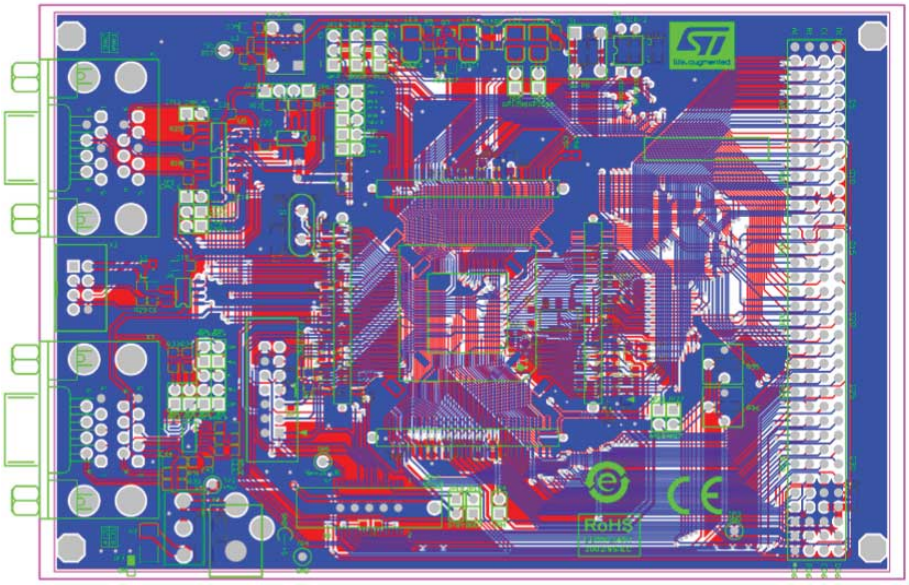
| JP28 | JP27 |
|---|---|
| AN18 | AN17 |
| Potentiometer, R36 | Potentiometer, R35 |

**Table 12. Jumper setting: JP19, JP18, JP4**

| JP19 | JP18 | JP4 |
|---|---|---|
| VSTBY<br>SRAM<br>Standby<br>voltage | VEN_IO2<br>(NEXUS) | VRH<br>Voltage<br>REF<br>high |
| 5 V | BOOTCFG1 | 5 VA |

# 3 PCB layout

Figure 15. PCB layout (top view)



# 4 General handling precautions

The following precautions are recommended when using the SPC564A-DISP, discovery board:

- Do not modify or manipulate the board when the external PSU supply is powered and connected to the board.
- Do not open and modify the PSU. Use AC plug adaptor if the main socket is not compatible with the PSU plug.
- Do not supply the board with a DC source higher than 5 V.
- Any equipment or tool used for any manipulation of the semiconductor devices or board modification should be shielded and connected to ground.
- The connectors and cables should be plugged and removed when the board is not supplied.
- It is recommended to use antistatic tools.

# Revision history

Table 13. **Document revision history**

| Date | Version | Changes |
|---|---|---|
| 02-Dec-2013 | 1 | Initial release. |
| 13-Jul-2015 | 2 | Changed value of DC source from 12 V to 5 V in Section 4 General handling precautions. |
| 30-Jul-2021 | 3 | Updated:<br>• Section 1.1 SPC564A-DISP Discovery board;<br>• Figure 2. HW overview;<br>• Figure 14. Jumper setting.<br>Minor text changes in:<br>• Section 2.1 5 VDC power supply;<br>• Section 2.5 High speed CAN interface. |

# Contents

**1 SPC564A-DISP with SPC564A70L7 . . . . . 2**

1.1 SPC564A-DISP Discovery board . . . . . 2

**2 Hardware overview . . . . . 3**

2.1 5 $V_{DC}$ power supply . . . . . 3

2.2 Device start-up configuration . . . . . 4

2.3 User LEDs . . . . . 4

2.4 JTAG/Nexus debug connection . . . . . 6

2.5 High speed CAN interface . . . . . 7

2.6 eSCI/K-LINE . . . . . 8

2.7 I/O header . . . . . 9

2.8 Jumper setting . . . . . 11

**3 PCB layout . . . . . 13**

**4 General handling precautions . . . . . 14**

**Revision history . . . . . 15**

# List of tables

Table 1. SPC564A-DISP – Device startup configuration . . . 4
Table 2. User LEDs . . . 4
Table 3. I/O header: pin out table . . . 9
Table 4. Jumper setting: JP12, JP9, JP10, JP8 . . . 11
Table 5. Jumper setting: JP26, JP20, JP24, JP25, JP23, JP21 . . . 11
Table 6. Jumper setting: JP7, JP6 . . . 11
Table 7. Jumper setting: JP14, JP15, JP16 . . . 12
Table 8. Jumper setting: JP11, JP13, JP29, JP30, JP31 . . . 12
Table 9. Jumper setting: JP5, JP3 . . . 12
Table 10. Jumper setting: GPIO207, GPIO219 . . . 12
Table 11. Jumper setting: JP28, JP27 . . . 12
Table 12. Jumper setting: JP19, JP18, JP4 . . . 12
Table 13. Document revision history . . . 15

# List of figures

Figure 1. SPC564A-DISP Discovery board . . . 2
Figure 2. HW overview . . . 3
Figure 3. PSU Section (+5.0 $V_{DC}$). . . . 3
Figure 4. Device start-up configuration . . . 4
Figure 5. User LEDs . . . 4
Figure 6. User LEDs - LE1/LE2 (schematic diagram). . . . 5
Figure 7. User LEDs - LE3/LE4 (schematic diagram). . . . 5
Figure 8. JTAG/Nexus debug connection. . . . 6
Figure 9. JTAG/Nexus debug connection (schematic diagram) . . . 6
Figure 10. High speed CAN interface . . . 7
Figure 11. High speed CAN interface (schematic diagram) . . . 7
Figure 12. High speed CAN interface (schematic diagram) . . . 8
Figure 13. High speed CAN interface, HW configurations . . . 8
Figure 14. Jumper setting . . . 11
Figure 15. PCB layout (top view) . . . 13

**IMPORTANT NOTICE – PLEASE READ CAREFULLY**

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, please refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2021 STMicroelectronics – All rights reserved