1000 W motor control power board based on STGIF10CH60TS-L SLLIMM™ 2nd series IPM

Introduction

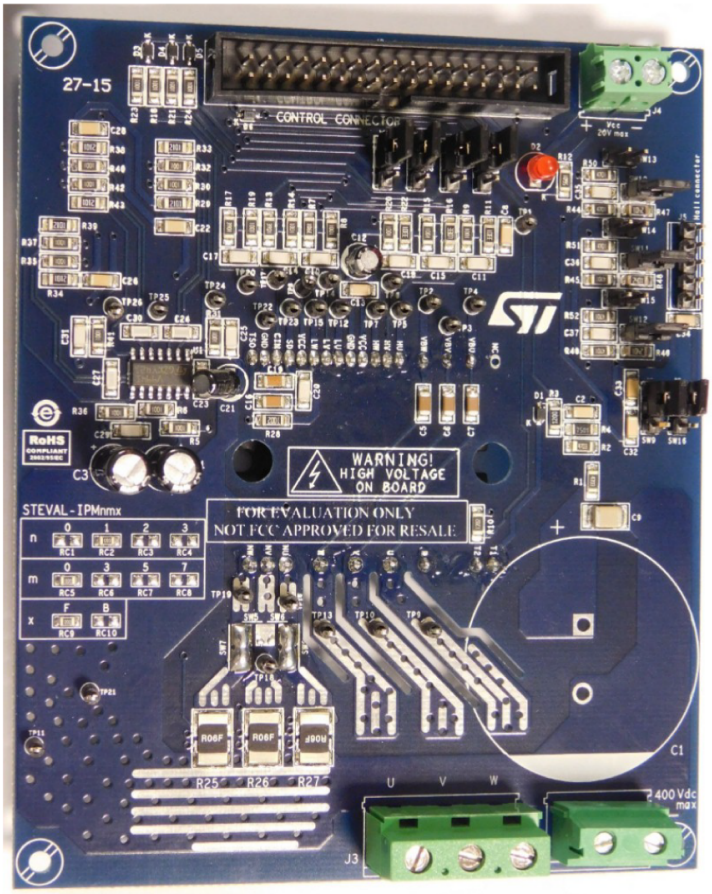
The STEVAL-IPM10F is a compact motor drive power board based on SLLIMM™ (small low-loss intelligent molded module) 2nd series (STGIF10CH60TS-L). It provides an affordable and easy-to-use solution for driving high power motors for a wide range of applications such as power white goods, air conditioning, compressors, power fans, high-end power tools and 3-phase inverters for motor drives in general. The IPM itself consists of short-circuit rugged IGBTs and a wide range of features like undervoltage lockout, smart shutdown, embedded temperature sensor and NTC, and overcurrent protection.

The main characteristics of this evaluation board are small size, minimal BOM and high efficiency. It consists of an interface circuit (BUS and V_{CC} connectors), bootstrap capacitors, snubber capacitor, hardware short-circuit protection, fault event and temperature monitoring. In order to increase the flexibility, it is designed to work in single- or three-shunt configuration and with double current sensing options such as using three dedicated onboard op-amps, or op-amps embedded in the MCU. The Hall/Encoder part completes the circuit.

Thanks to these advanced characteristics, the system has been specifically designed to achieve fast and accurate current feedback conditioning, satisfying the typical requirements for field-oriented control (FOC).

The STEVAL-IPM10F is compatible with ST's STM32-based control board, enabling designers to build a complete platform for motor control.

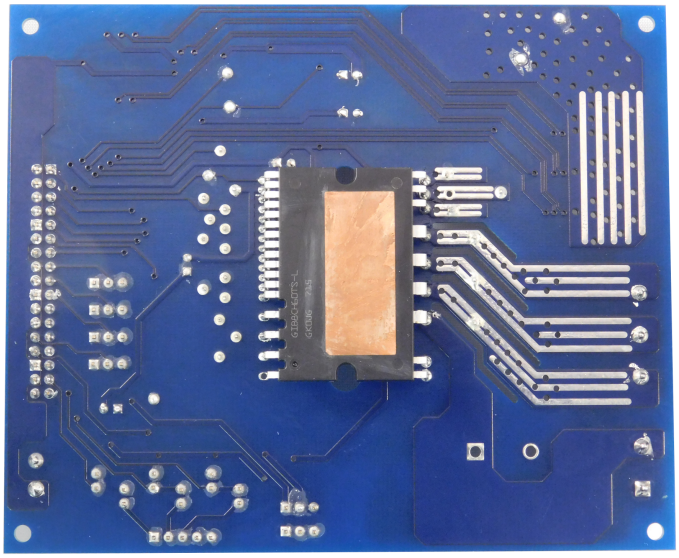
Figure 1. SLLIMM 2nd series motor control internal demo board (top view)



1 Key features

- Input voltage: 125 - 400 VDC
- Nominal power: up to 700 W
- Nominal current: up to 6 A
- Input auxiliary voltage: up to 20 V DC
- Motor control connector (32 pins) interfacing with ST MCU boards
- Single- or three-shunt resistors for current sensing (with sensing network)
- Two options for current sensing: dedicated op-amps or through MCU
- Overcurrent hardware protection
- IPM temperature monitoring and protection
- Hall sensors (3.3 / 5 V)/encoder inputs (3.3 / 5 V)
- IGBT intelligent power module:
  - SLLIMM™ 2nd series IPM (STGIF10CH60TS-L - Full molded package)
- Universal conception for further evaluation with bread board and testing pins
- Very compact size

Figure 2. SLLIMM 2nd series motor control internal demo board: (bottom view)



2 Circuit schematic

Following figures show the whole schematic of the SLLIMM™ 2nd series card for STGIF10CH60TS-L IPM products. This card consists of an interface circuit (BUS and V_{CC} connectors), bootstrap capacitors, snubber capacitor, short-circuit protection, fault output circuit, temperature monitoring, single-/three-shunt resistors and filters for input signals. It also includes bypass capacitors for V_{CC} and bootstrap capacitors. The capacitors are located very close to the drive IC, which is very helpful in preventing malfunction due to noise.

Two current sensing options are provided: three dedicated onboard op-amps or using opamps embedded on the MCU. Selection is performed through three jumpers.

The Hall/Encoder part (powered at 5 V or 3.3 V) completes the circuit.

2.1 Schematic diagrams

Figure 3. STEVAL-IPM10F circuit schematic (1 of 6)

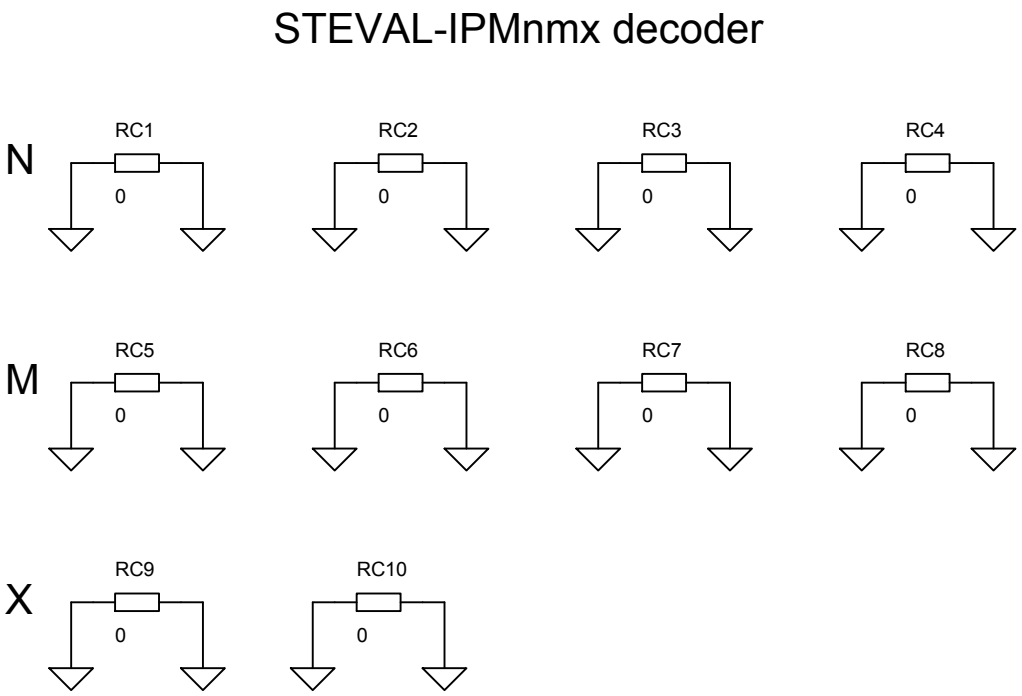


Figure 4. **STEVAL-IPM10F circuit schematic (2 of 6)**

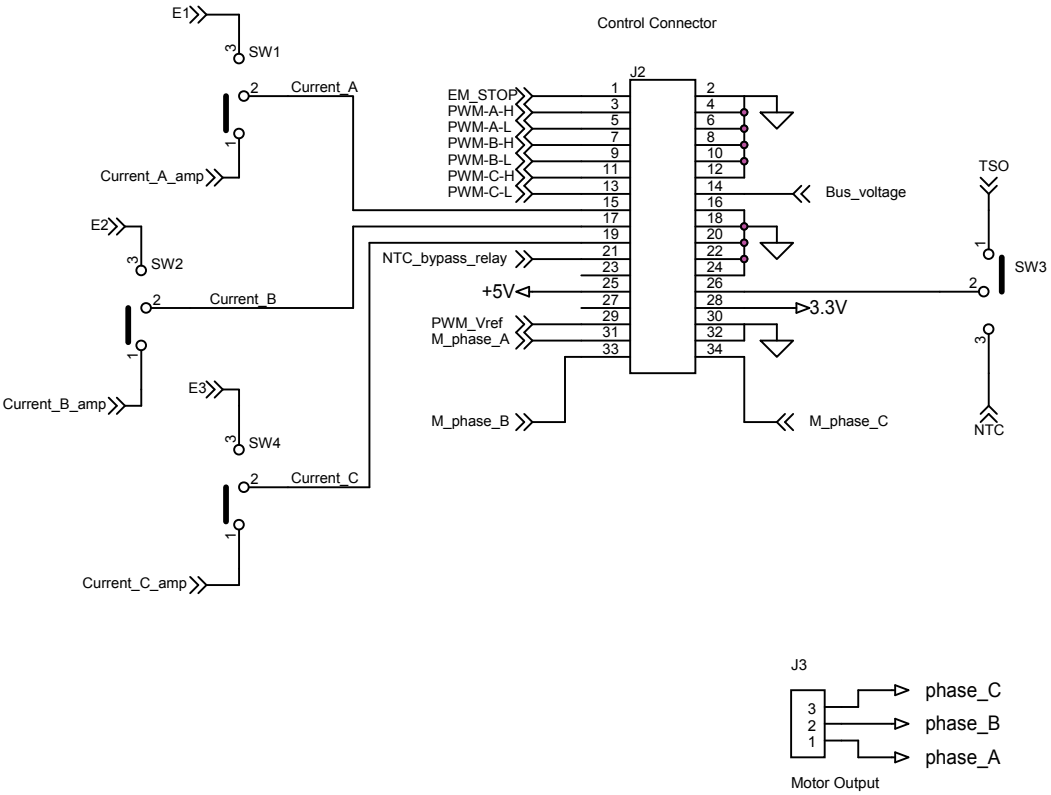


Figure 5. STEVAL-IPM10F circuit schematic (3 of 6)

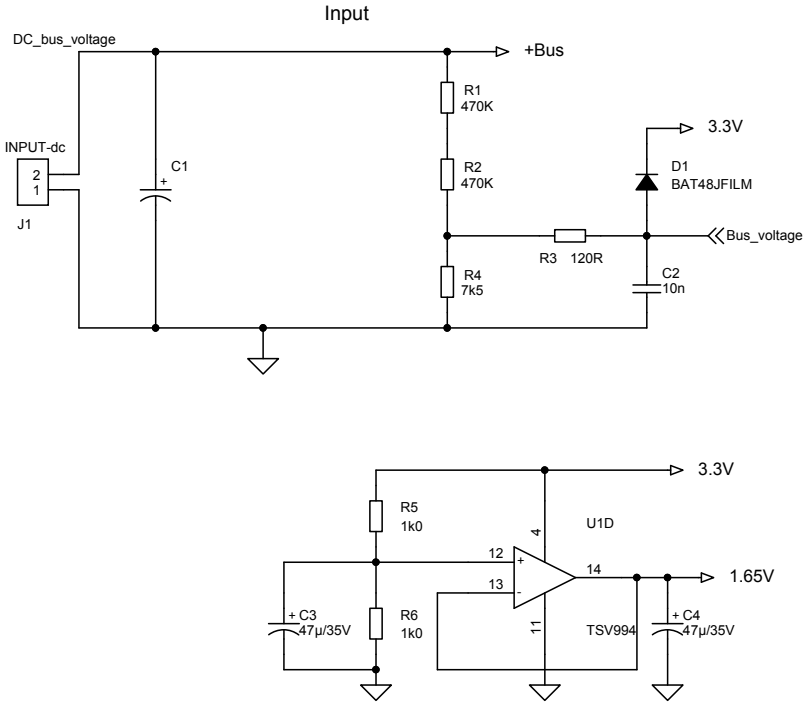


Figure 6. **STEVAL-IPM10F circuit schematic (4 of 6)**

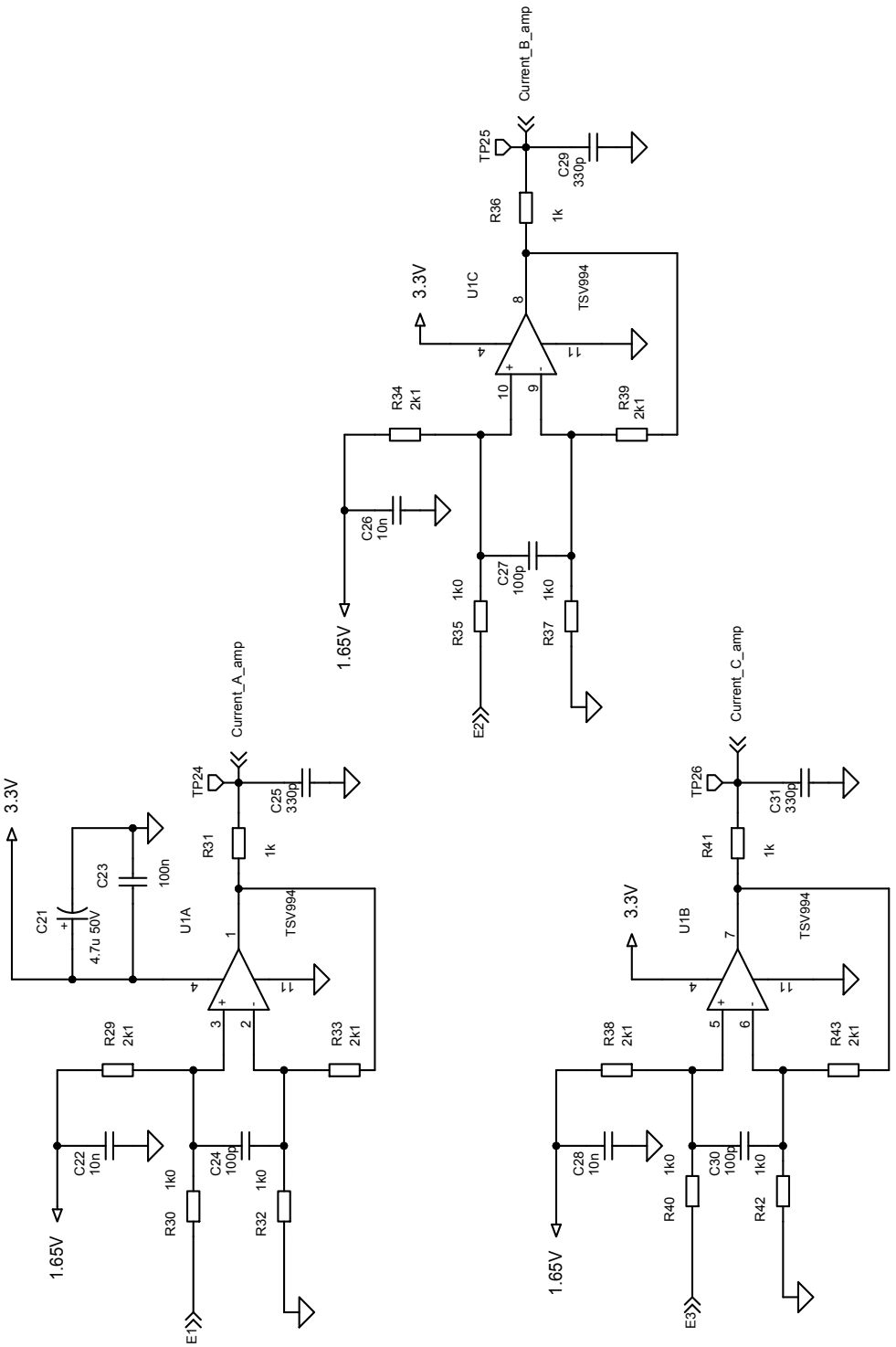


Figure 7. **STEVAL-IPM10F circuit schematic (5 of 6)**

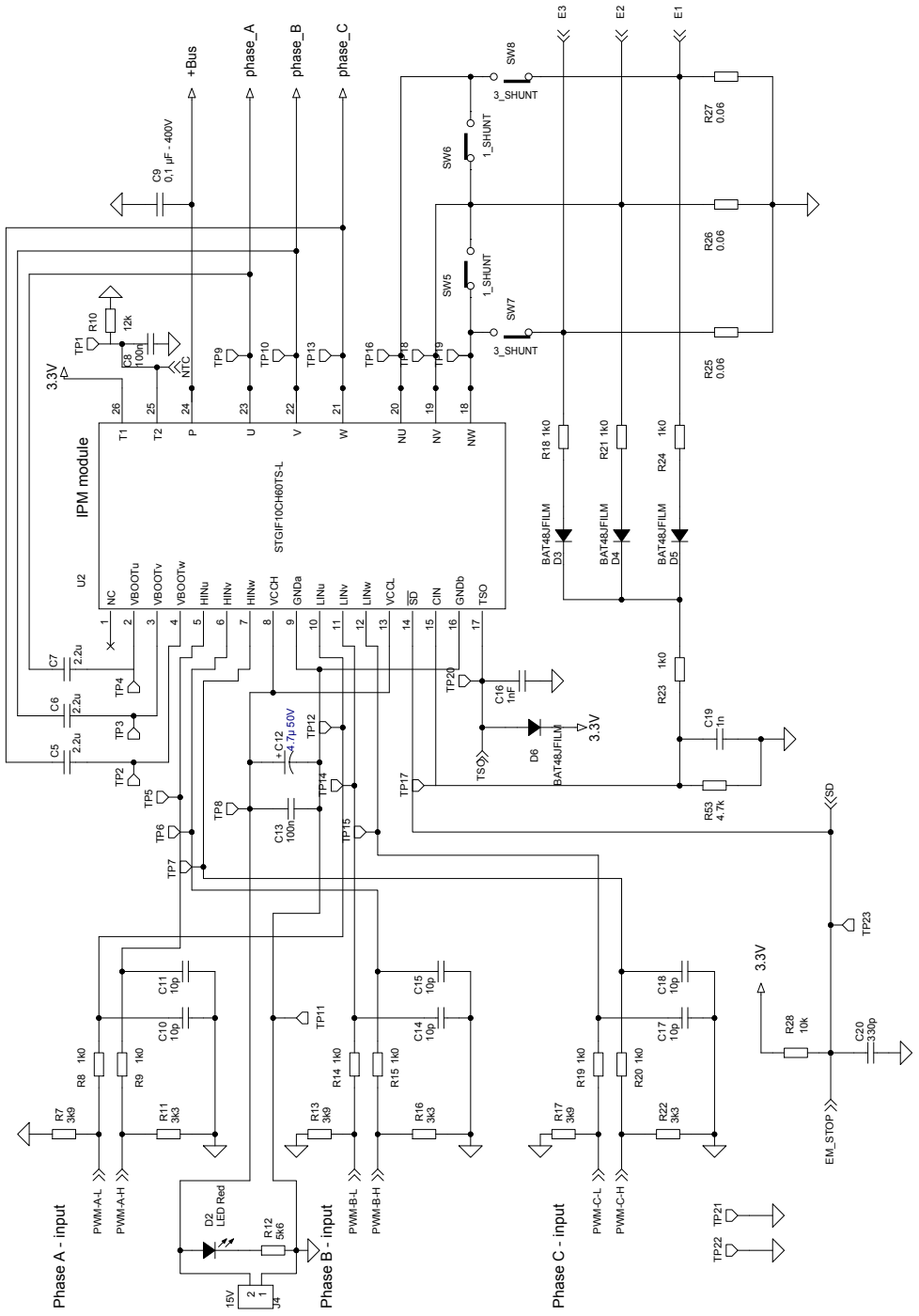
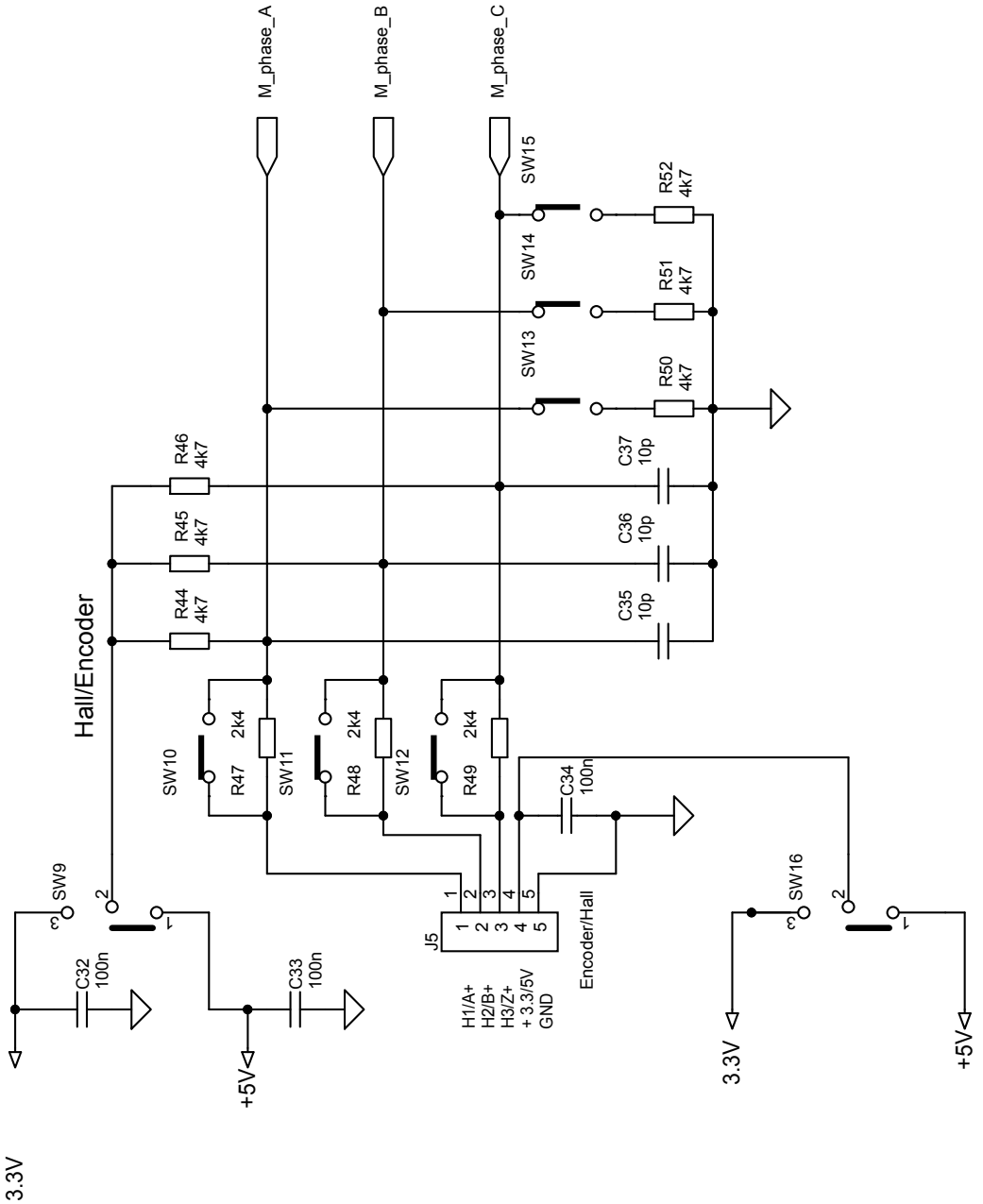


Figure 8. **STEVAL-IPM10F circuit schematic (6 of 6)**



3 Main characteristics

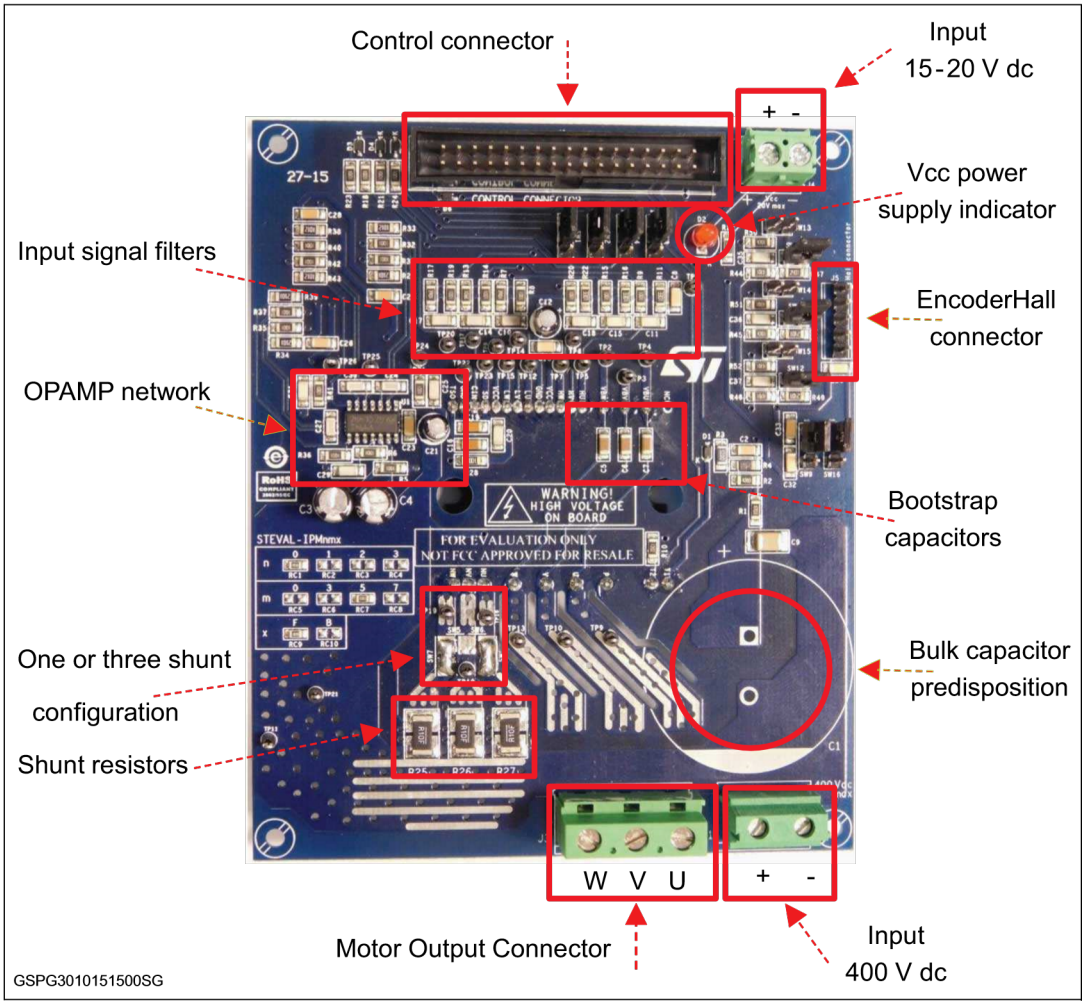
The board is designed to be compatible with DC supply from 125 VDC up to 400 VDC voltage.

A bulk capacitor according to the power level of the application must be mounted. The footprint is already provided on the board.

The SLLIMM integrates six IGBT switches with freewheeling diodes together with high voltage gate drivers. Thanks to this integrated module, the system is specifically designed to achieve power inversion in a reliable and compact design. Such integration reduces the required PCB area and the simplicity of the design increases reliability.

In order to increase the flexibility, it can operate in single- or three-shunt configuration by modifying solder bridge jumper settings (see Section 4.3.5 Single- or three-shunt selection).

Figure 9. STEVAL-IPM05F architecture



4 Filters and key parameters

4.1 Input signals

The input signals (LINx and HINx), able to drive the internal IGBTs, are active high. A 100 kΩ (typ.) pull-down resistor is built-in for each input signal. In order to prevent input signal oscillation, an RC filter was added on each input and placed as close as possible to the IPM. The filter is designed using a time constant of 10 ns (1 kΩ and 10 pF).

4.2 Bootstrap capacitor

In the 3-phase inverter, the emitters of the low side IGBTs are connected to the negative DC bus (V_{DC-}) as common reference ground, which allows all low side gate drivers to share the same power supply, while the emitter of high side IGBTs is alternately connected to the positive (V_{DC+}) and negative (V_{DC-}) DC bus during running conditions.

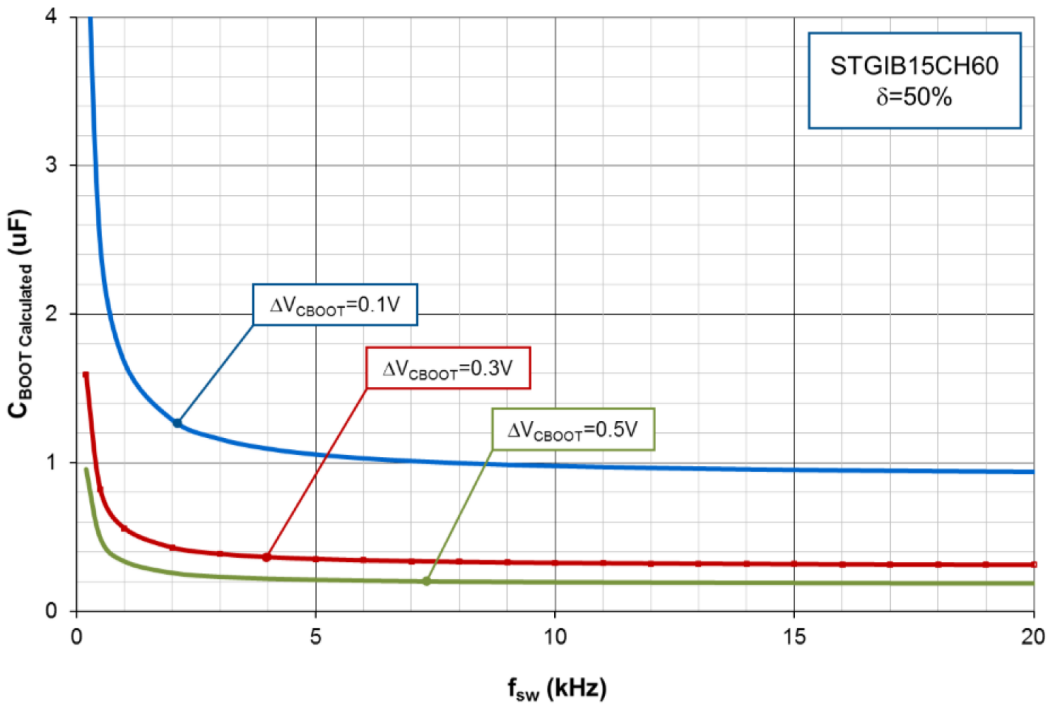
A bootstrap method is a simple and cheap solution to supply the high voltage section. This function is normally accomplished by a high voltage fast recovery diode. The SLLIMM 2nd series family includes a patented integrated structure that replaces the external diode. It is realized with a high voltage DMOS functioning as diode with series resistor. An internal charge pump provides the DMOS driving voltage. The value of the C_{BOOT} capacitor should be calculated according to the application condition.

Note: This curve is taken from application note AN4768 (available on www.st.com); calculations are based on the STGIB15CH60 device, which represents the worst case scenario for this kind of calculation.

Figure 10. C_{BOOT} graph selection shows the behavior of C_{BOOT} (calculated) versus switching frequency (f_{sw}), with different values of ΔV_{CBOOT} for a continuous sinusoidal modulation and a duty cycle δ = 50%.

The boot capacitor must be two or three times larger than the C_{BOOT} calculated in the graph. For this design, a value of 2.2 µF was selected.

Figure 10. C_{BOOT} graph selection



4.3 Overcurrent protection

The SLLIMM 2nd series integrates a comparator for fault sensing purposes. The comparator has an internal voltage reference V_{REF} (510 mV typ.) connected to the inverting input, while the non-inverting input available on the CIN pin can be connected to an external shunt resistor to implement the overcurrent protection function. When the comparator triggers, the device enters the shutdown state.

The comparator output is connected to the SD pin in order to send the fault message to the MCU.

4.3.1 SD Pin

The $\overline{SD}$ is an input/output pin (open drain type if used as output). Taking into account the voltage reference on $\overline{SD}$ (3.3 V), a pull up resistor of 10 kΩ (R28) is used to guarantee the right bias and consequently to keep the current on the open drain DMOS (I_{od}) lower than 3 mA.

The filter on $\overline{SD}$ (R28 and C20) has to be sized to obtain the desired re-starting time after a fault event and placed as close as possible to the $\overline{SD}$ pin.

A shutdown event can be managed by the MCU, in this case the $\overline{SD}$ functions as the input pin.

Conversely, the $\overline{SD}$ functions as an output pin when an overcurrent or undervoltage condition is detected.

4.3.2 Fault management

The SLLIMM 2nd series integrates a specific kind of fault management, useful when SD is functioning as output, able to identify the type of fault event.

As previously described, as soon as a fault occurs, the open-drain (DMOS) is activated and LVGx outputs are forced low.

Two types of fault can be signaled:

- Overcurrent (OC) sensed by the internal comparator (CIN);
- Undervoltage (UVLO) on supply voltage (VCC).

Each fault enables the SD open drain for a different time (see the table below).

The duration of a shutdown event therefore tells us the type of failure that has occurred.

Table 1. Fault timing

Symbol	Parameter	Event time	SD open-drain enable time result
OC	Over current event	≤ 24 µs	24 µs
		> 24 µs	OC time
UVLO	Undervoltage lockout event	≤ 70 µs	70 µs
		> 70 µs until VCC_LS exceeds the VCC_LS UV turn on threshold	UVLO time

1. *typical value (T_J = -40 °C to 125 °C)*
2. *without contribution of RC network on SD*

Figure 11. SD failure due to overcurrent shows a shutdown as the result of an overcurrent event. During the overcurrent, the voltage on the comparator (CIN) exceeds the threshold (0.51 V typ.) and the shutdown is able to stop the application. In this case, the SD event time is about 24 µs (for OC event less than 24 µs).

Figure 11. **SD failure due to overcurrent**

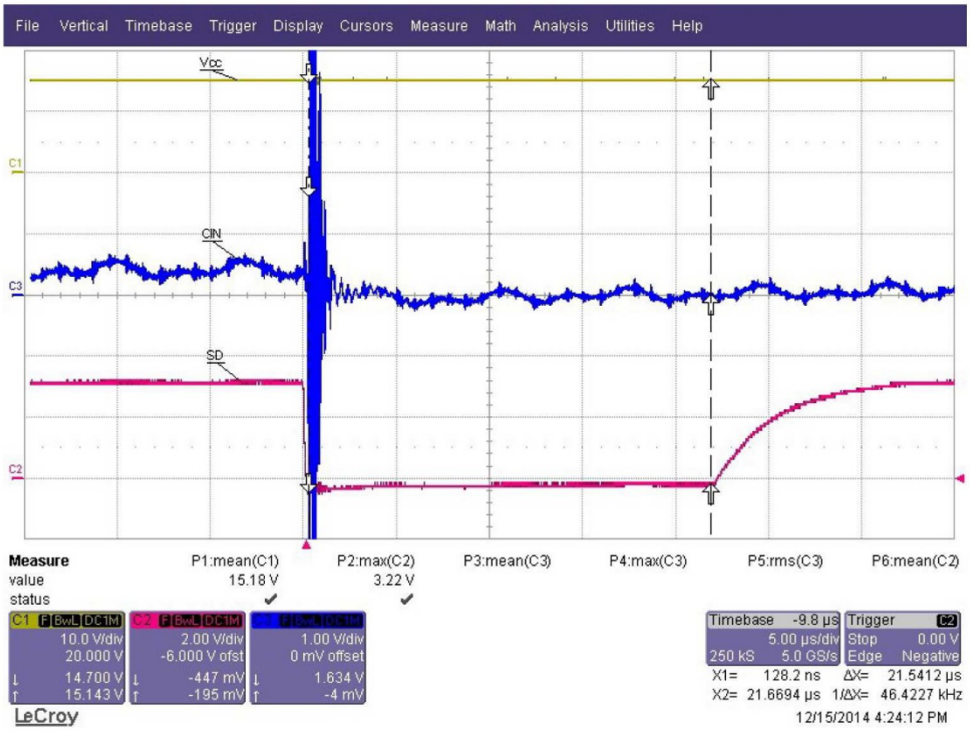


Figure 12. SD failure due to undervoltage (UVLO below 70 µs) shows the shutdown event as the result of an undervoltage condition on the V_{CC} supply. If V_{CC} drops below the undervoltage threshold, the shutdown can stop the application. If the voltage on V_{CC} rises above the V_{CC} on threshold in less than 70 µs, the SD event time is about 70 µs.

Figure 12. **SD failure due to undervoltage (UVLO below 70 µs)**

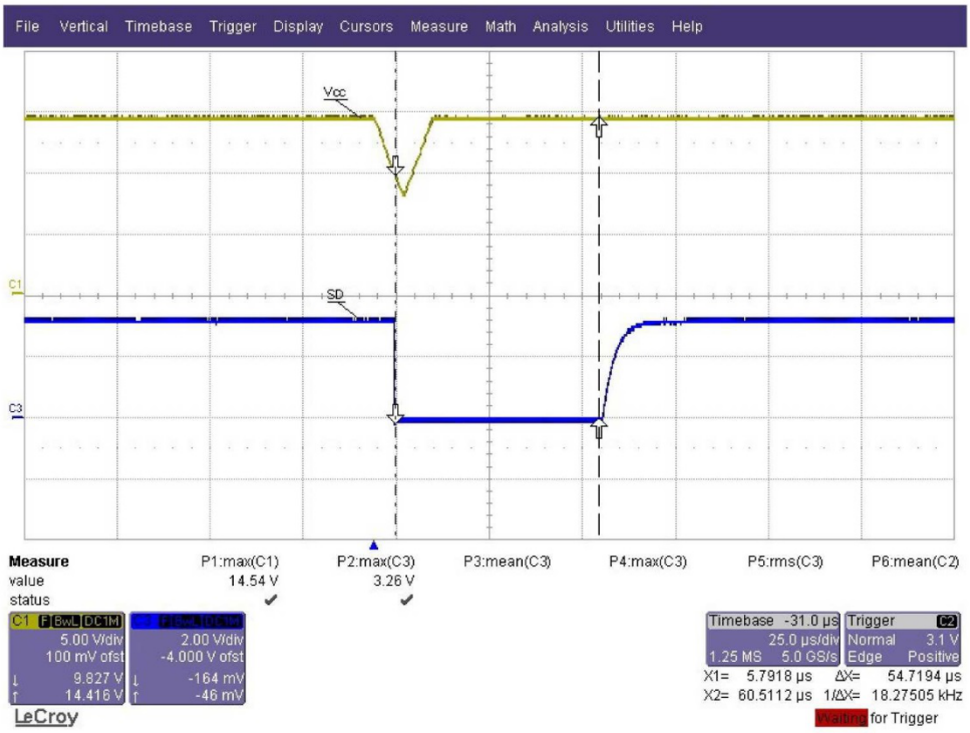
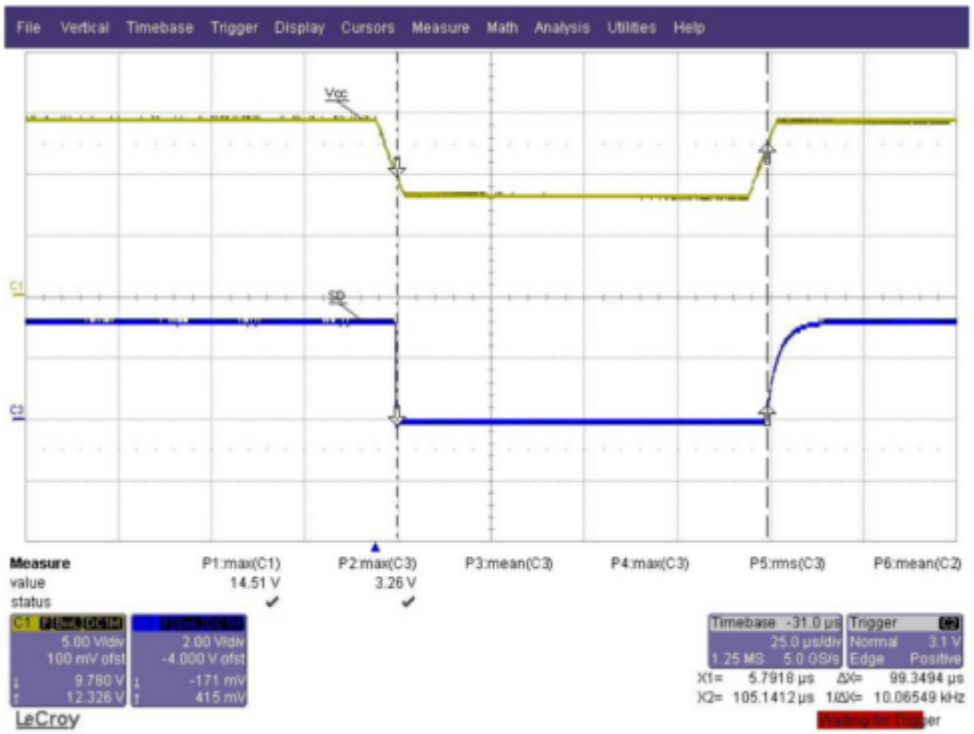


Figure 13. SD failure due to undervoltage (UVLO above 70 µs) shows the shutdown event as the result of an undervoltage condition on the V_{CC} supply. In this case, the drop on V_{CC} is greater than 70 µs. The SD event time is the same as the duration of drop.

Figure 13. **SD failure due to undervoltage (UVLO above 70 µs)**



4.3.3 Shunt resistor selection

The value of the shunt resistor is calculated by the following equation:

$$R_{SH} = \frac{V_{ref}}{I_{OC}} \quad (1)$$

Where V_{ref} is the internal comparator (CIN) (0.51 V typ.) and I_{OC} is the overcurrent threshold detection level.

The maximum OC protection level should be set to less than the pulsed collector current in the datasheet. In this design, the overcurrent threshold level is fixed at I_{OC} = 13 A in order to select a commercial shunt resistor value.

$$R_{SH} = \frac{V_{ref} \cdot \left(\frac{R23 + R53}{R53}\right) + V_F}{I_{OC}} = \frac{0.51 \cdot \left(\frac{1000 + 4700}{4700}\right) + 0.18}{13} = 0.061\Omega \quad (2)$$

Where V_F is the voltage drop across diodes D6, D7 and D8.

For the power rating of the shunt resistor, the following parameters must be considered:

- Maximum load current of inverter (85% of $I_{nom\ [Arms]}$): $I_{load(max)}$
- Shunt resistor value at TC = 25 °C
- Power derating ratio of shunt resistor at T_{SH} =100 °C
- Safety margin

The power rating is calculated by the following equation:

$$P_{SH} = \frac{1}{2} \cdot \frac{I^2_{load(\max)} \cdot R_{SH} \cdot margin}{Derating\ gratio} \quad (3)$$

The commercial value chosen was 0.06 Ω to which corresponds an overcurrent level of 13.3 A.

The power rating is:

- $$I_{nom} = 7A \rightarrow I_{nom[rms]} = \frac{I_{nom}}{\sqrt{2}} \rightarrow I_{load(\max)} = 85\,\% \left(I_{nom[rms]}\right) = 6\,A_{rms} \quad (4)$$
- Power derating ratio of shunt resistor at TSH = 100 °C: 80% (from datasheetmanufacturer)
- Safety margin: 30%

$$P_{SH} = \frac{1}{2} \cdot \frac{6.0^2 \cdot 0.06 \cdot 1.3}{0.8} = 1.75\,W \quad (5)$$

Considering the commercial value, a 1 W shunt resistor was selected.

Based on the previous equations and conditions, the minimum shunt resistance and power rating is summarized below.

Table 2. Shunt selection

Device	$I_{nom(peak)}$ [A]	$OCP_{(peak)}$ [A]	$I_{load(max)}$ [Arms]	R_{SHUNT} [Ω]	Minimum shunt power rating P_{SH} [W]
STGIB10CH60TS-L	10	13.3	6.0	0.06	1.75

4.3.4 RC filter

An RC filter network is required to prevent undesired short circuit operation due to the noise on the shunt resistor. In this design, the RC filter, composed of R23, R18, R21, R24 and C19, has a constant time of about 1.3 µs. Adding the turn-off propagation delay of the gate driver and the IGBT turn-off time (hundreds of nanoseconds in total), the total delay time is less than 5 µs of short circuit withstand IGBT time.

4.3.5 Single- or three-shunt selection

Single- or three-shunt resistor circuits can be adopted by setting the solder bridges SW5, SW6, SW7 and SW8.

The figures below illustrate how to set up the two configurations.

Figure 14. One-shunt configuration

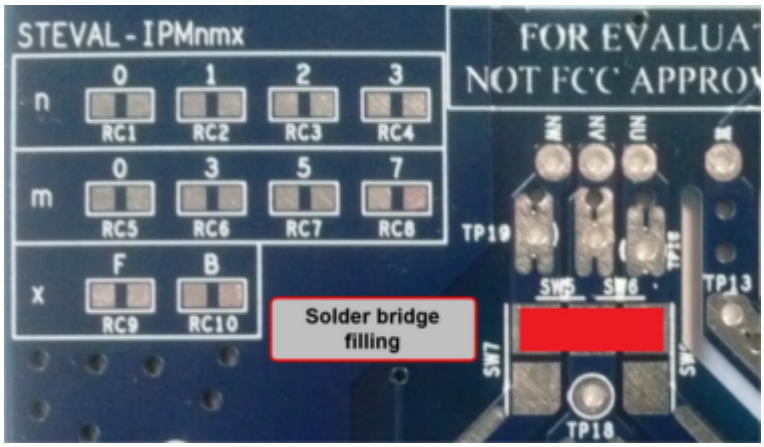
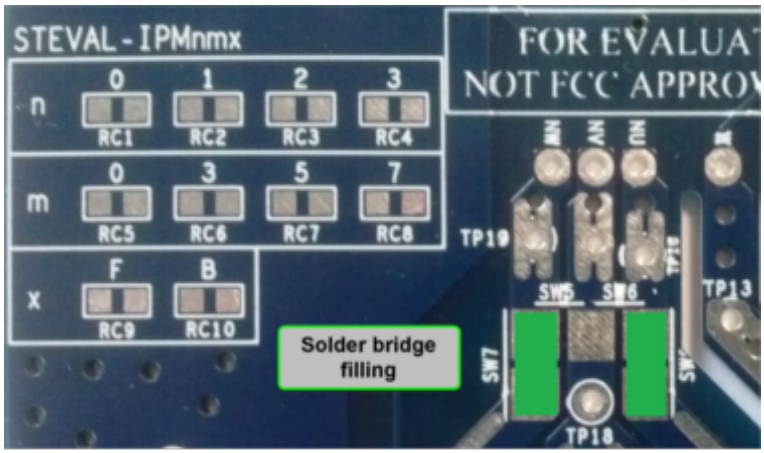


Figure 15. Three-shunt configuration



5 Current sensing amplifying network

The motor control demonstration board can be configured to run in three-shunt or single-shunt configurations for field oriented control (FOC).

The current can be sensed thanks to the shunt resistor and amplified by using the on board operational amplifiers or by the MCU (if equipped with op-amp).

Once the shunt configuration is chosen by setting solder bridge on SW5, SW6, SW7 and SW8 (as described in Section 4.3.5 Single- or three-shunt selection), the user can choose to send the voltage shunt to the MCU amplified or unamplified.

Single-shunt configuration requires a single op amp and three-shunt configuration requires three op amps; therefore, in single-shunt configuration, the only voltage which is sent to the MCU to control the sensing is connected to phase V through SW2.

SW1, SW2, SW4 can select which signals are sent to micro, as described below:

Table 3. Op-amp sensing configuration

Symbol	Configuration	Bridge	Sensing
SW1	Single Shunt	1-2	open
		2-3	open
	Three Shunt	1-2	On-board op-amp
		2-3	MCU op-amp
SW2	Single Shunt	1-2	On board op-amp
		2-3	MCU op-amp
	Three Shunt	1-2	On-board op-amp
		2-3	MCU op-amp
SW4	Single Shunt	1-2	open
		2-3	open
	Three Shunt	1-2	On-board op-amp
		2-3	MCU op-amp

The operational amplifier TSV994 used on amplifying networks has a 20 MHz gain bandwidth and operates with a single positive supply of 3.3 V.

The amplification network must allow bidirectional current sensing, so that an output offset V_O = +1.65 V represents zero current.

Referencing the STGIF10CH60TS-L (I_{OCP} = 10 A; R_{SHUNT} = 0.06 Ω), the maximum measurable phase current, considering that the output swings from +1.65 V to +3.3 V (MCU supply voltage) for positive currents and from +1.65 V to 0 for negative currents is:

Equation 5

$$MaxMeasCurrent = \frac{\Delta V}{r_m} = 13.3\ A \quad (6)$$

$$r_m = \frac{\Delta V}{MaxMeasCurrent} = \frac{1.65}{13.3} = 0.124\ \Omega \quad (7)$$

The overall trans-resistance of the two-port network is:

$$r_m = R_{SHUNT} \cdot AMP = 0.06 \cdot AMP = 0.124\ \Omega \quad (8)$$

$$AMP = \frac{r_m}{R_{SHUNT}} = \frac{0.124}{0.06} = 2.1 \quad (9)$$

Finally choosing R_a=R_b and R_c=R_d, the differential gain of the circuit is:

$$AMP = \frac{R_c}{R_a} = 2.1 \quad (10)$$

An amplification gain of 2.1 was chosen. The same amplification is obtained for all the other devices, taking into account the OCP current and the shunt resistance, as described in Table 1.

The RC filter for output amplification is designed to have a time constant that matches noise parameters in the range of 1.5 µs:

$$4 \cdot \tau = 4 \cdot R_e \cdot C_c = 1.5\ \mu s \quad (11)$$

$$C_c = \frac{1.5\ \mu s}{4 \cdot 1000} = 375\ pF\ \left(330\ pF\ selected\right) \quad (12)$$

Table 4. Amplifying networks

Phase		Amplifying network			RC filter	
	Ra	Rb	Rc	Rd	Re	Cc
Phase U	R30	R32	R29	R33	R31	C25
Phase V	R35	R37	R34	R39	R36	C29
Phase W	R40	R42	R38	R43	R41	C31

6 Temperature monitoring

The SLLIMM 2nd series family integrates a temperature sensor (VTSO) on the low side gate driver and an NTC thermistor placed close to the power stage.

They can be selected via SW3.

The board is designed to use both of them to monitor the internal IPM temperature through the MCU.

6.1 Thermal sensor (VTSO)

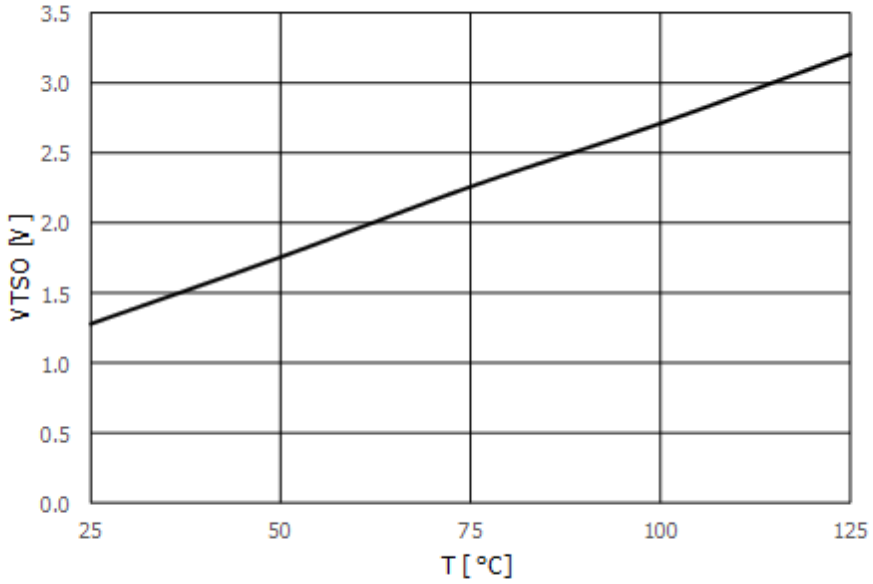
A voltage proportional to the temperature is available on the TSO pin (17) and easily measurable on the TP20 test pin.

To improve noise immunity, a 1 nF (C16) capacitor filter is placed on this pin.

The thermal sensor does not need any pull down resistors.

The following graph shows typical voltage variation as a function of temperature.

Figure 16. Thermal sensor voltage vs temperature



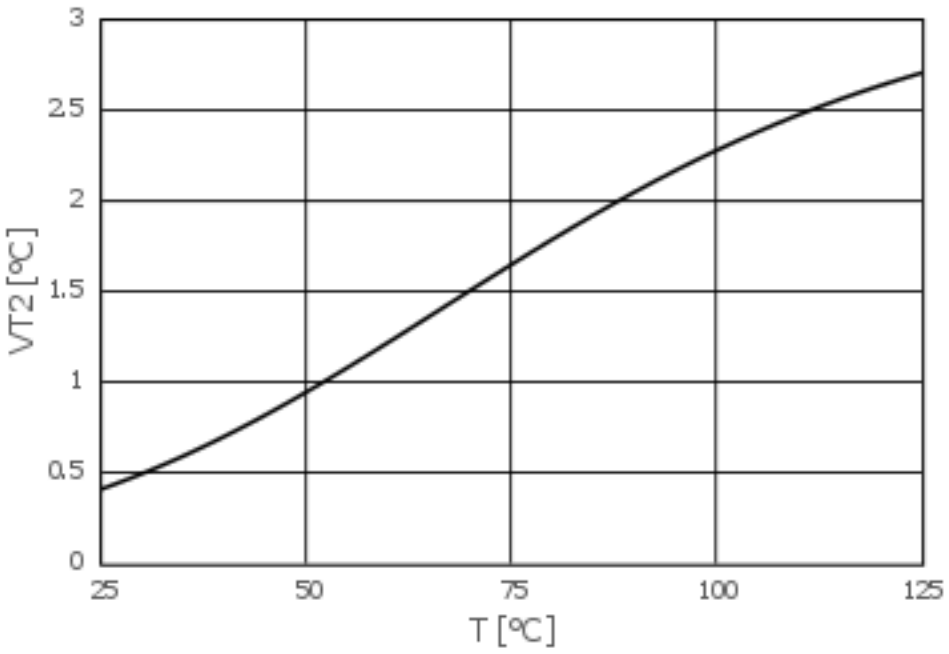
6.2 NTC Thermistor

The embedded thermistor (85 kΩ at 25 °C) in the IPM is connected between pins T1 and T2 (26, 25).

A12 kΩ pull up resistor (R10) ensures that the voltage variation on the NTC as a function of temperature is almost linear. This voltage is easily monitored on TP1 test pin.

The figure below shows the typical voltage on T2 as function of temperature.

Figure 17. **NTC voltage vs temperature**



7 Firmware configuration for STM32 PMSM FOC SDK

The following table summarizes the parameters which customize the latest version of the ST FW motor control library for permanent magnet synchronous motor (PMSM): STM32 PMSM FOC SDK for this STEVAL-IPM10F.

Table 5. ST motor control workbench GUI parameters

Block	Parameter	Value
Over current protection	Comparator threshold	$V_{ref} \cdot \left(\frac{R23 + R53}{R53}\right) + V_F = 0.83V$ (13)
	Overcurrent network offset	0
	Overcurrent network gain	0.1 V/A
Bus voltage sensing	Bus voltage divider	1/125
Rated bus voltage info	Min rated voltage	125 V
	Max rated voltage	400 V
	Nominal voltage	325 V
Current sensing	Current reading typology	Single- or three-shunt
	Shunt resistor value	0.06 Ω
	Amplifying network gain	2.1
Command stage	Phase U Driver	HS and LS: Active high
	Phase V Driver	HS and LS: Active high
	Phase W Driver	HS and LS: Active high

8 Connectors, jumpers and test pins

Table 6. Connectors

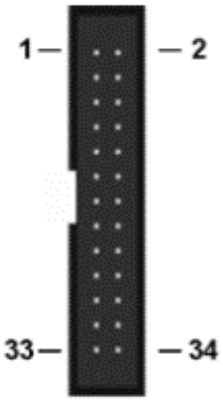
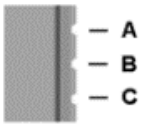
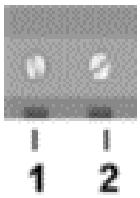
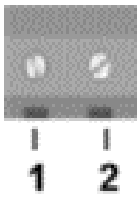
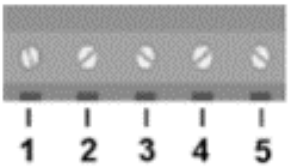
Connector	Reference	Description / pinout	
J2		Motor control connector	
		1 - emergency stop	2 - GND
		3 - PWM-1H	4 - GND
		5 - PWM-1L	6 - GND
		7 - PWM-2H	8 - GND
		9 - PWM-2L	10 - GND
		11 - PWM-3H	12 - GND
		13 - PWM-3L	14 - HV bus voltage
		15 - current phase A	16 - GND
		17 - current phase B	18 - GND
		19 - current phase C	20 - GND
		21 - NTC bypass relay	22 - GND
		23 - dissipative brake PWM	24 - GND
		25 - +V power	26 - heat sink temperature
		27- PFC sync.	28 - VDD_m
		29 - PWM VREF	30 - GND
		31 - measure phase A	32 - GND
		33 - measure phase B	34 - measure phase C
J3		Motor connector • phase A • phase B • phase C	
J4		VCC supply (20 VDC max) • positive • negative	
J7		Supply connector (DC – 125V to 400 V) 1. + (positive terminal) 2. - (negative terminal)	
J9		Hall sensors / encoder input connector 1. Hall sensors input 1 / encoder A+ 2. Hall sensors input 2 / encoder B+ 3. Hall sensors input 3 / encoder Z+ 4. 3.3 or 5 Vdc 5. GND	

Table 7. Jumpers

Jumper	Description	
SW3	TSO/NTC	
	TSO: jumper on 1-2	
	NTC: jumper on 2-3	
SW1	To choose current U to send to control board:	
	Jumper on 1-2: from amplification	
	Jumper on 2-3: directly from motor output	
SW2	To choose current V to send to control board	
	Jumper on 1-2: from amplification	
	Jumper on 2-3: directly from motor output	
SW4	To choose current W to send to control board:	
	Jumper on 1-2: from amplification	
	Jumper on 2-3: directly from motor output	
SW13	To modify phase A hall sensor network	
SW14	To modify phase B hall sensor network	
SW15	To modify phase C hall sensor network	
SW9, SW16	To choose input power for Hall/Encoder	
	Jumper on 1-2: 5 V	
	Jumper on 2-3: 3.3 V	
SW5, SW6 SW7, SW8	To choose one-shunt or three-shunt configuration. (Through solder bridge)	
	SW5, SW6 closed SW7, SW8 open	one shunt
	SW5, SW6 open SW7, SW8 closed	three shunt

Table 8. Test pins

Test Pin	Description
TP1	NTC (T2 pin)
TP2	VBOOTw
TP3	VBOOTv
TP4	VBOOTu
TP5	HinU (high side U control signal input)
TP6	HinV (high side V control signal input)
TP7	HinW (high side W control signal input)
TP8	VCCH
TP9	phase A (U pin)
TP10	phase B (V pin)
TP11	Ground
TP12	LinU (high side U control signal input)

Test Pin	Description
TP13	phase C (W pin)
TP14	LinV (high side V control signal input)
TP15	LinW (high side W control signal input)
TP16	Negative DC input for U phase
TP17	CIN
TP18	Negative DC input for V phase
TP19	Negative DC input for W phase
TP20	TSO (TSO pin)
TP21	Ground
TP22	Ground
TP23	SD (shutdown pin)
TP24	Current_A_amp
TP25	Current_B_amp
TP26	Current_C_amp

9 Bill of materials

The components used to build the evaluation board are listed below. The majority of the active components used are available from STMicroelectronics.

Table 9. Bill of materials

Item	Qty	Reference	Part/Value	Description	Manufacturer	Order code
1	4	C2, C22, C26, C28	10 nF, SMD 1206	Capacitor	AVX	12065C103KAT2A
2	9	C10, C11, C14, C15, C17, C18, C35, C36, C37	10 pF, SMD 1206	Capacitor	AVX	12061A100JAT2A
3	4	C20, C25, C29, C31	330 pF, SMD 1206	Capacitor	AVX	12065A331JAT2A
4	3	C5, C6, C7	2.2 µF, SMD 1206	Capacitor	Murata	GCM31MR71E225KA57L
5	6	C8, C13, C23, C32, C33, C34	100 nF, SMD 1206	Capacitor	AVX	12065C104KAZ2A
6	2	C12, C21	4.7 µF	Electrolytic capacitor	Any	Any
7	2	C19, C16	1 nF, SMD 1206	Capacitor	Kemet	C1206C102K5RACTU
8	1	C9	0.1 µF, SMD 1812	Capacitor	Murata	GRM43DR72J104KW01L
9	3	C24, C27, C30	100 pF, SMD 1206	Capacitor	Kemet	C1206C101J1GACTU
10	2	C3, C4	47 µF	Electrolytic capacitor	Any	
11	5	D1, D3, D4, D5, D6	Diode SOD323	Schottky diode	ST	BAT48J
12	1	D2	2 mA, 3 mm	Red LED	Ledtech	L4RR3000G1EP4
13	1	J2	Connector	Connector 34-pins	RS	625-7347
14	1	J3	7 mm - 3 pole	Connector	TE Connectivity AMP Connectors	282845-3
15	1	J4	5 mm - 2 pole	Connector -	Phoenix Contact	1935161
16	1	J1	7 mm - 2 pole	Connector	On Shore Technology Inc	OSTVI024152
17	1	J5	Connector	Five pins of pin header	RS	W81136T3825RC
18	2	R1, R2	470 kΩ, , SMD 1206	Resistor	Any	
19	1	R4	7.5 kΩ, SMD 1206	Capacitor	Panasonic	ERJP08F7501
20	1	R3	120 Ω, SMD 1206	Resistor	Any	Any
21	3	R7, R13, R17	3.9 kΩ, SMD 1206	Resistor	Any	Any
22	21	R5, R6, R8, R9, R14, R15, R19, R20, R23, R30, R32, R31, R18, R21, R24, R36, R35, R41, R42, R40, R37	Resistor, SMD 1206		Any	Any
23	3	R11, R16, R22	3.3 kΩ	Resistor	Any	Any
24	1	R28	10 kΩ, SMD 1206	Resistor	Any	Any
25	1	R10	12 kΩ, SMD 1206	Resistor	Any	Any

Item	Qty	Reference	Part/Value	Description	Manufacturer	Order code
26	6	R29, R33, R34, R38, R39, R43	2.1 kΩ, SMD 1206	Resistor	Any	Any
27	1	R12	5.6 kΩ, SMD 1206	Resistor	Any	Any
28	3	R25, R26, R27	0.06 Ω, SMD 2512	Resistor	Vishay	WSL2512R1000FEK
29	7	R44, R45, R46, R50, R51, R52, R53	4.7 kΩ, SMD 1206	Resistor	Any	Any
30	3	R47, R48, R49	2.4 kΩ, SMD 1206	Resistor	Any	Any
31	6	SW1, SW2, SW3,S W4, SW9, SW16	Jumper 2.54	Three pins of pin header	RS	W81136T3825RC
32	6	SW10, SW11, SW12, SW13, SW14, SW15	Jumper 2.54	Two pins of pin header	RS	W81136T3825RC
33	12	-	2.54 mm, low profile, connector	-	RS	881545-2
34	2	SW7, SW8		Solder bridge	Any	Any
35	2	SW5, SW6	open	-	Any	Any
36	26	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18, TP19, TP20, TP21, TP22, TP23, TP24, TP25, TP26	PCB terminal 1 mm	Test pin	KEYSTONE	5001
37	1	U1	20 MHz GBP	Rail-to-rail input/ output operational amplifiers, SO14	ST	TSV994
38	1	U2	8 A, 600 V	SLLIMM 2nd series IPM, 3-phase inverter, short-circuit rugged IGBTs	ST	STGIF5CH60TS-L
39	3	RC1,RC6,RC9	0 Ω, SMD 0805	Resistor	Any	Any
40	7	RC2, RC3, RC4, RC5, RC7, RC8, RC10	Not mounted	Not mounted	Any	Any
41	9	to close switch for: SW1, SW2, SW3, SW4, SW9, SW10, SW11, SW12, SW16	-	-	TE Connectivity	1-881545-1

10 PCB design guide

Optimization of PCB layout for high voltage, high current and high switching frequency applications is a critical point. PCB layout is a complex matter as it includes several aspects, such as length and width of track and circuit areas, but also the proper routing of the traces and the optimized reciprocal arrangement of the various system elements in the PCB area.

A good layout can help the application to properly function and achieve expected performance. On the other hand, a PCB without a careful layout can generate EMI issues, provide overvoltage spikes due to parasitic inductance along the PCB traces and produce higher power loss and even malfunction in the control and sensing stages.

In general, these conditions were applied during the design of the board:

- PCB traces designed as short as possible and the area of the circuit (power or signal) minimized to avoid the sensitivity of such structures to surrounding noise.
- Good distance between switching lines with high voltage transitions and the signal line sensitive to electrical noise.
- The shunt resistors were placed as close as possible to the low side pins of the SLLIMM. To decrease the parasitic inductance, a low inductance type resistor (SMD) was used.
- RC filters were placed as close as possible to the SLLIMM pins in order to increase their efficiency.

10.1 Layout of reference board

All the components are inserted on the top of the board. Only the IPM module is inserted on the bottom to allow the insertion of a suitable heatsink for the application.

Figure 18. Silk screen and etch - top side

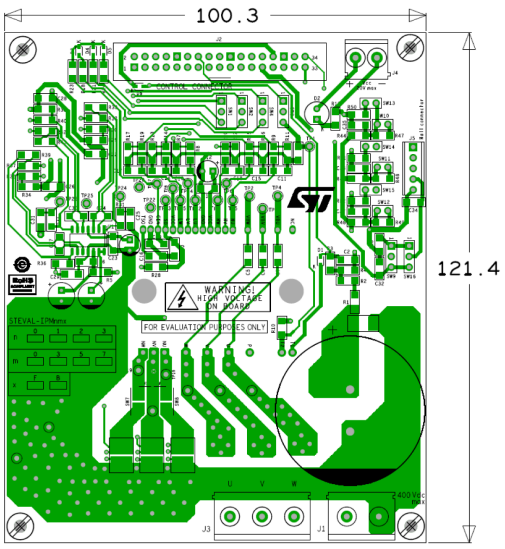
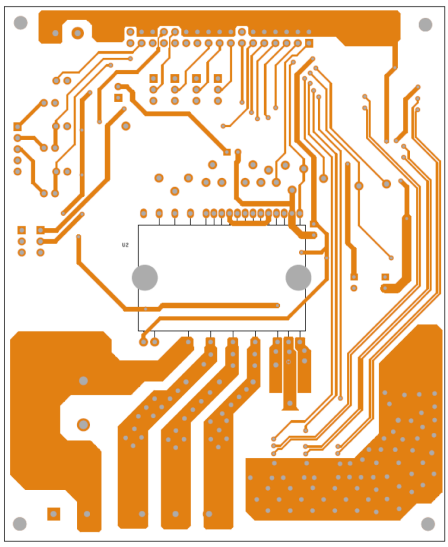


Figure 19. **Silk screen and etch - bottom side**



11 Recommendations and suggestions

- The BOM list is not provided with a bulk capacitor already inserted in the PCB. However, the necessary space has been included (C1). In order to obtain a stable bus supply voltage, it is advisable to use an adequate bulk capacity. For general motor control applications, an electrolytic capacitor of at least 100 µF is suggested.
- Similarly, the PCB does not come with a heat sink. In case of need, place an heat sink on top of the PCB with thermal conductive foil and screws. R_{TH} is an important factor for good thermal performance and depends on certain factors such as current phase, switching frequency, power factor and ambient temperature.
- The board requires +5 V and +3.3 V to be supplied externally through the 34-pin motor control connector J2. Please refer to the relevant board manuals for information on key connections and supplies.

12 General safety instructions

Danger:

The evaluation board works with high voltage which could be deadly for the users. Furthermore all circuits on the board are not isolated from the line input. Due to the high power density, the components on the board as well as the heat sink can be heated to a very high temperature, which can cause a burning risk when touched directly. This board is intended for use by experienced power electronics professionals who understand the precautions that must be taken to ensure that no danger or risk may occur while operating this board.

Caution: After the operation of the evaluation board, the bulk capacitor C1 (if used) may still store a high energy for several minutes. So it must be first discharged before any direct touching of the board.

Important:
To protect the bulk capacitor C1, we strongly recommended using an external brake chopper after C1 (to discharge the high brake current back from the induction motor).

13 References

All of the following reference material is freely available on www.st.com

1. STGIF10CH60TS-L datasheet
2. TSV994 datasheet
3. STTH15R06 datasheet
4. User manual UM1052 *STM32F PMSM single/dual FOC SDK v4.3*
5. Application note AN4076 *Two or three shunt resistor based current sensing circuit design in 3-phase inverters*

Revision history

Table 10. **Document revision history**

Date	Version	Changes
01-Mar-2016	1	Initial release.
16-Apr-2018	2	Updated cover page title. Updated Section 1 Key features Updated Figure 7. STEVAL-IPM10F circuit schematic (5 of 6) Updated Section 9 Bill of materials
18-Sep-2019	3	Updates Figure 5. STEVAL-IPM10F circuit schematic (3 of 6) and Figure 6. STEVAL-IPM10F circuit schematic (4 of 6).

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